Reducing MOSFET $1/f$ Noise and Power Consumption by Switched Biasing

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Abstract—Switched biasing is proposed as a technique for reducing the $1/f$ noise in MOSFET's. Conventional techniques, such as chopping or correlated double sampling, reduce the *effect* of $1/f$ noise in electronic circuits, whereas the switched biasing technique reduces the $1/f$ noise *itself*. Whereas noise reduction techniques generally lead to more power consumption, switched biasing can reduce the power consumption. It exploits an intriguing physical effect: Cycling a MOS transistor from strong inversion to accumulation reduces its intrinsic $1/f$ noise. As the $1/f$ noise is reduced at its physical roots, high frequency circuits, in which $1/f$ noise is being upconverted, can also benefit. This is demonstrated by applying switched biasing in a 0.8 μm CMOS sawtooth oscillator. By periodically switching off the bias currents, during time intervals that they are not contributing to the circuit operation, a reduction of the $1/f$ noise induced phase noise by more than 8 dB is achieved, while the power consumption is also reduced by 30%.

Index Terms—$1/f$ noise, CMOS, flicker noise, MOSFET, noise reduction, oscillators, phase noise, timing jitter.

I. INTRODUCTION

C MOS IC's nowadays contain up to several million transistors, mainly used in digital circuits, but also in analog and mixed analog–digital interface circuits. Charge transport in electronic devices is fundamentally accompanied by random noise. As a result, the signal-to-noise ratio of analog circuits is limited, and bit errors occur in data transmission systems.

Apart from white thermal noise, MOS transistors are notorious for flicker noise or $1/f$ noise with a power spectral density $\mathrm{PSD}(f)$ inversely proportional to frequency f (-10 dB/decade). Below a $1/f$ corner frequency f_c (see Fig. 1), this noise dominates white noise. $1/f$ noise is of increasing worry, as minimum size transistors in newer CMOS processes tend to have higher $1/f$ corner frequencies, typically well above 1 MHz. Moreover, as shown in Fig. 1, the effect of $1/f$ noise is not limited to low frequencies: $1/f$ noise is also upconverted to high frequencies [1], e.g., in active mixers, VCO's [2], and frequency dividers [3]. This is one of the important difficulties in implementing
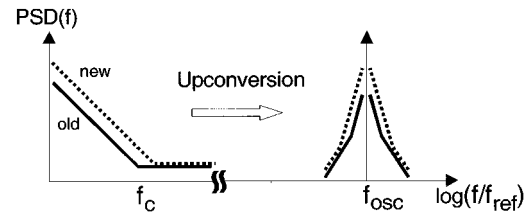
Fig. 1. The $1/f$ corner frequency f_c of minimum size transistors in newer CMOS processes tends to increase. Upconversion, e.g., in oscillators renders also additional noise at high frequencies.

analog CMOS circuits with similar noise performance than their bipolar counterparts.

Circuit techniques like chopping and correlated double sampling reduce the effect that $1/f$ noise has on circuits. In contrast, the current paper proposes a technique that tackles the problem at its physical roots: it *reduces the intrinsic $1/f$ noise itself*. It exploits an intriguing physical effect: Cycling a MOS transistor between strong inversion and accumulation reduces its $1/f$ noise. Although this effect was reported in 1991 [4], [5], it seems to have gone unnoticed to the solid-state circuits community for quite some time.[1] Recently, we showed that the noise reduction effect is relevant for the analysis of $1/f$ noise induced phase noise in ring oscillators with standard CMOS inverters [6]–[8]: about 8 dB phase noise reduction was attributed to the effect.

However, $1/f$ noise problems exist in many other circuits. This paper proposes switched biasing as a technique that can reduce $1/f$ noise in such cases, while simultaneously saving power. The effectiveness of the technique will be demonstrated by applying it to a sawtooth oscillator [9]–[11] realized in 0.8-μ CMOS process (previous work [6]–[8] was based on discrete HEF4007 devices).

The structure of the paper is as follows. In Section II, the problem of $1/f$ noise in MOSFET's is introduced, showing that noise reduction by increasing device dimensions comes at the cost of speed or power consumption. In Section III existing circuit design techniques to reduce $1/f$ noise will be reviewed, to clarify the difference with the switched biasing technique that is proposed in Section IV. In Section V, an application example of switched biasing in a sawtooth oscillator is presented, while experimental results are reported in Section VI. Section VII discusses the application perspective of the technique, while Section VIII ends with conclusions.

[1]No references to [4] and [5] in Science Citation Index '91–'97. The authors published the first results on ISCAS'98 [6].

II. 1/F Noise in MOSFET's

MOSFET noise measurements at low frequencies generally show a spectral density of the input (gate) referred voltage noise which is roughly inversely proportional to frequency f, and the MOS gate area $W \cdot L$.

Although there are probably several different physical mechanisms resulting in $1/f$ noise in MOSFET's, there are strong indications that traps at the Si–SiO$_2$ interface play the most important role [12], [13]. Electron trapping and detrapping can lead to conductance variations. The exact mechanism has been, and still is, subject to discussion. The two following frequently encountered modeling approaches exist:

1) the carrier-density fluctuation model (number fluctuations), predicting an input referred noise density independent of the gate bias voltage and proportional to the square of oxide thickness;
2) the mobility fluctuation model, predicting an input referred noise voltage increasing with gate bias voltage, and proportional to oxide thickness.

Hung proposed a unified model [13] with a functional form resembling the number fluctuation model at low bias and the mobility fluctuation model at high bias. This model is often used as the basis for circuit simulations.

Measurements of devices from many different CMOS processes with oxide thickness between 10–80 nm suggest that nMOS transistors behave as predicted by the number fluctuation model [14]. In the same study, the pMOS devices show a lower $1/f$ noise, which is however bias dependent, as in the mobility fluctuations model.

Noise measurements of newer deep sub-micron transistors render a much less consistent picture. For instance, nMOS transistors also may show bias dependence, while pMOS transistors may have a $1/f$ noise corner frequency comparable to nMOS transistors. In ultra thin oxide MOS transistors (e.g., 1.5 nm [15]), new $1/f$ noise mechanisms may even play an important role, e.g., due to direct tunneling currents.

From a designer's perspective, a pragmatic view is usually taken, concentrating on the question: given a certain IC process, what can I do to reduce the $1/f$ noise? The main controllable parameters are the W and L of the transistor and its biasing. Obviously, changing the biasing only helps for transistors showing significant bias dependence (as for the mobility fluctuation model). However, the biasing also affects many other important circuit performance aspects like transfer function, signal swing, speed, linearity and current efficiency. Due to the many tradeoffs, changing the bias is rarely practical. Increasing the gate area WL at constant W/L and constant bias has much less impact on most of the performance aspects mentioned. The main disadvantage in this case is the increase in gate-capacitance and resulting speed penalty.[2] By lowering the impedance level, the loss in speed can be compensated. However, a lower impedance level generally requires higher

transconductance values of the transistor, resulting in more power consumption.

In summary, it is concluded that the only practical way to reduce $1/f$ noise is by increasing device gate area. However, this comes at the cost of speed or power consumption.

III. Existing $1/f$ Noise Reduction Techniques

In this section, known circuit techniques for $1/f$ noise reduction will be reviewed briefly, in order to make a clear distinction between these techniques and the switched biasing technique and to be able to evaluate their relative benefits.

A. Keep $V_{DS} = 0$

$1/f$ noise relates to conductance variations. Thus, the noise current becomes zero for a MOS operating in the triode region at $V_{DS} = 0$ V. This property is useful in resistive circuits, for instance in current dividers [18] or transconductors [19]. However, if V_{DS} is increased, the $1/f$ noise comes up. Furthermore, almost all transistor circuits require voltage amplification, while a MOS transistor in the triode region has a maximum "intrinsic voltage gain" of 1. The vast majority of MOS circuits exploit MOS transistors operating in saturation, i.e., $V_{DS} \neq 0$.

B. DC Offset and Drift Reduction Techniques

DC offset and drift are basic problems in analog circuits, and several techniques have been developed to reduce the resulting low frequency errors. Examples of such techniques are chopper stabilization [16], auto-zeroing techniques (correlated double sampling [16]), dynamic element matching [20], dynamic current mirrors [21] and current copiers [22]. As $1/f$ noise at low frequencies is indistinguishable from drift, a reduction of low frequency $1/f$ noise is also achieved. The reduction factor is typically limited by device mismatch, timing errors and charge injection. All these techniques are limited to use at low frequencies. They do not help to reduce upconverted $1/f$ noise.

C. Reduce the Upconversion of $1/f$ Noise

Recently Hajimiri proposed a theory that is useful to quantify the upconversion effect of $1/f$ noise in oscillators [1]. The oscillator is modeled as a linear time variant system, and an impulse sensitivity function is defined that characterizes the sensitivity to upconversion. Based on this theory, it can be shown that symmetry in the oscillator waveform helps to minimize the upconversion [23]. However, the achievable symmetry is limited especially in cases where complementary devices are used. Furthermore, noise on the control input of a controlled oscillator remains a problem.

D. Phase-Locked Loop (PLL)

In a PLL the phase of a voltage controlled oscillator (VCO) is locked to the phase of a reference signal by means of a phase detector with feedback loop. If the reference is clean, the PLL suppresses the phase noise of the VCO by an amount determined by the loop gain [24]. Although this is a very useful commonly used technique, it has its limitations. For frequencies larger than the loop bandwidth, the phase noise of the (effectively free running) VCO still determines the phase noise of PLL. Hence, $1/f$

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[2]Assuming a bias independent input referred PSD(f) which is inversely proportional to $W \cdot L \cdot C_{ox}$ (instead of to $W \cdot L \cdot C_{ox}^2$, consistent with the number fluctuation model and [13]), it can be derived that there is a fixed ratio between transit frequency $f_t \approx g_m/(2\pi C_{gs})$ and $1/f$ corner frequency f_c. Hence, reducing f_c implies reducing f_t (there is no design freedom!).
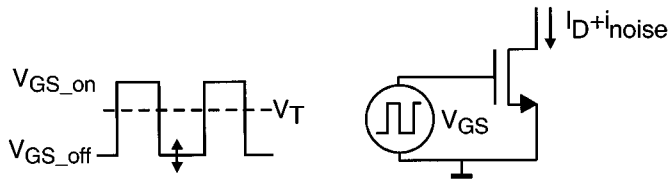
Fig. 2.   Varying V_{GS} cycles a MOSFET between strong inversion (V_{GS_on}) and accumulation (V_{GS_off}) ($V_{DS} > V_{DS, SAT}$).

noise can be a problem, especially for applications requiring a low loop bandwidth [8]. Within the loop bandwidth, the noise contribution of the phase detector and the frequency divider, that is often present between the VCO and phase detector, is a source of phase noise contributions that are not attenuated by the loop gain [24]. Hence, noise improvements are wanted in these blocks.

In summary, several circuit techniques have been discussed that reduce the effect of $1/f$ noise in circuits. Most of them are only effective at low frequencies, and do not help to reduce problems with upconverted $1/f$ noise. Minimizing upconversion by improving waveform symmetry or by using a PLL helps, but even then further improvements are desired, e.g., in oscillators, mixers, phase detectors and frequency dividers. We will now discuss switched biasing as a technique that tackles the $1/f$ noise in a very different way.

IV. SWITCHED BIASING: REDUCE $1/f$ NOISE ITSELF

A. Cycling between Strong Inversion and Accumulation

In 1991, Bloom and Nemirovsky [4] were the first to report that cycling a MOS transistor between strong inversion and accumulation reduces its $1/f$ noise observed in strong inversion. Shortly after, their results were reconfirmed and related to random telegraph signals [5]. We rediscovered the effect in ring oscillator phase noise experiments [8], and seem to be the first to exploit its impact on CMOS circuits.

Fig. 2 illustrates the basic idea of cycling a transistor between strong inversion and accumulation for an nMOST (nMOS transistor). A voltage source with a square wave signal switches the gate-source voltage of the nMOST between two bias values. The high level, V_{GS_on}, is larger than the threshold voltage, so that the transistor is biased at a constant voltage in strong inversion (nMOST is "on"). The low level, V_{GS_off}, is equal or lower than the threshold voltage (nMOST is "off") and is variable. Depending on V_{GS_off}, the low state of the square wave corresponds to biasing in moderate inversion, weak inversion or finally accumulation (holes in the p-bulk accumulate under the gate-oxide).

Using a new wideband measurement setup exploiting a differential probe [25], we did noise measurements on commercially available HEF4007 devices from six different IC manufacturers. Fig. 3 shows a typical result obtained for switching at 10 kHz and observing the spectrum from 10 Hz to 100 kHz. The peaks in the spectrum result from the switching and from 50 Hz interference. The upper line shows a noise spectrum from 10 Hz–100 kHz, which has roughly a $1/f$ decay (actually the slope is somewhat smaller than -10 dB/decade).
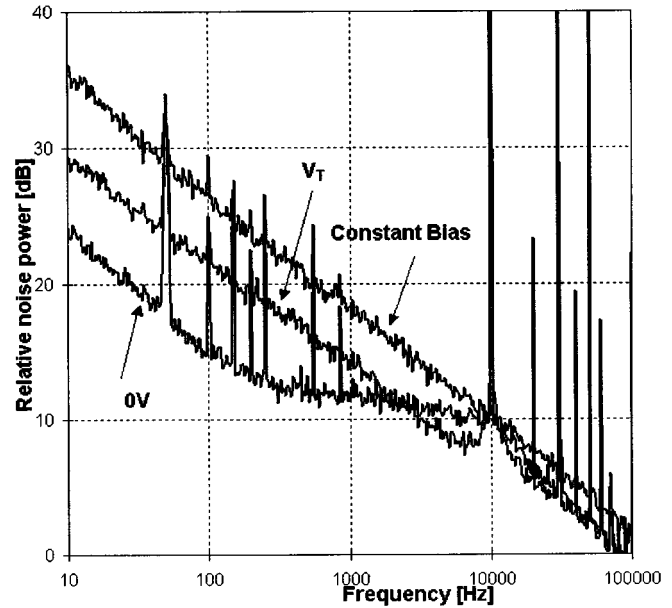

Fig. 3. $1/f$ noise baseband spectrum of HEF4007 MOSFETS at constant bias and switched bias (10 kHz) at 50% duty cycle for V_{GS_off} equal to V_T (=1.5 V) and 0 V (indicated in the figure).

The middle line renders the spectrum for V_{GS_off} equal to V_T (=1.5 V). The noise power is roughly 6 dB lower. This is what we can expect for 50% duty cycle, as the switching operation can be represented as a multiplication of the $1/f$ noise current with a square-wave signal with 50% duty cycle, $m(t)$, as follows:

$$m(t) = \frac{1}{2} + \frac{2}{\pi} \cdot \sin \omega_{sw} t + \frac{2}{3\pi} \sin 3\omega_{sw} t + \frac{2}{5\pi} \sin 5\omega_{sw} t + \cdots. \tag{1}$$

In the frequency domain this corresponds to a convolution of the PSD of the $1/f$ noise with a spectrum with delta functions at dc, ω_{sw}, $3\omega_{sw}$, $5\omega_{sw}$, etc. The dc-term determines the resulting noise power in baseband, which is $(1/2)^2$ (or -6 dB) compared to the original $1/f$ noise power.
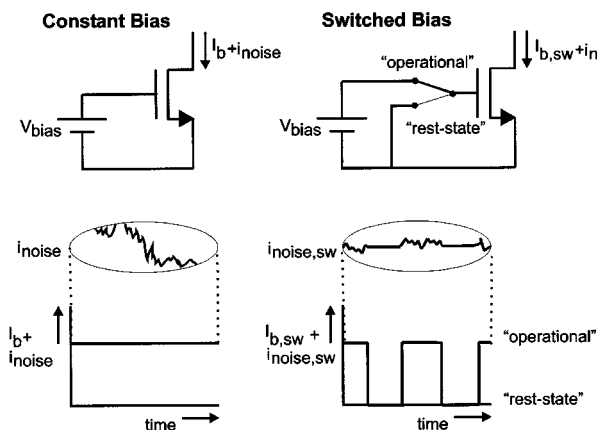
Indeed 6 dB reduction is observed in Fig. 3 for V_{GS_off} equal to V_T. However, if we decrease V_{GS_off} below V_T down to 0 V, an anomalous noise reduction of 8 dB is found!

This cannot be explained from modulation theory: The transistor in the off-state was already contributing negligible noise when $V_{GS\text{-off}}$ was equal to V_T. A further reduction in $V_{GS\text{-off}}$ is not supposed to have any effect. However, experiments show that the value $V_{GS\text{-off}}$ has a strong effect on the noise reduction, which is maximal when $V_{GS\text{-off}}$ corresponds to accumulation [4]. Measurements on 4007 devices from six different manufacturers show between 5 and 8-dB maximum noise reduction [25].

Another issue that is important is the duty-cycle dependence. Of course, the dc-term in (1) changes with duty cycle, and so do the high frequency components. Correcting for this effect, the duty cycle in experiments had no effect on the noise reduction up to switching frequencies of 1 MHz [25].

B. Switched Biasing Technique

With knowledge of the $1/f$ noise reduction effect, the switched biasing technique can now be defined. Fig. 4 illustrates the principle of switched biasing and compares it to

Fig. 4. Concept of switched biasing ($V_T > 0$).

Fig. 5. Principle of gradual turn-on of the charge-current for a capacitor in the sawtooth oscillator.

constant biasing. Instead of applying a constant gate-source bias, a MOS transistor is periodically switched between two states: 1) an "operational state" or "active state" in strong inversion, in which it contributes to the functional operation of a circuit (e.g., delivers a bias current); and 2) a "rest-state" or "inactive state" in—or close to—accumulation. In this state the MOS transistor is not operational. This rest-state is introduced with the purpose of *reducing the $1/f$ noise* of the MOS transistor *during its operational state*. Furthermore it reduces the power consumption.

For practical purposes an off-voltage of $V_{gs} = 0$ V is preferred, as the implementation is simply short-circuiting the gate to the source.

Of course, periodically switching transistors between an operational state and a rest-state is not always possible without affecting correct circuit operation. However, some circuits offer this freedom, for example because a bias current is needed only during certain time intervals or because signal processing is not taking place continuously.

Oscillators are among these circuits: In many types of oscillators, the transistors contribute actively to the circuit's operation during only a fraction of the period of oscillation. This part-time usage of transistors allows for periodic switch-off during nonoperational phases. In Section V an example of such an oscillator will be described.

V. APPLYING SWITCHED BIASING

To enable a quick verification of the ideas presented in Section IV, an integrated CMOS sawtooth oscillator which was already available [9] is used as an implementation vehicle for the "switched bias technique." This oscillator was designed for FM demodulation in video-recorders with hifi sound quality. It has the following properties:

- It combines a high control linearity with low phase noise at low power (THD < -70 dB for 1.8 MHz center frequency and ± 500 kHz frequency modulation; phase noise -103 dBc/Hz @ 10 kHz; $P = 1.8$ mW).
- Its phase noise performance has been improved to the extent that only the noise on the currents that periodically charge the oscillator's capacitors remains. For low frequencies, $1/f$ noise dominates the phase noise.
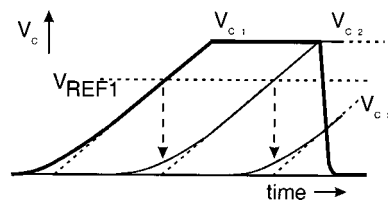
- The oscillator consists of a ring of identical stages that are active only part of the time. Applying switched biasing seemed attractive, as both power consumption and $1/f$ noise could benefit.

For sake of clarity, a brief review of the operation and characteristics of the oscillator will now be given. Then the $1/f$ noise problem in this oscillator is discussed, and the implementation of switched biasing to improve performance.

A. Coupled Sawtooth Oscillator

The coupled sawtooth oscillator to be discussed is a controllable relaxation oscillator based on a new principle [10], [11] that allows low phase noise to be achieved in combination with high control linearity. Compared at equal control linearity and power dissipation, the phase noise of this type of oscillator is significantly lower (14 dB) than that of a conventional relaxation oscillator. This is achieved by using an alternative for the Schmitt trigger that is commonly used in a relaxation oscillator to periodically reverse the capacitor current each time the capacitor voltage crosses one of the trigger's two threshold levels. The noise present on these decision levels is the dominant contributor to phase noise in a conventional relaxation oscillator [17]. This is due to the fast decisions taken by the trigger circuit, resulting in nearly ideal sampling of the threshold-level noise. As a consequence, over a large bandwidth the threshold-level noise is converted into phase noise. In a relaxation oscillator with a Schmitt trigger, high linearity requires a high speed Schmitt trigger [10], [11]. This leads to a tradeoff between linearity and phase noise.

In the coupled sawtooth oscillator these issues are decoupled by *gradually turning on a capacitor's charge current* instead of instantly, as happens in the regenerative oscillator.

It consists of a ring of identical stages each of which subsequently produces a rising voltage ramp across a capacitor. Its construction is such that only rising edges of the capacitor voltages and a reference voltage V_{REF1} determine the timing (see Fig. 5).

Fig. 6 shows the circuit schematic of stage n of a coupled sawtooth oscillator consisting of a ring of six stages. The operation of the circuit is as follows. Transistor M_4 supplies the charge current I_b that is mirrored to become the tail current I_b of the differential pair $M_{1,2}$. This differential pair *gradually* starts charging the capacitor with I_b as soon as the capacitor voltage in stage $(n-1)$ reaches the vicinity of the bias level V_{REF1}.

Of course the capacitors should also be discharged. The timing of the discharge is noncritical, as only rising edges are used to couple the individual stages. Transistor M_3, whose gate is driven by two inverters in series, discharges the capacitor
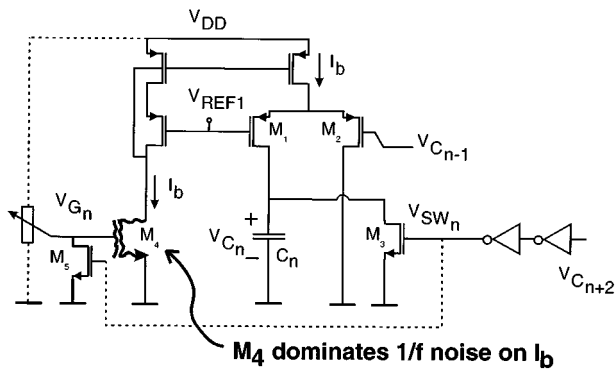
Fig. 6.   Circuit schematic of section n of the coupled sawtooth ring oscillator.

during the time that the capacitor voltage in stage $(n + 2)$ is larger than the inverter's decision level.

It can be shown [10] that this gradual start-up of the charge current does not introduce any deterioration of the oscillator's control linearity, due to the point-symmetrical transfer function of the differential pairs that are used to implement the gradual turn-on. Moreover, this gradual start-up leads to low phase noise as the noise present on the threshold-level V_{REF1} is effectively lowpass filtered due to the long start-up time of the ramp (in contrast to wideband sampling of noise by instantaneous switching in a traditional Schmitt-trigger-based relaxation oscillator). Fig. 7 gives a qualitative time-domain impression of this filtering. Also shown in this figure is the time error Δt_{trig} that would result if a trigger circuit is used to instantly start a new capacitor voltage ramp. For the same control linearity, its variance is much larger than the variance of the time error Δt_{saw} appearing in the sawtooth oscillator. The key point here is that the long start-up time does not affect control linearity, while it reduces phase noise. In a relaxation oscillator with a Schmitt trigger, high linearity requires a high-speed Schmitt trigger [10], [11].

B. Switched Biasing Implementation

As a result of the filtering of the threshold-level noise, the $1/f$ noise present on the capacitor's charge current now appears to be the dominant contributor to phase noise in the coupled sawtooth oscillator. At low frequencies, $1/f$ noise dominates the noise performance. This is visible from the -30 dB/dec slope in the phase noise spectrum of the oscillator shown in Fig. 8.

Thus, it makes sense to further reduce the $1/f$ induced phase noise of the coupled sawtooth oscillator using the switched bias technique. The oscillator's operation allows the current I_b, and thus the $1/f$ noise contributing transistors, to be switched off when the capacitor in a particular stage is not producing a rising ramp. The easiest way to implement this is to switch off these transistors at the same time as the capacitor is discharged. In this way *no change at all* will be noticeable in the capacitor *waveforms* and the oscillator's timing is not harmed in any way. The signal, necessary to switch the transistors, is supplied by the oscillator itself.

As the capacitor waveforms remain the same, no change in the amount of upconversion of $1/f$ noise is expected [1]. As a result, any change in the $1/f$ noise-induced phase noise when
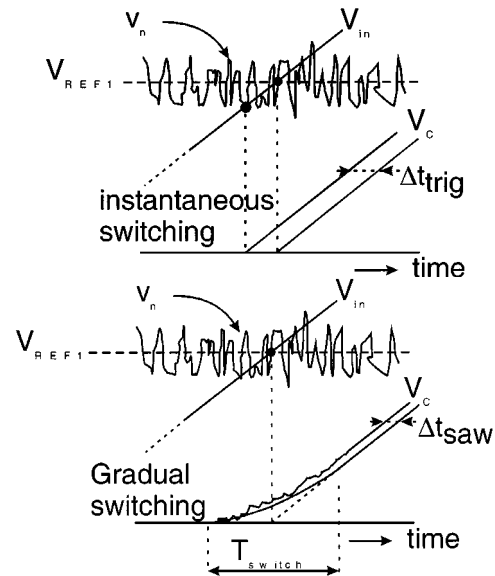

Fig. 7.   Effective filtering of noise v_n on the threshold level V_{REF1} in the coupled sawtooth oscillator results in a smaller time error Δt_{saw} due to gradual turn-on compared to the time error Δt_{trig} that would appear in a regenerative oscillator (instantaneous switching).
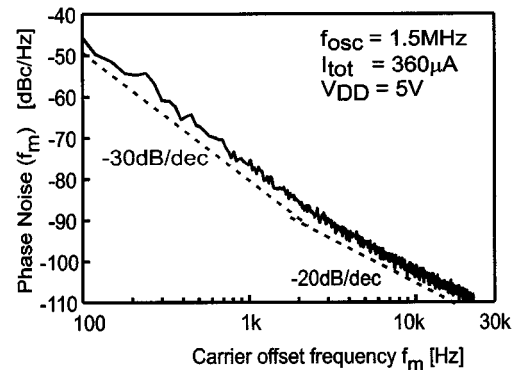

Fig. 8.   Phase noise [dBc/Hz] of the sawtooth oscillator as a function of carrier offset: below 2 kHz, $1/f$ noise dominates (-30 dB/dec).

applying switched biasing *is to be explained by a change in the transistors' intrinsic $1/f$ noise.*

In the experiments to be described, an integrated version of the sawtooth oscillator was used with extra bond-outs for capacitors and bias currents. In the available IC's, not all transistors that contribute $1/f$ noise to the current I_b were accessible. In order to demonstrate the feasibility of the switched bias technique, it is applied to one external current-bias transistor M_4 (see Fig. 6) which is available on the same die as the oscillator circuit. Transistor M_4 has a small $W/L = 4/0.8$ such that its $1/f$ noise dominates in the current I_b. Of course this is not optimal for overall $1/f$ noise minimization, but the main issue here is to show the feasibility of a technique. To further simplify the experimental setup, the switched bias technique was applied only to one stage. In the other stages, external low-noise current sources were used. Note that these simplifications are only made because of limited availability of IC's. However, they can just as well be applied to the other current source devices.

The dashed lines in Fig. 6 show the implementation of the switched biasing in the coupled sawtooth oscillator: transistor
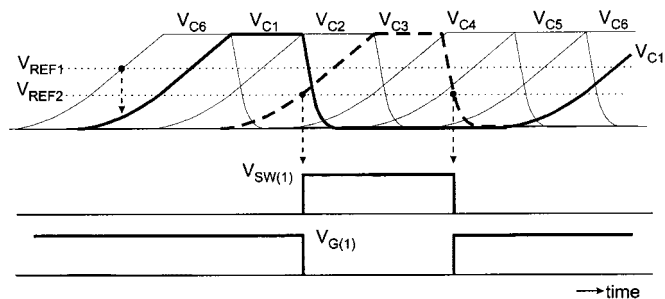
Fig. 9. Capacitor voltages of the 6-stage coupled sawtooth oscillator and signals V_{SW} and V_G that are used in stage 1 (see Fig. 6 with $n = 1$) to respectively discharge C_1 and accomplish switched biasing.
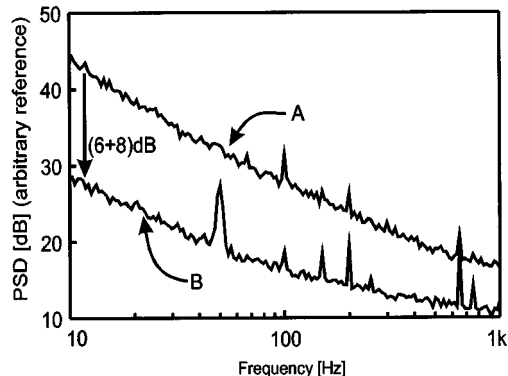

Fig. 10. Measured baseband noise spectra of an nMOST with $W/L = 4/0.8$ ($V_T = 0.7$ V) for constant bias (curve A) and switched bias (curve B: $f_{switch} = 100$ kHz, duty-cycle $= 50\%$, $V_{GS\_on} = 1.5$ V, $V_{GS\_off} = 0$ V).

M_5 switches off the bias transistor M_4 at the same time as transistor M_3 discharges the capacitor. Fig. 9 shows the gate voltage $V_{SW(1)}$ of transistors M_3 and M_5 in stage 1 together with the resulting gate voltage $V_{G(1)}$ of bias transistor M_4.

We will now discuss the measurement result obtained for both constant bias and switched bias mode, for direct comparison.

VI. EXPERIMENTAL RESULTS

Before doing phase noise measurements, the $1/f$ noise of the available 0.8 μ CMOS nMOS transistors were evaluated in baseband, using the switched-bias measurement setup proposed in [25]. The measured noise spectra for nMOS devices with $W/L = 4/0.8$ are shown in Fig. 10.

Curve A shows the $1/f$ noise spectrum measured with the devices constantly biased at a gate-source voltage of 1.5 V ($V_T = 0.7$ V), and curve B shows the noise spectrum of the devices switched periodically between 1.5 V and 0 V with a 100 kHz, 50% duty cycle square-wave signal. Apart from the expected reduction of 6 dB (see Section IV), the measurements show an additional reduction in $1/f$ noise spectral density of about 8 dB at low frequencies, which is in the same order of the results reported in [4], [5], [8], and [25] (spectral peaks are due to 50 Hz related interference).

The devices characterized above were used to implement switched biasing in the current source of the sawtooth oscillator, in the way described in the previous section. From the baseband experiment we expect 8 dB phase noise reduction. Due to limitations of the experimental setup, the oscillator
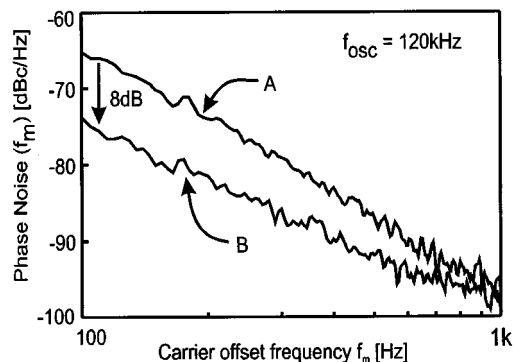

Fig. 11. Phase noise (dBc/Hz) of the sawtooth oscillator as a function of carrier offset frequency for the constant bias (curve A) and switched bias condition (curve B): 8 dB reduction is achieved at 100 Hz.

is running at a rather low frequency $f_{osc} = 120$ kHz. As expected, the application of switched biasing does not visibly affect the oscillator's capacitor waveforms observed with an oscilloscope. However, a large difference is measured in the oscillator phase noise shown in Fig. 11: for switched biasing (curve B) the phase noise at 100 Hz carrier-offset frequency is *about 8 dB lower than for constant biasing*. As motivated in the previous Section, this reduction is to be explained *by a change in the transistors'* $1/f$ *noise*. Indeed, the amount of reduction is in compliance with the reduction observed in the baseband measurements of Fig. 10.

The experiment shows that switching off a transistor during phases in which it is not actively contributing to the circuit's operation helps to reduce its $1/f$ noise during active phases. In addition, the *power consumption* in stage 1 is *reduced* by more than 30%.

Although switched biasing is applied to just one current source in this experimental circuit, it can of course just as well be applied to the other current sources. As all oscillator sections are identical and contribute to the phase noise equally, the same reduction in phase noise is expected in that case.

Of course, the same noise performance can be achieved by using large devices in the current sources. However, with switched biasing we can use smaller devices to obtain the same noise performance and in addition achieve a reduction in power consumption.

VII. DISCUSSION AND APPLICATION PERSPECTIVE

In Section VI we showed that switched biasing results in lower $1/f$ noise-induced phase noise. However, the technique is not limited to use in oscillators. We will now make some notes on its application perspective.

First of all, the fact that switched biasing tackles $1/f$ noise at its physical roots is important. The switched bias technique effectively reduces the $1/f$ noise corner frequency, without a speed or power dissipation penalty. In contrast, we showed that a reduction in power consumption can simultaneously be achieved.

Tackling the $1/f$ noise at its physical roots is essentially different from other techniques. It is *not* the *effect* of the $1/f$ noise that is reduced, but the $1/f$ *noise itself*. The beneficial effects of switched biasing are therefore *not limited* to low frequencies,

but can also reduce $1/f$ noise problems in high frequency circuits. This raises the question whether high frequency switching is just as effective in reducing $1/f$ noise as it is at low switching frequencies. In our experiments so far we demonstrated $1/f$ noise reduction up to switching frequencies of a few MHz. No duty-cycle dependence was found after correction for the modulation effect (see Section IV) [25]. Further experiments are needed to evaluate the $1/f$ noise reduction behavior at higher switching frequencies. Of course a high switching frequency comes at the cost of additional dynamic power consumption, and hence a low switching frequency, e.g., roughly equal to f_c, might be more attractive from a power consumption point of view, while achieving the same beneficial noise reduction.

Quite some electronic circuits are not active all of the time. The part-time activity of circuits can result from their topology, but also from part-time system activity, e.g., in time division multiple access (TDMA) communication systems. If $1/f$ noise reduction is obtained together with a reduction in power consumption, the effort of switching off devices pays off. Especially if switching signals are available in some form, as in the sawtooth oscillator discussed above, implementing switched biasing comes at hardly any additional cost. Applying switched biasing can also be quite straightforward in cases in which switching already takes place, but not with sufficient amplitude. In such cases decreasing the off gate-source voltage might already be sufficient. We showed for instance that $1/f$ noise reduction comes more or less for free in ring oscillators due to the large swing signals that occur there naturally [10]. Implementing switched biasing is expected to be rather straightforward in many discrete-time circuits, e.g., in PLL's, analog-to-digital (AD) converters, frequency dividers, mixers, and switched capacitor-, switched opamp-, and switched-current circuits.

As noted above, switched biasing is completely different from existing $1/f$ noise reduction techniques. It can be viewed as an *orthogonal technique* that can be applied in combination with other noise reduction techniques. Thus the phase noise in an oscillator could for instance be reduced on device level by switched biasing, while simultaneously minimizing the upconversion by maximizing waveform symmetry [1]. Since both techniques have different limitations, in this way *the product of noise reduction factors* of both techniques is obtained.

In order to apply this technique in industrial designs, an improved transistor model must be developed, to allow accurate noise reduction predictions. Actually, switched biasing experiments may enhance the understanding of $1/f$ noise mechanisms as they render new information: Normal $1/f$ noise measurements only show the noise under static biasing conditions, time averaged over a long time. With switched biasing information about the dynamic behavior of the intrinsic noise generation processes is also obtained [25]. This new information may help to validate or falsify noise models.

VIII. CONCLUSIONS

Switched biasing has been proposed as a new circuit technique. It introduces off-switching of MOS transistors during the time they are not actively contributing to the circuit's operation.

This not only saves power, but also *reduces the intrinsic $1/f$ noise* of the switched MOSFET's during active phases. The feasibility of the technique was demonstrated in a 6-stage coupled sawtooth oscillator [10] running at $f_{\mathrm{osc}} = 120$ kHz. Experiments demonstrate the effectiveness of the technique: 8 dB reduction of the $1/f$ noise induced phase noise is achieved, while the power consumption is reduced by more than 30%. The authors believe that switched biasing can be useful in many other circuits, especially in cases where upconversion of $1/f$ noise occurs.

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