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STRAY-INSENSITIVE SWITCHED-CAPACITOR SAMPLE-DELAY-HOLD BUFFERS FOR VIDEO FREQUENCY APPLICATIONS

Indexing terms: Switched capacitor networks, Discrete time systems

Two video frequency switched-capacitor sample-delay-hold (SDH) buffers are presented. The circuits provide a correct transition from the continuous-time to the discrete-time domain or vice versa. Experimental results show an excellent frequency behaviour for clock frequencies up to 25 MHz.

Introduction: Switched-capacitor (SC) circuits are analogue discrete-time signal processing circuits. At the front-end of these circuits, the continuous-time input signal has to be transformed into a discrete-time version. To optimise the settling speed of the SC circuit by creating step-input settling responses, the input interface circuit has to transform the continuous-time input signal into a uniform-sampled full period sample-and-hold (SH) signal. At the back-end of the SC circuit, the transition from the discrete-time to the continuous-time domain has to be made. Owing to the finite circuit time constants of the SC circuit, the output signals will contain continuous-time transients, even for true full period SH input signals. Therefore, an output interface circuit is required to sample the output signal of the SC circuit at the ends of the settling periods and to transform the obtained signal sample sequence into a full period SH signal. Obviously, the use of the input and output interface circuits is especially advantageous in high-frequency SC circuits, in which the accuracy of the signal processing is affected by the finite settling speeds of the continuous-time subcircuits.

The commonly applied interface circuit is the delay-free sample-and-hold buffer, operating on a biphase 50% duty cycle clock pattern as shown in Fig. 1. The delay-free tracking phase ϕ_2 causes a continuous-time input settling response of the amplifier during this tracking phase. A cascade of two delay-free SH buffers, driven by opposite clock phases, is necessary to obtain a full period SH signal. For a biphase SC filter using both clock phases as sampling phase (double-sampling),[1,2] three amplifiers are required to realise the SH signal during both clock phases.

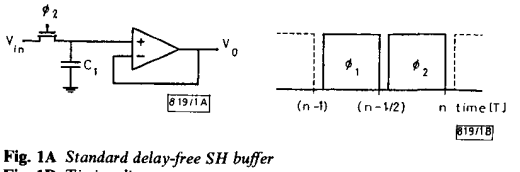

Fig. 1A *Standard delay-free SH buffer*
Fig. 1B *Timing diagram*

This paper presents two novel input/output interface circuits, which realise a full period SH signal with the use of only one amplifier.[2] The introduction of a half period delay between the input and output signal samples guarantees an optimal step-input settling response of the amplifier.

Stray-insensitive sample-delay-hold buffers: Fig. 2*a* shows a stray-insensitive sample-delay-hold (SDH) buffer suitable for biphase single-sampling SC filters. The transfer function of

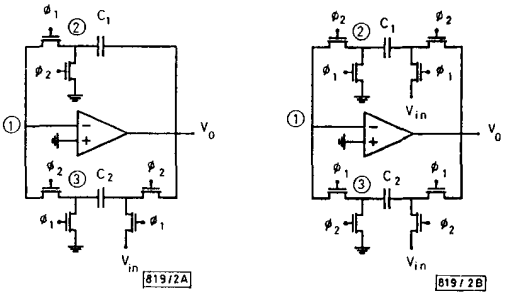

Fig. 2A *Single-sampling SDH buffer*
Fig. 2B *Double-sampling SDH buffer*

this circuit can be found from the difference eqns. 1 and 2:

$$\phi_2: \quad V_0(n) = \frac{C_2 V_{in}(n-1/2) + Cp_1 V_0(n-1/2)/A}{C_2 + [C_2 + Cp_1 + Cp_3]/A} \tag{1}$$

$$\phi_1: \quad V_0(n-1/2) = \frac{[C_1 + Cp_1/A]V_0(n-1)}{C_1 + [C_1 + Cp_1 + Cp_2]/A} \tag{2}$$

These equations include the effects caused by a finite open-loop gain A of the amplifier and by the stray capacitances at the circuit nodes 1, 2 and 3. For $A \gg 1$, the output signal of the SDH buffer only changes values at the beginning of clock phase ϕ_2 and holds this value over a full clock period. A double-sampling implementation of the SDH buffer is shown in Fig. 2*b*.

Assuming identical parasitic capacitances at the nodes 1, 2 and 3 in Figs. 2*a* and *b* and $C_1 = C_2$, eqn. 1 is valid during both clock phases. For $A \gg 1$, the periodic output spectrum of the ideal SDH buffers is

$$V_{OUT}(\omega) = \sum_{n=-\infty}^{n=+\infty} V_{IN}(\omega - n\omega_T)e^{-j(\omega - n\omega_T)T/2}[1 - e^{-j\omega T}]/j\omega T$$
$$= \sum_{n=-\infty}^{n=+\infty} V_{IN}(\omega - n\omega_T)e^{jn\pi}e^{-j\omega T} \sin(\omega T/2)/(\omega T/2) \tag{3}$$

with a sample period T and $\omega_T = 2\pi/T$. Note that in the double-sampling implementation the sample frequency is twice the clock frequency. For applications of the SDH buffers in the video frequency range, high-performance amplifiers with a transconductance in the order of several mA/V and a slew-rate in the order of hundreds of mV/ns have to be used. To prevent saturation of the amplifiers during the non-overlapping time slots of the biphase clock pattern, the continuous feedback technique,[3] shown in Fig. 3, will be added to both SDH buffers.

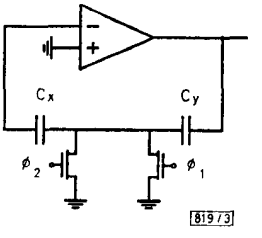

Fig. 3 *Continuous feedback technique*

Experimental results: The single- and double-sampling SDH buffers have been realised using capacitances C_1, C_2, C_x and C_y of 0·28 pF. The switches are realised with transmission gates consisting of 60/2·5 μm NMOS and 60/3 μm PMOS transistors. The widths of the switch transistors in the feedback loops are 30 μm. The amplifiers are BiCMOS folded-cascode transconductance amplifiers with an experimental DC-gain of 69 dB and a unity-gain frequency of 98 MHz. The gain responses of the SDH buffers have been measured for clock frequencies of 1, 5 and 25 MHz. Fig. 4*a* shows the experimental gain response of the single-sampling SDH buffer for which the sample and clock frequency are equal. The experimental results of the double-sampling SDH buffer are shown in Fig. 4*b* for the same clock frequencies. The doubling

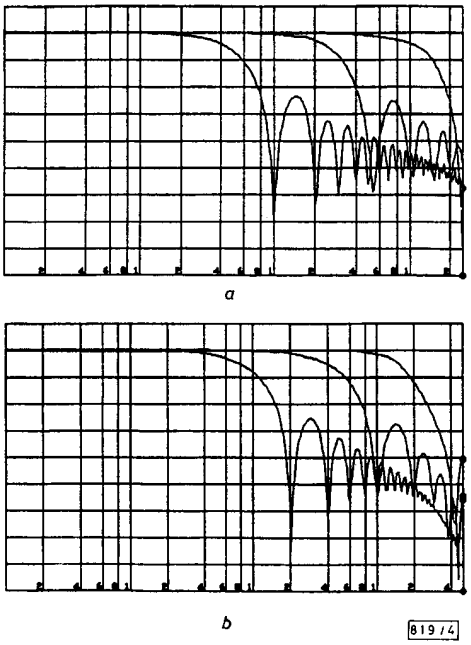

Fig. 4 *Experimental gain response (vert. 5 dB/div) of SDH buffers for clock frequency of 1, 5 and 25 MHz*
a Single-sampling
b Double-sampling

of the sample rate is demonstrated clearly. Fig. 5 shows the phase response of the single- and double-sampling SDH buffer for a 25 MHz clock frequency. The ideal phase response $-2\pi f_{IN}/f_{CLOCK}$ is met very closely. The circuits operate at a $\pm$2·5 V power supply. The experimental dynamic range for 1% distortion (0·8 V_{PP} input signal) is 52·5 dB for the double-sampling SDH buffer (bandwidth = 5 MHz) and 49·5 dB for the single-sampling version (bandwidth = 2·5 MHz).

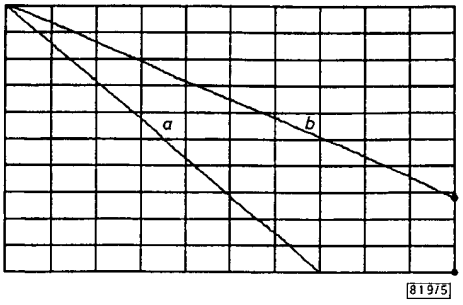

Fig. 5 *Experimental phase response (vert. 5 deg/div) of SDH buffers for clock frequency of 25 MHz*
a Single-sampling
b Double-sampling

Conclusions: Two stray-insensitive switched-capacitor sample-delay-hold buffers for video frequency applications are presented. Both buffers use only one amplifier and can be used as input or output stage for SC video frequency filters.

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ERROR PROBABILITY OF COHERENT PSK AND FSK SYSTEMS WITH MULTIPLE COCHANNEL INTERFERENCES

Indexing terms: Errors, Phase-shift keying, Frequency/shift keying, Interference, Noise

The symbol error probability of binary and quaternary CPSK and binary CPSK systems with multiple cochannel interferences and Gaussian noise is investigated. Numerical results obtained by using the Monte Carlo method are presented as an example.

Introduction: A great amount of work has been devoted to evaluating the performance of digital communication systems with interference and noise. But only an upper bound on error probability is given for the case of multiple interferences with unequal amplitude. It seems rather pessimistic to take the upper bound as a design criterion. In this letter, the error probability of binary and quaternary CPSK and binary CPSK systems corrupted by multiple cochannel interferences and noise is investigated and a better result has been obtained.

Mathematical analysis: Three assumptions are made in the analysis.

(i) The noise is a zero-mean stationary Gaussian process. It can be written as

$$N(t) = N'(t) \cos \omega_0 t - N''(t) \sin \omega_0 t \quad (1)$$

where $N'(t)$ and $N''(t)$ are zero-mean independent stationary low-pass Gaussian random processes with power equal to

$$\sigma^2 = E[N(t)]^2 = E[N'(t)]^2 = E[N''(t)]^2 \quad (2)$$