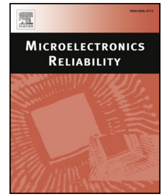
Microelectronics Reliability 88–90 (2018) 147–151

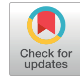
Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel



Towards understanding recovery of hot-carrier induced degradation



Maurits J. de Jong*, Cora Salm, Jurriaan Schmitz

MESA+ Institute for Nanotechnology, University of Twente, Enschede, The Netherlands

ARTICLE INFO

Keywords:
Hot-carrier injection
Recovery
Annealing
Passivation
Hydrogen

ABSTRACT

This article treats the recovery of hot-carrier degraded nMOSFETs by annealing in a nitrogen ambient. The recovery rate is investigated as a function of the annealing temperature, where the recovery for increasing temperatures is in agreement with the passivation processes. At the original post-metal anneal temperature of $T = 400$ °C, the device's original performance is fully restored. Higher temperatures induce a permanent, unrecoverable change to the devices, manifested in a gradual V_T shift. The recovery rate is found to be independent of both the transistor gate length and the cooling rate (quench, slow and stepped cooling) upon annealing. These findings are used to gain further understanding of the mechanisms behind the recovery of hot-carrier damage. The recovery rate exhibits Arrhenius behavior and the recovery data are consistent with Stesmans' recovery model.

1. Introduction

Several degradation mechanisms like hot-carrier injection (HCI) and bias temperature instability (BTI) arise when an electrical stress is applied to nMOSFET's. Charge trapping, defect formation in the gate oxide and at the interface play a role, although there is still some discussion to what degree [1]. There is however consensus that for both mechanisms hydrogen plays a pivotal role in the degradation and recovery of the devices [2]. Hydrogen may be released from Si-atoms at the interface and the so called P_b-centers, Si-atoms at the interface with a dangling bond, may be created. The defects can act as a charge trap, which can result in a shift of the threshold voltage, ΔV_T.

Less is known about the recovery, however it is assumed that during recovery, hydrogen atoms in the vicinity of the interface may repassivate the P_b-centers [2]. The hydrogen density at the interface is related to the concentration and diffusion of hydrogen species (H, H^+, H_2) in the gate stack. The diffusion rate in Si and SiO_2 is known to be different [3], suggesting that the materials in the immediate vicinity of the defective interface matter for recovery. Furthermore, both bias [4] and temperature [5] affect the recovery rate of the devices.

It is reported that the gettering of hydrogen atoms at grain boundaries in poly-Si films depends on the cooling rate and not on the anneal time itself [6]. A slower cooling rate will getter hydrogen from a bigger area due to a longer diffusion length. This raises the question if the repassivation rate and thus ΔV_T can be affected by varying the gate length of the devices and the cooling rate, schematically visualized in Fig. 1.

The motivation behind this work lies in the pursuit of self-healing transistors, see *e.g.* [7] and [8]. To investigate the properties of the recovery mechanism, the spontaneous recovery in a nitrogen ambient is investigated as a function of the temperature, the gate length and cooling rate. It is expected that V_T and the subthreshold swing will decrease and g_m, $I_{d,lin}$ will increase during recovery.

2. Experimental

2.1. Temperature dependence

The devices under study were long-channel nMOSFETs with a gate width of $W = 10.0$ µm, a gate length varying between $L = 0.6$ µm and $L = 10.0$ µm and a gate oxide thickness of $t_{ox} = 4.5$ nm. Annealing was done die for die, where each die contained nMOSFETs of all the gate lengths. Since the slow, long-term degradation and recovery of HCD were investigated, measurements were done using the measure-stress-measure (MSM) method. The threshold voltage of the pre-stress measurement is used as reference for maximum passivation and a reference for further measurements. Measurements were performed with a Keithley 4200-SCS and four Keithley 4200-PA Remote PreAmps for the source, drain, gate and bulk contacts. For the V_T-extraction, the drain bias was kept at $V_{ds} = 0.1$ V and the gate voltage was swept from $V_{gs} = -1$ V to $V_{gs} = 3$ V in steps of 25 mV at $T = 25$ °C. Using the extrapolation in the linear region (ELR) of the maximum transconductance, $g_{m,max}$, V_T was extracted [9]. The subthreshold swing, *SS*, is determined between $V_{gs} = 0.05$ V and $V_{gs} = 0.4$ V, $I_{d,lin}$ is determined

* Corresponding author.
E-mail address: m.j.dejong@utwente.nl (M.J. de Jong).

https://doi.org/10.1016/j.microrel.2018.07.057
Received 28 May 2018; Received in revised form 21 June 2018; Accepted 5 July 2018
Available online 30 September 2018
0026-2714/ © 2018 Elsevier Ltd. All rights reserved.

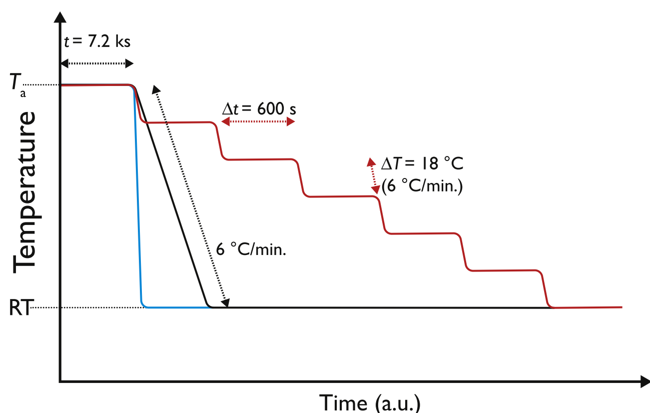


Fig. 1. Different types of cooling process, quench cooling (blue), slow cooling (black) and stepped cooling (red) from the annealing temperature (T_a) to room temperature (RT). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

at $V_{gs} = 2$ V.

During electrical stress, a constant voltage stress (CVS) was applied to the device at a temperature of $T = 25$ °C for a cumulative time of 3 ks if not otherwise specified, where two electrical measurements were performed per decade of stress time. The applied source-drain bias was kept at $V_{ds} = 4.5$ V and the source-gate bias was kept so that $|I_b|$ was maximum, which varied between $V_{gs} = 1.75$ V to $V_{gs} = 2.1$ V for the devices with a gate length of $L = 0.6$ μm to $L = 1.0$ μm. A source-drain bias of $V_{ds} = 6.5$ V and a source-gate bias of $V_{gs} = 1.7$ V was applied to the devices with a gate length of $L = 10.0$ μm. There was a delay of 1 s between the stress and measurement phase, to minimize short time-scale recovery components. The results are from one device and to minimize the variance, 15 measurements were done on the same device to determine the threshold voltage.

Positive bias temperature instability (PBTI) was measured on separate devices under identical conditions as for HCI, but with source and drain kept at ground. The threshold voltage was measured after 1 s delay, to investigate the long-term BTI contribution to ΔV_T under the HCI condition. No significant shift in the threshold voltage was measured after BTI stressing, indicating that it can be neglected for the devices that underwent HCI.

After electrical stress, the devices were annealed die for die in a nitrogen ambient (ramp rate: ~8 °C/min) according to Fig. 2 for 60 min. The bias on contacts of the device were kept floating during the anneal. After electrical measurements, the devices were annealed again in a nitrogen ambient for increasing higher temperatures (between $T = 100$ °C and $T = 540$ °C). After the anneal at $T = 500$ °C, an anneal at $T = 400$ °C and an anneal at $T = 350$ °C were done again, each followed by electrical measurements.

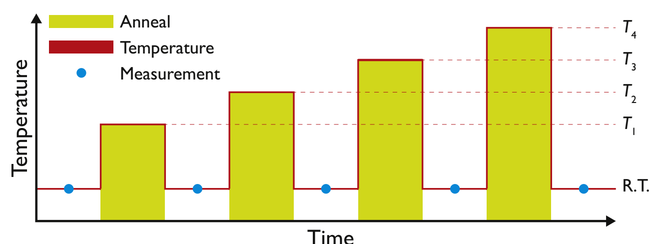


Fig. 2. The measurement process to investigate different anneal cycles of a single die. The blue dots represent the moment of the measurement, green represent the moments that the device is annealed and the corresponding temperature is given in red. Four anneal temperatures are given by T_1 to T_4. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

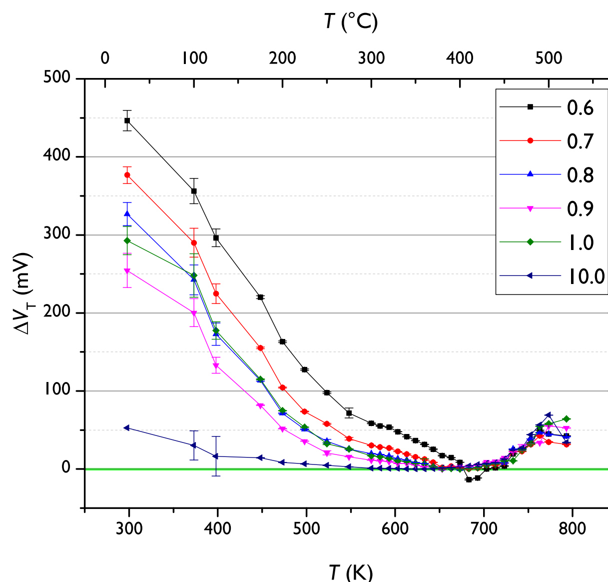


Fig. 3. The shift in the threshold voltage as a function of the applied thermal treatment. The devices have a width of $W = 10$ μm and the legend indicates L in μm. The electrical measurements were done at $T = 25$ °C.

The cooling rate dependency was investigated by stressing the devices for 3 ks. The quench cooling (the blue curve in Fig. 1) was done by removing the device from the furnace. The slow cooling (the black curve) had a cooling rate of 6 °C/min. The stepped cooling (the red curve) was done with steps of $\Delta T = 18$ °C, after which the temperature was kept constant for 10 min. This was done step by step to a temperature of $T \approx 110$ °C, where any extra recovery should be negligible [5].

3. Results and discussion

3.1. Anneal temperature dependence

Fig. 3 shows the recovery as a function of the applied temperature for devices exposed to electrical stress for 3 ks. As expected, a smaller gate length results in more degradation and thus a larger ΔV_T.

There is more recovery after annealing at a higher temperature. After an anneal at $T = 350$ °C to $T = 400$ °C, $\Delta V_T \approx 0$. This temperature coincides with the applied temperature during the post-metal anneal step and corresponds with the various values for total recovery reported by literature [5,10]. The data suggests that the device is completely recovered from the HCD. The devices with more degradation show a higher absolute recovery rate, although normalized to the maximum ΔV_T of each gate length, all devices show similar recovery.

After exposure to higher temperatures, $T > 450$ °C, V_T starts to increase. A temperature of $T \approx 400$ °C corresponds to a thermal energy higher than the bonding energy of Si−H bonds. This temperature range coincides with earlier reported values [6,11], suggesting that more P_b-centers at the Si/SiO_2-interface are introduced by the anneal. The ΔV_T is similar for all devices, suggesting that defects are introduced at the same rate/concentration, regardless of the gate length.

Due to thermal degradation, ΔV_T(500 °C) > 0 mV. It was checked if the devices could be repaired with an additional anneal at $T = 400$ °C and $T = 350$ °C in an nitrogen ambient (the temperature where total recovery took place). However, no significant shift in V_T was observed after the second anneal at the temperature where total recovery should take place, however these anneals show negligible effect on ΔV_T. After HCD, sufficient hydrogen atoms were present to accommodate repassivation of P_b-centers. It is reported for some time that at higher temperatures, out diffusion of hydrogen into vacuum can take

Microelectronics Reliability 88–90 (2018) 147–151

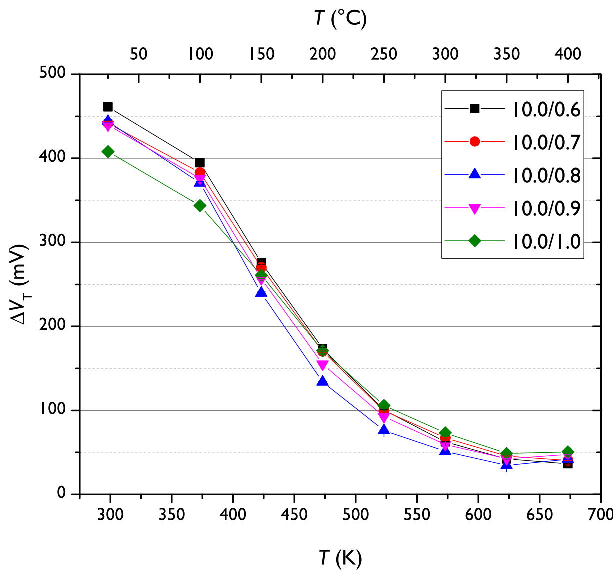


Fig. 4. Recovery of ΔV_T as a function of the applied thermal treatment. The electrical measurements were done at T = 25 °C. The legend indicates W/L in μm/μm.

place [11]. This raises the question if this happens for hydrogen in the device in a nitrogen ambient and subsequently decrease the hydrogen density. Perhaps insufficient hydrogen atoms were present for the re-passivation process after thermal degradation at T = 500 °C.

3.2. Gate length dependence

Devices of various gate lengths, stressed to roughly the same ΔV_T were annealed. The results are shown in Fig. 4. The figure suggests similar recovery behavior in terms of ΔV_T, regardless of the gate length.

The recovery of Δg_m is shown in Fig. 5 for the same experiment as reported in Fig. 4. The shift is larger for smaller devices, if the same ΔV_T is induced. The relative recovery of Δg_m is shown in the plot, where a percentage of 100% indicates the maximum degradation directly after electrical stress. A negative recovery means that g_m becomes higher than the pre-stress value. Overall, there is no significant gate length dependency for the recovery during an anneal up to a temperatures of

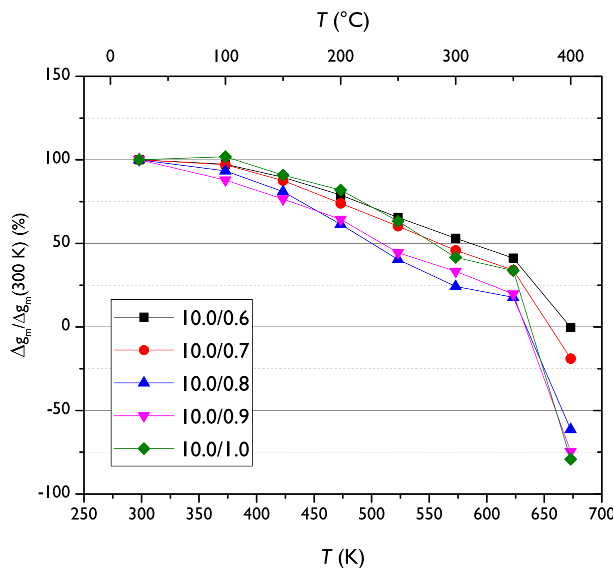


Fig. 5. Relative recovery of Δg_m. The electrical measurements were done at T = 25 °C. The legend indicates W/L in μm/μm.

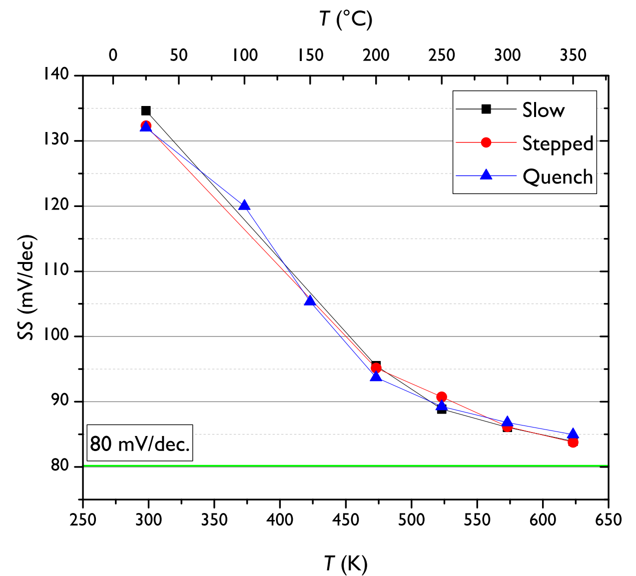


Fig. 6. Recovery of SS of the devices with W/L = 10.0/0.6 in μm as a function of the temperature of the thermal treatment. The legend indicates the cooling rate. The subthreshold swing was measured between V_{gs} = 0.05 V and V_{gs} = 0.45 V at T = 25 °C. The green line indicates the value of the fresh device (~80 mV/dec). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

T = 350 °C when the degraded devices have the same shift in the threshold voltage.

3.3. Cooling rate dependence

Devices of various gate lengths have been exposed to electrical stress for 3 ks. The effect of the cooling rate (see Fig. 1) on the recovery has been investigated. Fig. 6 shows the recovery of SS and Fig. 7 shows the recovery of $I_{d,lin}$ as a function of the annealing temperature. Similar recovery behavior of SS and $I_{d,lin}$ are seen for all experiments.

A change in the number of interface defects, N_{it}, oxide defects and fixed charge in the oxide have an influence on SS, V_T and g_m. Fig. 8 shows ΔSS as a function of ΔV_T. The slope between ΔV_T and ΔSS can be

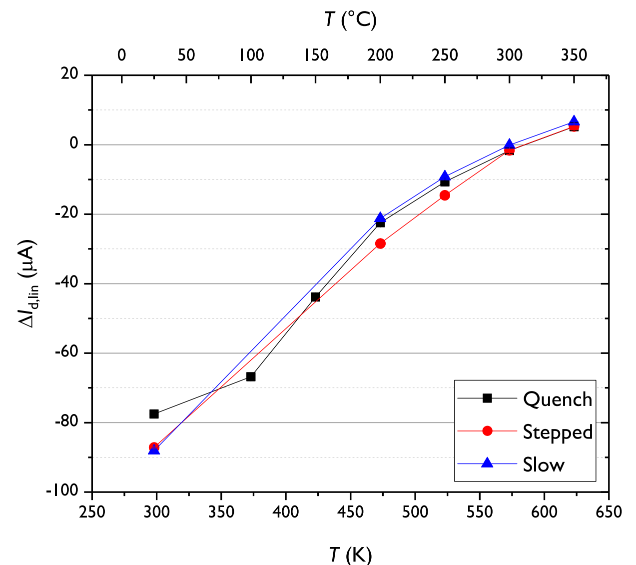


Fig. 7. Recovery of $\Delta I_{d,lin}$ of the devices with W/L = 10.0/0.6 in μm as a function of the temperature of the thermal treatment. The legend indicates the cooling rate. The drain current was measured at V_{gs} = 2 V at T = 25 °C.

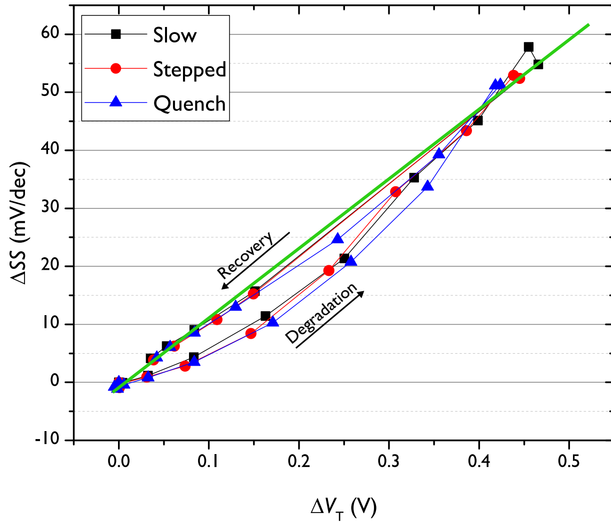


Fig. 8. Correlation between ΔSS and ΔV_T of the devices with $W/L = 10.0/0.6$ in μm. The legend indicates the cooling rate. The subthreshold swing was measured between $V_{gs} = 0.05$ V and $V_{gs} = 0.4$ V at $T = 25$ °C. The green line is a guide to the eye to indicate a proportional recovery rate for V_T and SS. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

used to indicate if the proportion of the degradation and recovery contributed to interface defects [12] will change. The green line is a guide to the eye, indicating a constant proportion of the degradation contributed to ΔN_{it}. During degradation, V_T and SS do not change proportionally at the same rate for different stress times. This is in contrast to an earlier report [12]. The recovery phase does follow the proportionality line until almost complete recovery is achieved for increasing higher temperatures. This suggests that interface defects are removed proportionally with the same rate during the anneal step.

The correlation between the maximum transconductance and the threshold voltage is given in Fig. 9. It would be expected that after annealing, the induced recovery will follow the line of degradation. The data suggests that this is not the case, since V_T seems to recover with a higher rate than g_m at the lower anneal temperatures. Furthermore, in contrast with Fig. 8, an S-curve is observed instead of a linear behavior. An explanation does not fall within the scope of this paper, however this behavior is observed for $I_{d,lin}$ too and for all cooling rates. A more

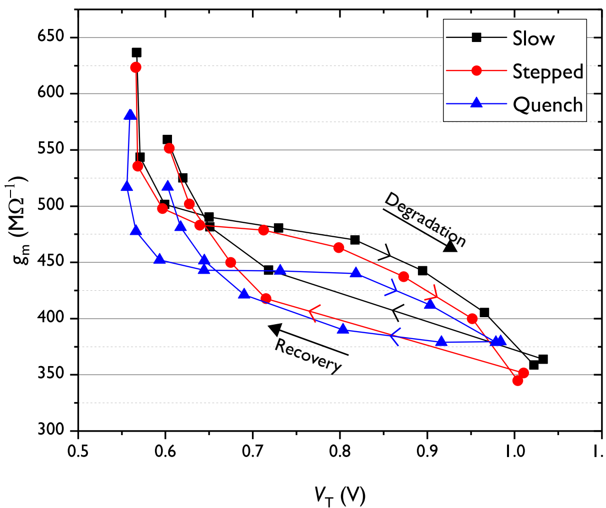


Fig. 9. Correlation between $g_{m,max}$ and V_T of the devices with $W/L = 10.0/0.6$ in μm. The legend indicates the cooling rate. The measurements of g_m and V_T were performed at $T = 25$ °C.

profound S-curve was observed for a smaller gate length. The S-curve was observed during an earlier experiment [13].

The devices show no significant difference in recovery as a function of the cooling rate. This suggests that the same amount of hydrogen can be gettered at the interface under the conditions of the experiment, regardless of the cooling rate. Based on the earlier findings of Shika et al. [6], one may expect that the hydrogen passivation exhibits a clear cooling rate dependency. Here no such dependence was found. The difference may be attributed to a different physical situation, in particular the annealing ambient and the difference between poly-silicon grain boundaries and the Si/SiO_2-interface.

The recovery of the degraded devices may follow an exponential time dependency of the form of Eq. (1).

$$V_T = V_{T0} + \Delta V_T \cdot \exp\ (-t/\tau) \tag{1}$$

Here is V_{T0} the threshold voltage of the unstressed device and τ some parameter that depends, among others, on the annealing temperature. The devices have been annealed for 7200 s at various annealing temperatures. The same devices are annealed at increasing higher temperatures, and although cumulative annealing effects may play a role, here is assumed that the effect of the anneal at the highest temperatures has the biggest effect on the recovery. Fig. 10 shows τ as a function of the annealing temperature. The data is consistent with an Arrhenius dependency between $1/\tau$ and $1/kT$ (see linear relation of the inset of Fig. 10). A higher temperature will result in a lower recovery time. There are several models to describe the recovery by passivation of P_b-centers at the $Si\text{-}SiO_2$-interface, in line of or an extension to Eq. (1).

The model of Stesmans [14], in line with [5], assumes that the energy to passivate the dangling bonds is normally distributed due to the different configurations of interface defects. The ratio between the unpassivated interface defects ($[P_b]$) and the maximum number of interface defects (N_0) can be described by Eq. (2), which can be used to fit the data of Fig. 3. Here is assumed that since $\Delta V_T \propto \Delta N_{it}$ and $\Delta N_{it} \gg N_{unstressed} \rightarrow N_0 \approx \Delta N_{it}$.

$$\frac{[P_b]}{N_0} = \frac{1}{\sqrt{2\pi}\sigma_{E_f}} \int_{E_f-3\sigma_{E_f}}^{E_f+3\sigma_{E_f}} \exp\left(-\frac{(\epsilon-E_f)^2}{2\sigma_{E_f}^2}\right) \times \exp\left(-k_{f,0}[H_2]t_{bake}\exp\left(-\frac{\epsilon}{kT}\right)\right)d\epsilon \tag{2}$$

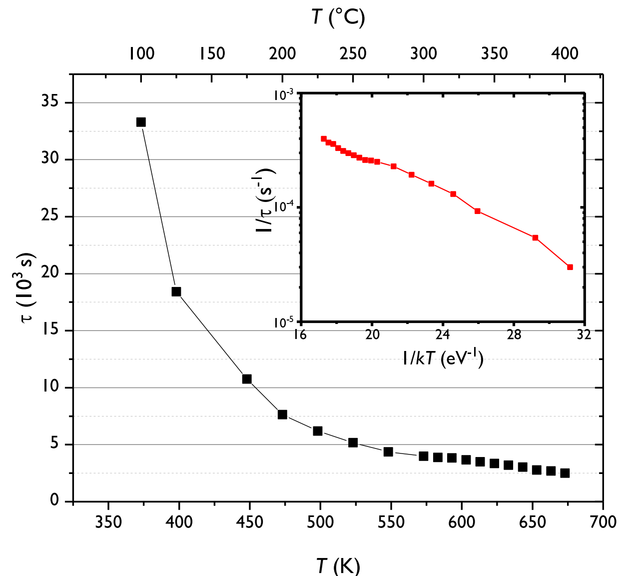


Fig. 10. Recovery constant τ as a function of the annealing temperature of the devices with $W/L = 10.0/0.6$ in μm. The inset shows $1/\tau$ as a function of $1/kT$.

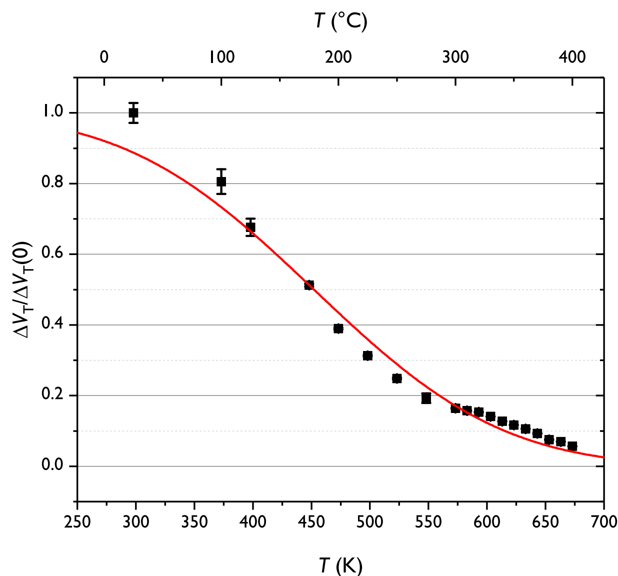


Fig. 11. The data of Fig. 3 fitted by the passivation model of Stesmans [14].

Here $[H_2]$ is the volume concentration of molecular hydrogen in SiO_2 ($\approx 10^{18}$ cm^{-3}) [15]. Assumed is that at lower temperatures the concentration does not change and the out-diffusion of hydrogen will only start to arise at higher temperatures. E_f is the passivation energy, σ_{E_f} the standard deviation of the passivation energy, $k_{f,0}$ is the rate constant and t_{bake} the anneal temperature ($t_{bake} = 7200$ s). Solving Eq. (2) under the previously mentioned assumptions using the least-squares method, an $E_f = 1.39$ eV, $\sigma_{E_f} = 0.369$ eV and $k_{f,0} = 2 \cdot 10^{-7}$ cm^3/s are found, resulting in the fit of Fig. 11. It is expected that no perfect match will be observed, because some assumptions, like those for the concentration $[H_2]$ or $N_{unstressed}$, may be less valid or change for different temperatures. Although the values are somewhat different than previously reported values [5,14], the model of Stesmans is consistent with the data of the relative ΔV_T-recovery.

4. Conclusions

Several recovery experiments have been performed on long channel nMOSFETs exposed to hot-carrier injection. The devices were annealed in a nitrogen ambient and investigated for varying temperatures, gate lengths and cooling rates. Up to a temperature of $T = 400$ °C, V_T, g_m, $I_{d,lin}$ and *SS* recover to their initial values. Exposure at higher temperatures increases V_T again. The shift due to thermal degradation is not recoverable by annealing at a lower temperature. The temperature coincides with a thermal energy higher than the binding energy of Si—H bonds at the Si/SiO_2-interface, suggesting that for higher temperatures the Si—H bonds begin to dissociate and hydrogen to diffuse out of the device into the ambient. The recovery was similar for devices of varying gate length if the same shift in threshold voltage was applied and for different cooling rates (quench, slow and stepped cooling). The recovery data was consistent with models from literature and the passivation energy seemed to be normally distributed.

The data suggests that under the experimental conditions in hot-carrier degraded devices, sufficient hydrogen is present and can reach the Si/SiO_2-interface for recovery. Further no significant improvements in recovery rate can be achieved with the same temperature, but different cooling rates. In conclusion, the first steps are taken to get a more comprehensive picture and better understanding of the hydrogen-related recovery process in degraded MOSFETs.

References

[1] J.H. Stathis, S. Mahapatra, T. Grasser, Controversial issues in negative bias temperature instability, Microelectron. Reliab. 81 (2018) 244–251.
[2] S. Mahapatra, D. Saha, D. Varghese, P.B. Kumar, On the generation and recovery of interface traps in MOSFETs subjected to NBTI, FN, and HCI stress, IEEE Trans. Electron Devices 53 (7) (2006) 1583–1592.
[3] D.L. Griscom, Diffusion of radiolytic molecular hydrogen as a mechanism for the postirradiation buildup of interface states in SiO_2-on-Si structures, J. Appl. Phys. 58 (7) (1985) 2524–2533.
[4] Lars-Åke Ragnarsson, Per Lundgren, Electrical characterization of Pb centers in (100)Si-SiO_2 structures: the influence of surface potential on passivation during post metallization anneal, J. Appl. Phys. 88 (2) (2000) 938–942.
[5] G. Pobegen, Recovery From Hot Carrier Induced Degradation Through Temperature Treatment, Springer International Publishing, Cham, 2015, pp. 221–230.
[6] Y. Shika, T. Bessho, Y. Okabe, H. Ogata, S. Kamo, K. Kitahara, A. Hara, Impact of the hydrogenation process on the performance of self-aligned metal double-gate low-temperature polycrystalline-silicon thin-film transistors, Jpn. J. Appl. Phys. 52 (3S) (2013) 03BB01.
[7] J. Schmitz, Self-healing in semiconductors, Future Trends in Microelectronics, 2015 Mallorca, Spain.
[8] H.T. Lue, P.Y. Du, C.P. Chen, W.C. Chen, C.C. Hsieh, Y.H. Hsiao, Y.H. Shih, C.Y. Lu, Radically extending the cycling endurance of flash memory (to 100M cycles) by using built-in thermal annealing to self-heal the stress-induced damage, vol., (Dec. 2012) 9.1.1–9.1.4.
[9] A. Ortiz-Conde, F.J. García Sánchez, J.J. Liou, A. Cerdeira, M. Estrada, Y. Yue, A review of recent MOSFET threshold voltage extraction methods, Microelectron. Reliab. 42 (4) (2002) 583–596.
[10] Anastasios A. Katsetos, Negative bias temperature instability (NBTI) recovery with bake, Microelectron. Reliab. 48 (10) (2008) 1655–1659.
[11] J.H. Stathis, Dissociation kinetics of hydrogen-passivated (100) Si/SiO_2 interface defects, J. Appl. Phys. 77 (12) (1995) 6205–6207.
[12] Z. Yu, S. Guo, R. Wang, P. Hao, R. Huang, New observations on the two-stage degradation of hot carrier reliability in high-k/metal-gate MOSFETs, 2017 IEEE 24th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), vol., July 2017, pp. 1–4.
[13] M.J. de Jong, C. Salm, J. Schmitz, Observations on the recovery of hot carrier degradation of hydrogen/deuterium passivated nMOSFETs, Microelectron. Reliab. 76–77 (2017) 136–140.
[14] A. Stesmans, Passivation of P_{b0} and P_{b1} interface defects in thermal (100) Si/SiO_2 with molecular hydrogen, Appl. Phys. Lett. 68 (15) (1996) 2076–2078.
[15] J.E. Shelby, Molecular diffusion and solubility of hydrogen isotopes in vitreous silica, J. Appl. Phys. 48 (8) (1977) 3387–3394.