Brief Papers

A Robust 43-GHz VCO in CMOS for OC-768 SONET Applications

Arnoud P. van der Wel, *Student Member, IEEE*, Sander L. J. Gierkink, Robert C. Frye, Vito Boccuzzi, *Member, IEEE*, and Bram Nauta, *Senior Member, IEEE*

***Abstract*—In this paper, we present a 43-GHz LC-VCO in 0.13-μm CMOS for use in SONET OC-768 optical networks. A tuned output buffer is used to provide 1.3 V_{p-p} (single-ended) into a 90-fF capacitive load as is required when the VCO is used in typical clock and data recovery (CDR) circuits. Phase noise is -90 dBc/Hz at a 1-MHz offset from the carrier; this meets SONET jitter specifications. The design has a tune range of 4.2%. The VCO, including output buffers, consumes 14 mA from a 1-V supply and occupies 0.06 mm^2 of die area. Modern CMOS process characteristics and the high center frequency of this design mean that the tank loss is not dominated by the integrated inductor, but rather by the tank capacitance. An area-efficient inductor design that does not require any optimization is used.**

***Index Terms*—CMOS, OC-768, SONET, voltage-controlled oscillator.**

I. Motivation

AT PRESENT, circuits for 40-GB/s optical communication networks are commonly made using III-V compounds or in SiGe processes [1]. With the advent of smaller and faster CMOS technology, it has become possible to make such circuits in standard CMOS, leading to lower cost solutions and opening the way to increased integration. One of the principal functions that is required in optical networks is that of clock and data recovery (CDR). For this, a voltage-controlled oscillator (VCO) is a central building block. Several authors have presented 40+ GHz VCOs in CMOS [2], [3], but application of a VCO to a real CDR circuit requires that the VCO should be capable of driving a capacitive load with a large voltage swing. This presents challenges in terms of phase noise. An architecture with a tuned output buffer is presented that satisfies the drive requirements and has a 4% tune range. The design is low power (14 mW), low voltage (1 V), and occupies a very small die area (0.06 mm^2).

II. Specifications

A. Jitter Requirements

In OC-768 optical networks, the specified bitrate is 39.81 GHz. Eight percent forward error correction (FEC) is commonly used; this makes for a "raw" bitrate of 43 GHz, which is the design center frequency of this VCO. A single bit time (commonly referred to as a unit interval or UI) at this data rate is 23.3 ps. ITU requirements [4] specify the maximum allowable jitter, whereas for VCOs, the measured quantity is the phase noise spectrum. Conversion between jitter and phase noise is straightforward:

$$\Delta\phi^2_{\mathrm{RMS}} = \int_{\mathrm{band}} 2 \cdot \mathcal{L}(f) df \tag{1}$$

where $\mathcal{L}(f)$ is the phase noise spectrum, band is the offset frequency band of interest, and $\Delta\phi_{\mathrm{RMS}}$ is the RMS jitter in radians [5].

ITU requirements state that jitter in a band from 16 to 320 MHz should not be more than 0.1 UI_{p-p}. This requirement does not translate directly to VCO specifications: it dictates the behavior of the whole CDR subsystem and it is up to the designer of the subsystem to divide the jitter "budget" in an optimal fashion. If 25% of the jitter budget is expended on the VCO and $\mathcal{L}$ (1 MHz) is lower than -87 dBc/Hz, then the VCO is suitable for use in a SONET OC-768 CDR system. For a more complete treatment of this subject, see, for example, [1].

B. Output Drive Requirements

By examining the CDR circuit, the drive requirements of the VCO can be determined. Two types of CDR circuit are commonly used. These are the Hogge (linear) detector [6] and the Alexander (bang-bang) detector [7]. Though they differ in their operating principle, they do not place significantly different demands on the VCO. A realistic, useful output is if 90 fF (representing the input capacitance of a 70/0.13 n-channel MOSFET) can be driven by the VCO with more than 0.6 V_{p-p} (single-ended) over all anticipated temperature variations and process spread.

For both the Hogge and the Alexander CDR architectures, two active clock flanks are required per UI. This means that at 43 GB/s, we need a 43-GHz differential clock source or a 21.5-GHz quadrature clock source. Additional constraints such as power and area will decide which of these two is chosen. A 43-GHz differential clock is promising for its small die area and relative simplicity; quadrature generation is not required. Half-rate CDR systems (see, for example, [8]) halve the clock frequency requirement at the expense of slower locking performance.

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A. P. van der Wel and B. Nauta are with the IC Design Group, Faculty of EEMCS, Mesa+ Research Institute, University of Twente, 7500AE Enschede, The Netherlands (e-mail: a.p.vanderwel@utwente.nl).

S. L. J. Gierkink, R. C. Frye, and V. Boccuzzi are with the Wireless Circuits Research Group, Agere Systems, Allentown, PA 18109 USA.

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III. Oscillator Architecture and Design

A. Architecture

The high center frequency, fixed frequency application, and stringent phase noise requirements point to an *LC*-type oscillator. At 40 GHz, a benefit is that the required inductors are small so this often-cited disadvantage of integrated *LC* oscillators does not apply. Many fully integrated *LC* oscillators at lower frequencies have been presented, and much design effort has been put into the design of a high quality-factor (Q) inductor. For a given power consumption, low phase noise dictates the use of a high-Q tank. For the *LC*-tank

$$\frac{1}{Q_{\rm tank}} = \frac{1}{Q_L} + \frac{1}{Q_C} \tag{2}$$

where $Q_{\rm tank}$, Q_L, and Q_C are the quality factors of the tank, and the inductor and capacitor that make up the tank, respectively. If Q_L is much lower than Q_C, as is commonly the case for integrated *LC*-tanks at frequencies up to a few gigahertz, improving Q_L directly leads to a higher tank Q, and hence, to lower phase noise at given power [9]. With the advent of modern CMOS processes with copper metallization, a "low-k" interconnect dielectric and eight or more metal layers (all contributing to reduced inductor losses), Q_C at 40 GHz is significantly lower than Q_L, and improving the latter is no longer necessary. Rather, design effort needs to be put into making Q_C as high as possible.

An output buffer is required because of the large $C_{\rm load}$ that needs to be driven. Absorbing it directly into the VCO tank would unacceptably lower tank Q, since $C_{\rm load}$ is the input capacitance of a MOSFET, which is lossy due to the gate series resistance. Moreover, absorbing $C_{\rm load}$ into the VCO tank would mean that changes in $C_{\rm load}$ (e.g., due to wiring) would influence the operation of the VCO core, which is not desirable. We use a tuned output buffer into which $C_{\rm load}$ is absorbed.

B. Design

The central part of the tuned oscillator is the *LC*-tank. Since the oscillation frequency ($\omega_0 = 1/\sqrt{LC}$) dictates the product of L and C, the only design freedom is in choosing the tank impedance Z_0:

$$Z_0 = \sqrt{\frac{L}{C}}. \tag{3}$$

Commonly, constraints such as startup gain, required oscillation amplitude, and tune range dictate the selection of Z_0 [10], while $Q_{\rm tank}$ is not significantly impacted. Here, however, tank losses are dominated by $C_{\rm tank}$, and this opens the possibility of reducing tank losses by lowering Z_0. A significant part of $C_{\rm tank}$ is parasitics (these have a low Q and sum to approximately 100 fF), so by adding high-Q metal–insulator–metal (MIM)[1] capacitance, Q_C will rise. This is illustrated by

$$\frac{1}{Q_C} = \sum_n \frac{1}{Q_n \cdot \left(\frac{C}{C_n}\right)} \tag{4}$$

[1]MIM capacitance consists of a thin dielectric between metal layers 7 and 8 with $Q \approx 35$ at 40 GHz.

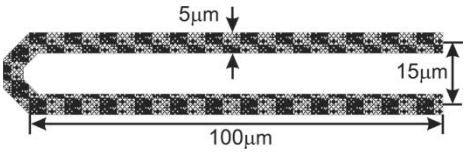

Fig. 1. Scalable inductor layout does not require optimization of Q.

in which C is the parallel combination of several smaller C_n's, each with a quality factor Q_n, and Q_C is the quality factor of the parallel combination.

Now, taking into account not only required startup gain, tune range, and voltage swing, but also $Q_{\rm tank}$, we may select Z_0. In this case, all requirements are met using $Z_0 = 25\,\Omega$. This means a tank capacitance of 150 fF with a Q of approximately 10.

1) Inductor Design: An important component of the tank is the inductor. The availability of copper metallization (standard in modern CMOS processes) and operation at 40 GHz means it is not necessary to tie several metal layers together for a low series resistance. Hence, a single turn on the top metal layer is used. Inductor Q is very high at 40 GHz, so measures to maximize it are not required. For example, a patterned ground shield is not used because all inductor losses (including substrate losses) are low compared to losses in the $C_{\rm tank}$. Fig. 3 shows the equivalent circuit model of the inductor. Parasitic capacitances are so small that their low Q does not significantly impact the Q of $C_{\rm tank}$, into which they are absorbed. Also, we can freely change the shape of the inductor to suit layout requirements and minimize die area rather than using the common round or octagonal shapes that maximize Q. A long and thin rectangular shape is chosen because it allows very compact layout of the VCO (core and output buffer) and because it is easily scaled to other inductance values. The inductor layout is shown in Fig. 1.

Though it is not necessary to maximize inductor Q in this case, it *is* necessary to accurately characterize the inductor. To this end, the inductor layout is simulated using IES^3 [11], which offers efficient 2.5D electromagnetic (EM) simulation. To ensure accurate modeling of skin effect, which we expect to be significant at 40 GHz, special care is taken when meshing the inductor prior to simulation: the single thick copper layer forming the inductor is broken up into three layers, and a very fine mesh is applied around all edges of the inductor. This is illustrated in Fig. 2 where the mesh on one leg of the inductor is shown.

EM simulation produces a y-parameter matrix to which a circuit model fit is made. This circuit model (Fig. 3) can then be used in the circuit simulator. Two lossy capacitors model substrate loss; while two coupled inductive branches model the inductor itself. In this way, the model incorporates a first-order approximation of the skin effect: the branch with the high inductance and high series resistance represents the "center" part of the copper trace and models inductor behavior at low frequencies, while the branch with low inductance and low series resistance represents the "outer" part of the copper trace and models inductor behavior at high frequencies. At 40 GHz, the "outer" part of the copper trace dominates, giving an effective inductance of 83 pH and a Q of 35.

2) Circuit Topology: The circuit diagram of the oscillator is shown in Fig. 4. For brevity, the inductor is shown as an ideal

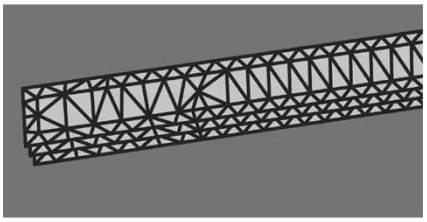

Fig. 2. Careful meshing prior to EM simulation ensures accurate modeling of skin effect.

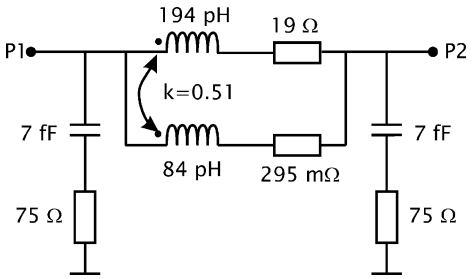

Fig. 3. Circuit model of inductor.

83 pH inductor. In actual simulations, the full equivalent circuit model of the inductor is used.

The VCO gain cell is equipped with nMOS transistors. The transistors used have a fingered structure with fingers of 2-μm width each. Tuning is done with two pMOS accumulation-mode varactors that have two fingers of 0.4×2.4 μm each; the gate terminal is connected to the tank and the bulk terminal is connected to $V_{\rm tune}$, which is continuous from 0 to 1 V. The oscillator is biased with a current source from the positive supply, for better immunity to supply voltage variations, and to allow direct coupling to the output buffer stage.

The output buffer consists of an n-channel transistor with a tuned drain load for which the inductor layout is reused. The small dimensions of the inductor mean that this does not add significantly to the size of the circuit. The tuned load enables us to achieve a peak-to-peak output voltage swing of 1.3 V (single-ended, typically) into 90 fF, which is larger than the 1-V supply voltage. Both the in-phase and the antiphase output of the VCO achieve this swing. Since the peak output voltage of the buffer is higher than the supply voltage, a cascode transistor with the gate connected to the supply is included to prevent any detrimental effects on reliability. In this way, no gate oxide anywhere in the output buffer is subjected to more than the 1-V supply voltage. Only the (reverse-biased) drain–bulk junction of the cascode transistor is subjected to a peak voltage of around 1.5 $V_{\rm dd}$, but this does not pose reliability problems. The large signal voltage gain of the output buffer is approximately 1, its principal function being a reduction of the capacitive loading of the VCO core. The output of the buffer is capacitively coupled to the load using an interdigitated capacitor, and the DC level at the output is placed at half the supply voltage using a high-impedance resistive divider. The load still needs to be absorbed into the output buffer tank to bring it to resonance at the correct frequency but this is no longer critical, as the only thing influenced is the output amplitude, not the center frequency or the phase noise. We see that the application of integrated tuned buffers becomes practical at frequencies of 40 GHz and above because of the small physical size and high Q of the required inductors.

A startup gain of two is chosen to ensure reliable startup of the VCO. An even lower startup gain could reduce parasitics, thereby improving Q_C, $Q_{\rm tank}$, and the phase noise performance, but for the prototype, robust startup behavior was deemed preferable.

IV. Experimental Results

For testing purposes, a special version[2] of the VCO was made to drive 50 Ω. It was processed in a 0.13-μm standard CMOS process with one poly and eight metal layers. Metallization is copper, and the top metal layer is especially thick (3 μm). The interconnect dielectric is low-k; $\epsilon_r = 3$. The process features an MIM capacitance between M7 and M8 that has a capacitance of approximately 1 fF/μm^2 and a low series resistance. The substrate is lightly doped p-Si with a resistivity of 10 $\Omega \cdot$ cm.

To drive 50 Ω, the VCO core is not changed, so representative measurements of the phase noise are possible. Output voltage is lower, and the purpose of the tuned output buffer is somewhat defeated when driving a low-impedance load. Nevertheless, this test version exhibits performance in excellent agreement with simulations, lending credence to the expectation that the original version will perform according to simulation results as well.

The VCO is tested by wafer probing. Supply current is 14 mA at 1 V, of which 7 mA is drawn by the VCO core and 7 mA by the output buffer. To reduce capacitive coupling to the substrate, the output bondpads consist of only the top three metal layers. The output is measured using an Agilent 8565 EC spectrum analyzer. At 40 GHz, a double terminated line is preferred for connecting the VCO to the analyzer, so a 50-Ω shunt resistor is included on the chip. This means that the output buffer sees 25 Ω. Output power is essentially constant over tune range at −24 dBm. Simulated output power for this version is −15.5 dBm, while cable and connector loss are measured as 4.5 dB at 40 GHz, and probe/bondpad loss is estimated at 1 dB. Measured output power is, therefore, approximately 3 dB below simulated output power.

The tuning characteristic is shown in Fig. 5. Though the C–V curve of the varactor is nonlinear, the large voltage swing in the VCO core tends to linearize the tuning characteristic [12] and the resulting tuning curve is quite linear.

The noise sidebands are measured with the spectrum analyzer. With the aid of a specialized program, Δf^{-3} and Δf^{-2} fits are made on the phase noise spectrum (Fig. 6). This allows us to clearly identify the different parts of the phase noise spectrum: a Δf^{-3} (−30 dB/decade) characteristic due to $1/f$ noise of the active devices for offset frequencies up to 2 MHz, and a Δf^{-2} (−20 dB/decade) characteristic due to thermal noise for larger offset frequencies.

Measured phase noise is essentially constant over tune range. At 1 MHz (in the −30 dB/dec range) it is −90 dBc/Hz and at and at 4-MHz offset (in the −20 dB/dec range) it is −105 dBc/Hz. From measuring 19 samples on half a wafer, we find a center frequency spread (1 σ) of 1.9% (0.78 GHz). This indicates that to compensate for wafer-to-wafer and

[2]At the time of design, ITU specs were still for 7% FEC so the design center frequency of this version is 42.6 GHz rather than 43 GHz.

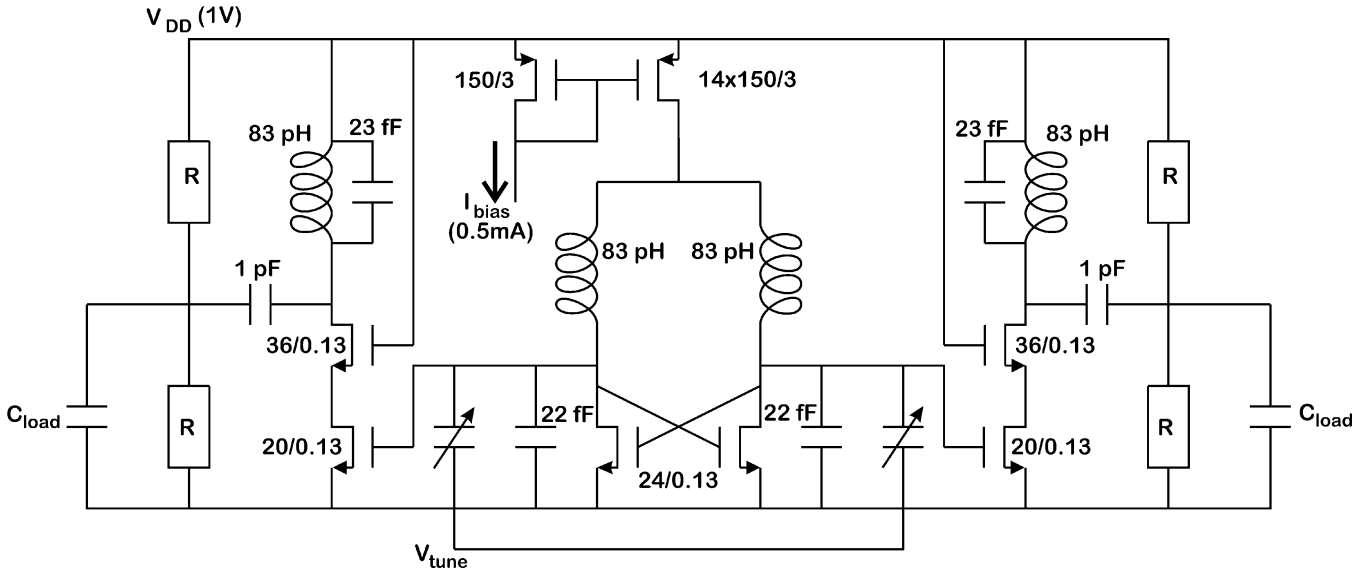

Fig. 4. VCO with tuned output buffer.

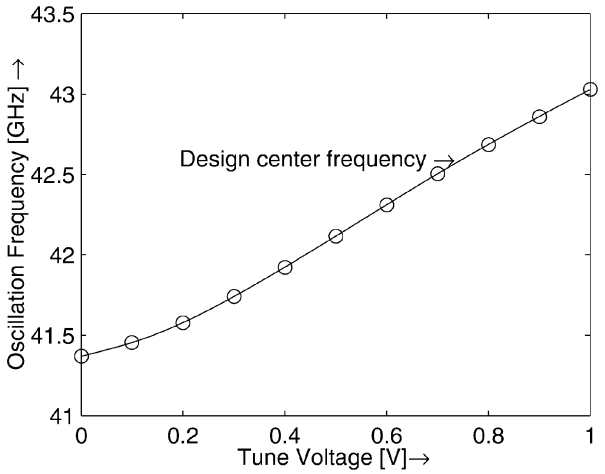

Fig. 5. Tune range.

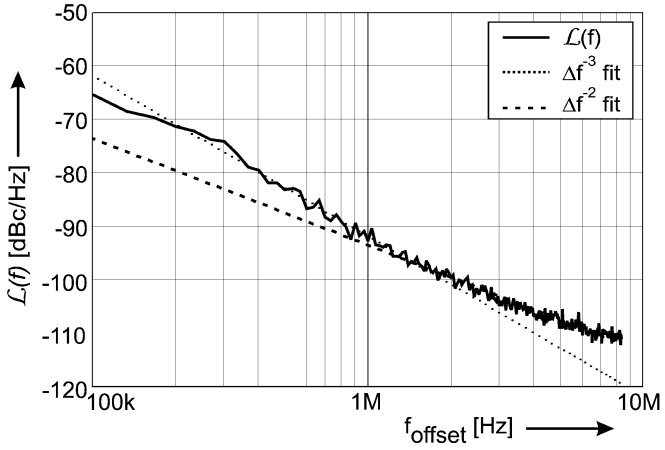

Fig. 6. Different contributions to the phase noise spectrum.

batch-to-batch spread, a larger tune range than the 4% of the current prototype will be required. A die photograph is shown in Fig. 7. The distinctive inductor shape is clearly visible, twice at the top (the VCO core) and twice below that (the tuned

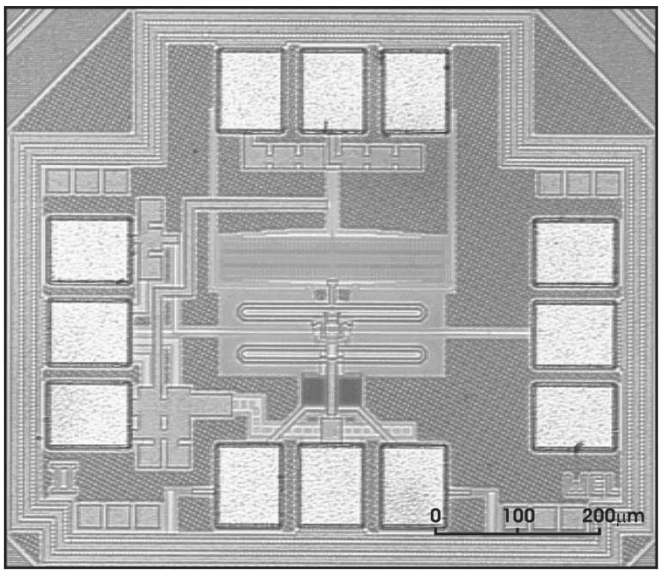

Fig. 7. Die photo.

output buffer). To satisfy minimum metal density requirements, a fillpattern is generated in the unused areas of the die. This fillpattern is kept well clear of the inductors to preclude any influence on their properties.

V. Summary and Conclusion

A 43-GHz LC-VCO in 0.13-μm standard CMOS is presented. The 43-GHz center frequency, along with the properties of modern CMOS processes mean tank loss is dominated by the tank capacitance $C_{\rm tank}$ rather than the the tank inductance $L_{\rm tank}$. Rigorous maximization of Q_L is not required and design effort is focused on maximizing Q_C. Since a significant part of the $C_{\rm tank}$ consists of low-Q parasitics, lowering the tank impedance Z_0 (increasing $C_{\rm tank}$ while decreasing $L_{\rm tank}$) makes Q_C higher. The VCO has a tune range of 4.2%, and has both in-phase and antiphase outputs that each have a peak-to-peak output voltage swing larger than the supply

voltage. The output voltage (simulated: 1.3 V_{p-p} (typ.) into 90 fF; measured: -18.5 dBm into 25 Ω) makes the VCO capable of driving high-speed digital logic. Phase noise is -90 dBc/Hz at a 1-MHz offset and supply current is 14 mA from a 1-V supply, of which 7 mA is drawn by the VCO core. The VCO occupies 220×270 μm of die area. The low phase noise and high output drive capability make the VCO suitable for CDR circuits in OC-768 optical networks. The inductor used shows promise for circuits beyond 40 GHz, as we have shown that a high Q can easily be attained without optimization and without occupying a large die area.

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