Size Dependence of the Magnetic and Electrical Properties of the Spin-Valve Transistor

Sungdong Kim, O. M. J. van't Erve, R. Vlutters, R. Jansen, and J. C. Lodder, *Member, IEEE*

***Abstract*—The electrical and magnetic properties of the spin-valve transistor (SVT) are investigated as a function of transistor size. A new fabrication process, designed to study the size dependence of the SVT properties, uses: silicon-on-insulator (SOI) wafers, a combination of ion beam and wet etching and a negative tone photoresist (SU8) as an insulating layer. The Si/Pt emitter and Si/Au collector Schottky barrier height do not depend on the transistor dimensions. The parasitic leakage current of the Si/Au collector is, however, proportional to its area. The relative collector current change with magnetic field is 240%, independent of size, while the transfer ratio starts to decrease for SVTs with an emitter area below $25 \times 25\ \mu m^2$. The maximum input current is found to be limited by the maximum current density allowed in the base (1.7×10^7 A/cm^2), which is in agreement with the maximum current density for spin valves.**

***Index Terms*—Hot electron, magnetic devices, reliability, Schottky diodes, spin-valve transistor.**

I. Introduction

THE spin-valve transistor (SVT) [1], [2], is a spin-electronic device that utilizes hot electrons and spin-dependent transport. In the emerging field of spintronics or magnetoelectronics, in which electron spin rather than charge is used [3], the SVT is used as an aid to study spin transport phenomena of hot electrons. The SVT also shows a huge magnetic response of more than 200% at room temperature in small magnetic fields [4]. Therefore, practical applications such as magnetic field sensors or memory elements in a magnetic random access memory (MRAM) are currently being explored.

The SVT is a ferromagnet-semiconductor hybrid structure analogous to a metal base transistor (MBT) where the metal base contains a metallic spin valve. The transistor used here has an n-type Si(100) emitter and collector and a Pt/$Ni_{80}Fe_{20}$/Au/Co/Au base layer. When the Si/Pt emitter Schottky diode is forward biased, electrons are injected into the base layer with an excess energy around 0.9 eV. While these hot electrons traverse the base layer they undergo scattering, which is dependent on the magnetization of the magnetic layers in the spin-valve base. Those electrons that reach the collector with the right momentum and a high enough energy will be able to surpass the collector energy barrier and make up the collector current. The rest of the electrons are reflected at this energy barrier and flow back as the base current. Note that both MBTs and SVTs generally show no amplification, however, this is not required for typical spin-electronic applications such as sensors and MRAM elements.

So far, SVTs have been studied with an emitter size of $350 \times 350\ \mu m^2$. This size is convenient to process and allows detailed study of the SVT properties. It might also be adequate for some applications such as magnetic field sensors, but it is certainly too large to serve as a memory element in a MRAM or as the sensing element in a magnetic read head. We therefore introduce a new fabrication process so as to be able to study the effects of scaling of the lateral dimensions of the SVT on its main electrical and magnetic properties.

In the next section, this new fabrication process will be described and we will emphasize the differences with the process for $350 \times 350\ \mu m^2$ transistors found in [5]. In the result and discussion section, the main magnetic and electrical properties of the SVT will be discussed in terms of size dependence. Insight in the failure mechanism of the SVT is also obtained from the size dependence study and will be discussed at the end of the result and discussion section.

II. Fabrication

High quality Schottky barriers are a necessity for proper operation of the SVT. Since it is not possible to grow device quality Si on top of metal films, we use an *in situ* metal bonding technique to form a metal bond between two Si wafers [6]. The bonded structure is further processed into smaller devices using standard photolithography and a series of dry and wet etching steps.

A fabrication process for SVTs is previously described in [5], the transistor dimensions ranged from 1×1 mm^2 to $350 \times 350\ \mu m^2$. The transistors in that process are designed to be contacted by direct ultrasonic wire bonding with Au wire, which becomes unpractical below $200 \times 200\ \mu m^2$ because of the minimum area needed for wire bonding. The new process described here differs from the previous process by the use of contact leads and bond pads that make the electrical connections to the transistor. Three main changes to the process in [5] are made to realize the miniaturization of the SVT. First, the emitters in [5] are etched from a 360 μm-thick Si wafer by a time-controlled etch process to a height of 30 μm. This height implies a large aspect ratio when the lateral emitter size is reduced to 10 μm and does not allow contact leads to the emitter, because the latter would suffer from the large step height. To solve this, we introduce the use of silicon-on-insulator (SOI) wafers, where we use the insulator layer (SiO_2) as an etch stop, which allows a reduction of emitter height from 30 μm

Manuscript received December 6, 2001; revised February 1, 2002. This work was supported in part by the Dutch Technology Foundation (STW) and Fellowship of the Royal Netherlands Academy of Arts and Sciences. The review of this paper was arranged by Editor J. N. Burghartz.

The authors are with the Systems and Materials for Information storage, MESA$^+$ Research Institute, University of Twente, 7500 AE Enschede, The Netherlands (e-mail: ron.jansen@el.utwente.nl).

Publisher Item Identifier S 0018-9383(02)04326-5.

to 3 μm. Secondly, the repair etch, as used in [5], designed to remove damaged silicon caused by an ion beam etch (IBE), also removed the small Si emitters. The damage to the Si is reduced by the use of a combination of ion beam and wet etch techniques and the repair etch no longer removes the small Si emitters. Finally, the introduction of contact leads and bond pads requires an insulating layer, for this we use SU8 [7], a negative tone photoresist.

Fig. 1 shows the steps in this process scheme. We start by preparing two separate wafers, an SOI wafer for the emitter and an n-Si (100) wafer for the collector. 30 nm of oxide is grown on both wafers by dry oxidation. This layer helps to smoothen the surface and it protects the wafers from subsequent steps. An additional Si_3N_4 layer is grown by PECVD on the backside of the n-Si wafer, which is needed later in the process. The wafers are sawn to 11.9×17.9 mm^2 for the n-Si wafer and 11.9×20.9 mm^2 for the SOI wafer. The two wafers are then immersed in a sequence of chemicals; 100% HNO3, 1% HF, 5% TMAH, 50% HF, after which they are free of saw dust and oxide.

The cleaned wafers are mounted on a bonding tool, specially designed for *in situ* metal bonding and loaded into an ultrahigh vacuum deposition system. When the pressure reaches the low 10^{-10} Torr range, the deposition of magnetic layers starts. A shutter hides the collector wafer (n-Si) during the deposition of Pt 20 Å/$Ni_{80}Fe_{20}$ 30 Å/Au 40 Å/Co 30 Å on the emitter SOI wafer. The shutter is opened before the deposition of the last 20 Å Au layer on both wafers, simultaneously. During the deposition of the last Au layer, the bonding tool is triggered and both wafers are bonded. The obtained structure is now SOI/Pt/NiFe/Au/Co/Au//Au/Si, where // denotes the metal bond, shown in Fig. 1 (2).

This structure is now immersed in TMAH 10% at 85°C, the handle Si layer of the SOI wafer is etched, while the buried oxide layer acts as an etch stop. Simultaneously the Si_3N_4 layer protects the n-Si wafer. The buried oxide is subsequently etched by BHF. The structure of the thinned sample is illustrated in Fig. 1 (3). A Cr/Au layer, patterned by lift off, is used as a mask for the device Si etch that defines the emitters. The lateral emitter size, used here, ranges from 300×300 μm^2 to 10×10 μm^2.

In [5], the base was delineated by IBE. The IBE creates damage to the collector Si causing undesirable edge leakage currents that undermine the working of the SVT. The damaged Si is removed by a repair etch with TMAH. The repair process etches not only the damaged Si but also the sides of the Si emitter. The time needed to repair the IBE damage also removed the small emitters and this process should thus be redesigned for small structures. This is accomplished by a combination of IBE and wet etching. We stop the IBE of the base layer in the last metal layer (Au) and continue to etch this layer with a KI solution. The etch rate of the IBE proved to be reproducible enough for a time controlled etch stop in the Au layer. The damage to the Si is reduced considerably, though a small edge leakage current remains. The repair etch is reduced in time accordingly and the small emitters survive. Fig. 1 (4) shows the transistor at this point in the process. The rectangular base is about twice the size of the emitter and ranges from 700×360 μm^2 to 22×14 μm^2.

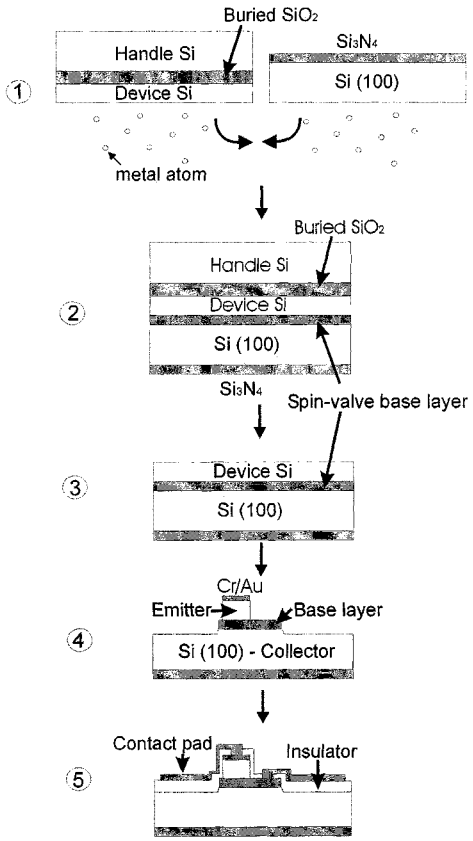

Fig. 1. Schematic diagram of the fabrication process. See text for details.

The transistor should be insulated before bond pads and contact leads to the transistor can be made. Negative tone photoresist, SU8 (Microresist, mr-L6500.5exp), is used for this purpose. SU8 is chosen for three reasons, first the low process temperature (< 140 °C), secondly, the good chemical and thermal stability and finally less process steps are required compared with SiO_2 or Si_3N_4 layers. A 300 nm thick layer of SU8 is spun onto the sample and the contact holes are formed by conventional photolithography. A Cr/Au metal film is then patterned by lift off to form the bond pads and contact leads [Fig. 1 (5)]. The transistor is finally contacted by ultrasonically wire bonding the bond pads with Au wire.

III. Results and Discussion

A. Schottky Diodes

The emitter and collector barriers are characterized by current–voltage (I–V) measurements, to confirm that they show no size dependence. The Schottky barrier height and ideality factor are determined by fitting the measured I–V curves with the thermionic emission theory. The resulting barrier height is plotted against transistor size in Fig. 2. The transistor size used throughout this article is the length of one side of the square emitter. Both the emitter and collector barrier height are independent of the transistor size over the investigated range. The Si/Pt emitter diode has a 0.86 ± 0.01 eV barrier height and Si/Au shows 0.80 ± 0.01 eV. The ideality factor is 1.04 ± 0.02, close to ideal thermionic emission for all diodes.

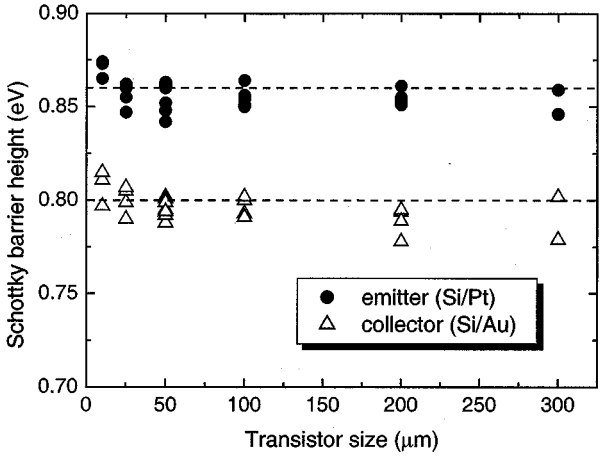

Fig. 2. Schottky barrier height of emitter and collector diode for various transistor sizes. The dotted lines indicate the average barrier height: 0.86 eV for the Si/Pt emitter and 0.80 eV for the Si/Au collector. The transistor size is an edge length of the square emitter.

B. Magnetocurrent

The collector current as a function of applied magnetic field is shown in Fig. 3 for all transistor sizes. The absolute collector current, with an applied emitter current of 1 mA, is shown on the left vertical axis. The relative change in collector current (magnetocurrent $MC = \left(I_C^P - I_C^{\mathrm{AP}}\right)/I_C^{\mathrm{AP}}$) is shown on the right vertical axis. I_C^P is the maximum collector current, which is obtained when the magnetizations of the two magnetic layers of the spin valve are aligned (parallel state). I_C^{AP} corresponds to the antiparallel state of the spin valve, where the collector current is reduced to its minimum value. As the SVT becomes smaller than 25 μm, the magnetization reversal process is no longer smooth, and small steps can be observed (see Fig. 3). This can possibly be attributed to process induced pinning sites along the base edge or by redeposition on the sides of the spin valve during the IBE etch of the base. More research is needed to optimize the magnetization reversal of the small transistors.

The MC as a function of transistor size is summarized in Fig. 4, which shows that the MC is constant around 240% over the investigated size range. This value is comparable to the previously measured value between 200% and 300% in the 350 μm transistors [4], [5] and verifies that this new process has no noticeable side effects on the main SVT property.

C. Transfer Ratio

While the MC value remains constant, the transfer ratio shows some size dependence, albeit weak. The transfer ratio is defined as the ratio of parallel collector current to emitter current ($\alpha = I_C^P/I_E$). For the SVT used here, it has a value around 10^{-5} above 25 μm, as shown in Fig. 5. It starts to decrease below 25 μm and is 6×10^{-6} for the 10 μm SVT. This can be attributed to the deterioration of the emitter efficiency, which is the ratio between the current that is actually injected as hot electrons and the total emitter current. Process-induced defects along the emitter edge can be responsible for this deterioration. Electrons passing through the edge defects enter the base layer with a lower energy and can thus not contribute to the collector current. This reduces the absolute collector current value but does not affect the relative collector current change, MC. This phenomenon is not an intrinsic property of the device, but related to the fabrication process.

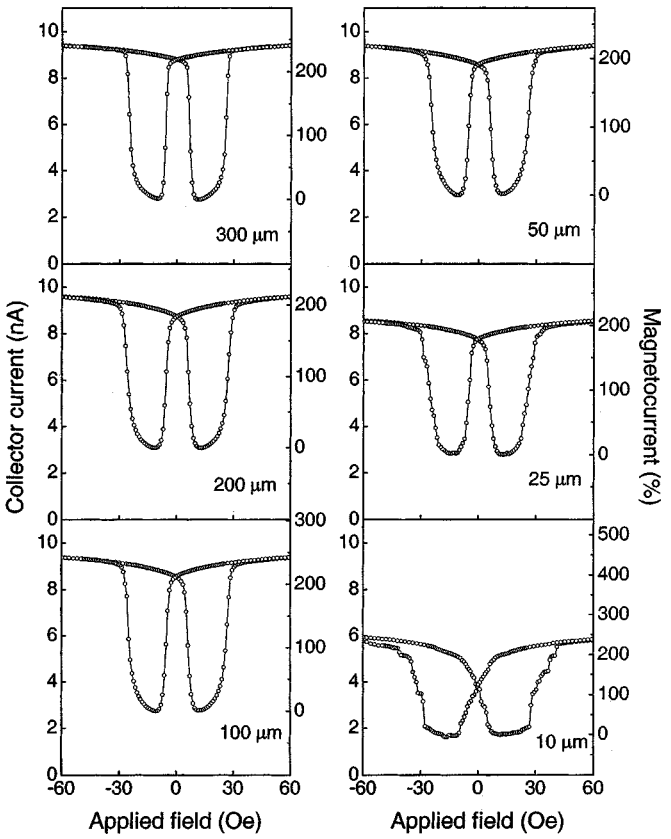

Fig. 3. Collector current as a function of applied field for various sized transistors. The emitter current is set to 1 mA. The absolute collector current is plotted on the left vertical axis and the corresponding MC on the right axis.

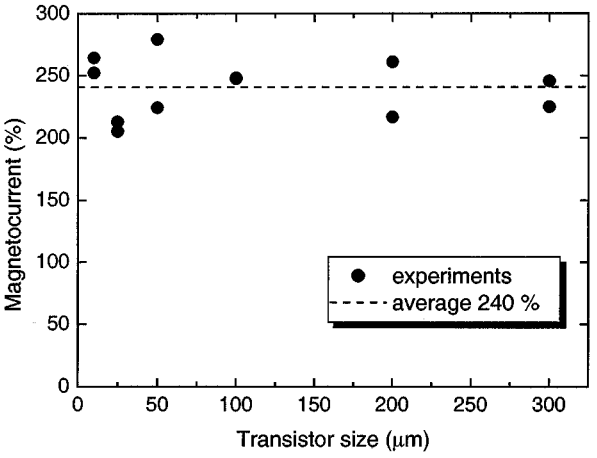

Fig. 4. Dependence of magnetocurrent on transistor size. The dotted line shows the average MC of 240%.

D. Leakage Current

The collector current consists of two parts, the current caused by the hot electron transfer across the base and an additional leakage current: $I_C = \alpha I_E + I_{\mathrm{leak}}$. Part of the leakage current is inherent to a reverse biased Schottky barrier. This is proportional to its area and another part is caused by process damage,

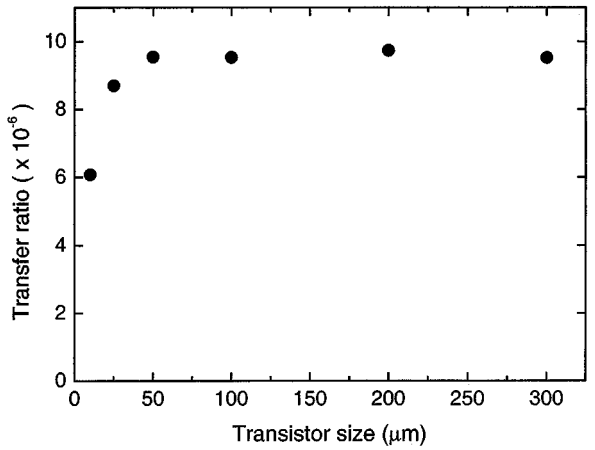

Fig. 5. Transfer ratio as function of transistor size.

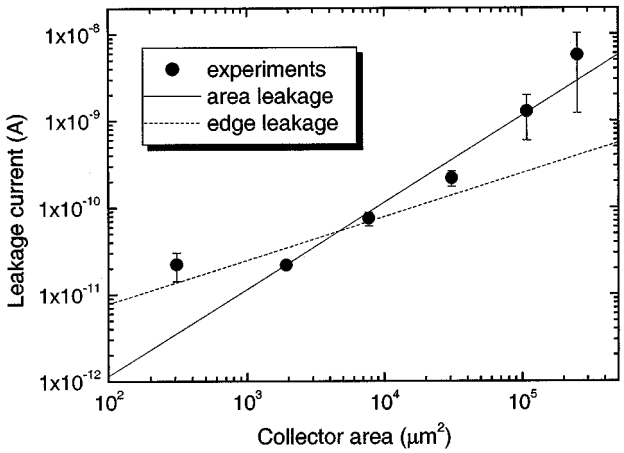

Fig. 6. Dependence of collector leakage current on collector area. The circles are the leakage currents of the reversed biased collector diode (1 V). Two lines that represent leakage current proportional to area (solid) and edge length (dotted) have also been included.

mainly around its edges. As described before, we use a repair etch to minimize process-induced leakage current. The repaired collector diode usually shows a leakage current below 10^{-9} A. In Fig. 6, the leakage current of the reverse-biased collector diode (1 V) with zero emitter current at room temperature is plotted against collector area on a log–log scale. In addition to the measured data, two lines are drawn, with $I_{\rm leak}$ proportional to area (solid) and edge (dotted), respectively. The leakage current can be fitted well with the line proportional to area, implying that area leakage current dominates the leakage current and the repair process is effective in suppressing the process-induced parasitic edge leakage current. The deviation of the smallest diode from the fit with the area leakage is either due to the increasing importance of edge with decreasing size or to the limit of the current measurement setup, which is in the 10^{-12} A range. The latter also makes it difficult to interpret the leakage current characteristics of emitter diode, which is an order of magnitude lower than that of collector diode due to the higher Pt/Si Schottky barrier, and hence, the results are not discussed here.

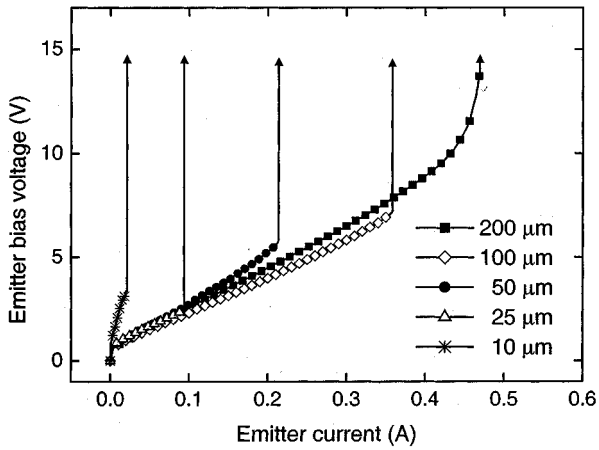

Fig. 7. Emitter bias voltage versus emitter current for different sized SVTs; the abrupt jump indicates the breakdown point.

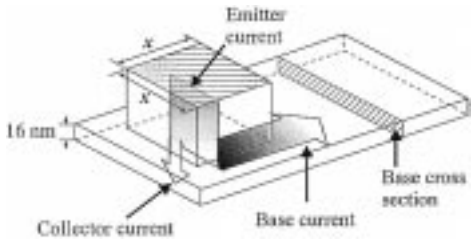

Fig. 8. Schematic diagram of the SVT showing the current flow and the cross sections. x is 10, 25, 50, 100, or 200 μm.

E. Maximum Input Current

To determine the maximum input emitter current we gradually increase the emitter current until device breakdown. Both the emitter bias voltage as well as the collector current is being monitored. As expected and shown in Fig. 7, the emitter bias voltage increases with higher emitter current and so does the collector current (not shown). The maximum emitter current is determined from the point where the emitter bias voltage jumps abruptly, indicating breakdown of the emitter or base.

A three-dimensional (3-D) schematic illustration shows the current flow in the SVT (Fig. 8). Note that the emitter current and base current are almost equal due to the low transfer ratio, while the cross section of the base is much smaller than the emitter area due to the thin base layer (16 nm).

Obviously, the breakdown current decreases for smaller transistors, top graph of Fig. 9. When we look at the current density in the emitter (J_E) at breakdown we see a strong increase with decreasing emitter area, middle graph of Fig. 9, this is counterintuitive and discarded as cause for device breakdown. However, when we look at the base current density (J_B) at breakdown it remains constant at around 1.7×10^7 A/cm^2, bottom graph of Fig. 9. This implies that the input current is limited by the maximum possible current density in the base and not by the much lower current density in the emitter.

Electromigration failure of the base is the most reasonable cause for this limit, which is indirectly confirmed by other studies of GMR sensors [8]–[10]. Here one finds breakdown of

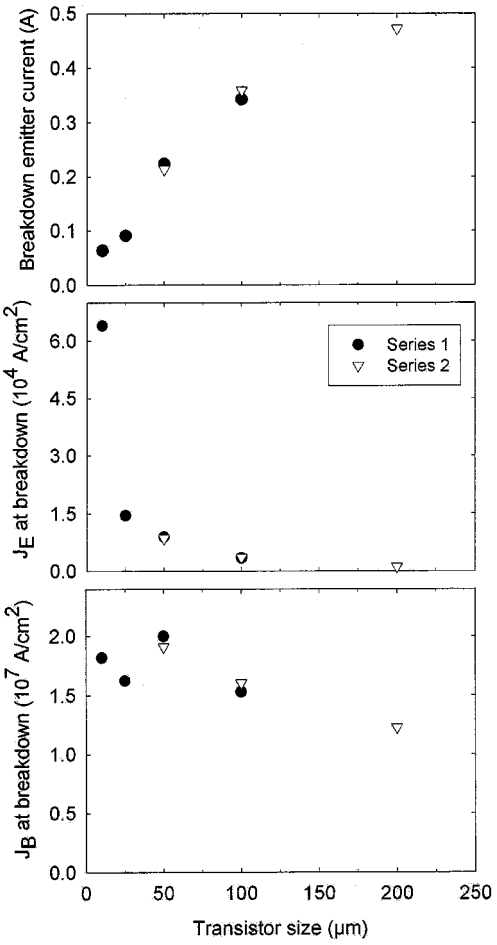

Fig. 9. (Top) Emitter current at device breakdown for two series of SVTs. (Middle) Emitter current density (J_E) at device breakdown. (Bottom) Base current density (J_B) at device breakdown.

the spin valve caused by electromigration failure at the same order of magnitude for the current density.

IV. Conclusion

SVTs with dimensions down to 10×10 μm^2 were successfully fabricated using SOI wafers, a combination of dry and wet etching techniques and SU8 as an insulating layer. These transistors were used to investigate the influence of size on the electrical and magnetic properties of the SVT.

We found that the Schottky barrier height was independent of the transistor dimensions, whereas the parasitic collector leakage current scaled proportional to the area. The magnetic response was also found to be independent of dimension, i.e., the MC remained constant around 240% for all transistor sizes. The transfer ratio showed a slight decrease for transistors with dimensions below 25×25 μm^2, which is probably caused by damage to the emitter edges. The highest current density of the SVT is found in the metal base. Breakdown occurred when the current density in the metal base exceeded 1.7×10^7 A/cm^2, which is in agreement with the value for electromigration failure of spin valves.

In conclusion, the intrinsic properties of the SVT do not show size-dependent behavior, which enables a further miniaturization.

References

[1] D. J. Monsma, J. C. Lodder, Th. J. A. Popma, and B. Dieny, "Perpendicular hot electron spin-valve effect in a new magnetic field sensor: The spin-valve transistor," *Phys. Rev. Lett.*, vol. 74, no. 26, pp. 5260–5263, June 1995.

[2] D. J. Monsma, R. Vlutters, and J. C. Lodder, "Room temperature-operating spin-valve transistor formed by vacuum bonding," *Science*, vol. 281, pp. 407–409, July 1998.

[3] G. A. Prinz, "Magnetoelectronics," *Science*, vol. 282, pp. 1660–1663, Nov. 1998.

[4] R. Jansen, O. M. J. van't Erve, S. D. Kim, R. Vlutters, P. S. A. Kumar, and J. C. Lodder, "The spin-valve transistor: Fabrication, characterization and physics," *J. Appl. Phys.*, vol. 89, no. 11, pp. 7431–7436, June 2001.

[5] P. S. A. Kumar, R. Jansen, O. M. J. van't Erve, R. Vlutters, P. de Haan, and J. C. Lodder, "Low-field magnetocurrent above 200% in a spin-valve transistor at room temperature," *J. Magn. Magn. Mat.*, vol. 214, pp. L1–L6, May 2000.

[6] T. Shimatsu, R. H. Mollema, D. Monsma, E. G. Keim, and J. C. Lodder, "Metal bonding during sputter film deposition," *J. Vac. Sci. Technol. A*, vol. 16, no. 4, pp. 2125–2131, July–Aug. 1998.

[7] K. Y. Lee, N. LaBianca, S. A. Rishton, S. Zolgharnain, J. D. Gelorme, J. Shaw, and T. H.-P. Chang, "Micromachining applications of a high resolution ultrathick photoresist," *J. Vac. Sci. Technol. B*, vol. 13, pp. 3012–3016, Nov.–Dec. 1995.

[8] I.-F. Tsu, C. Chang, and H. S. Elderman, "Electrical reliability of giant magneto-resistive recording sensors," in *Mat. Res. Soc. Symp. Proc.*, vol. 563, 1999, pp. 139–145.

[9] S. Shinubara, Y. Takeda, H. Sakue, T. Takahagi, and A. H. Verbruggen, "Electromigration reliability study of a GMR spin valve device," in *Mat. Res. Soc. Symp. Proc.*, vol. 563, 1999, pp. 145–153.

[10] S. Bae, I.-F. Tsu, E. S. Murdock, and J. H. Judy, "Electromigration-induced failure analyzes of single layred NiFe permalloy thin films for giant magnetoresistive read head," *J. Appl. Phys.*, vol. 90, pp. 2427–2432, Sept. 2001.

Sungdong Kim received the B.S., M.S., and Ph.D. degrees from the Department of Metallurgical Engineering, Seoul National University, Seoul, Korea, in 1992, 1994, and 1998, respectively.

He is currently working in the Storage Laboratory, Samsung Advanced Institute of Technology, as a Member of the Research Staff after a postdoctoral fellowship at SMI, MESA$^+$ Research Institute. His research interest is the fabrication of magnetic devices.

O. M. J. van't Erve, photograph and biography not available at the time of publication.

R. Vlutters, photograph and biography not available at the time of publication.

R. Jansen, photograph and biography not available at the time of publication.

J. C. Lodder (M'89), photograph and biography not available at the time of publication.