Furnace and rapid thermal crystallization of amorphous $\text{Ge}_x\text{Si}_{1-x}$ and Si for thin film transistors

J.B. Rem, M.C.V. de Leuw, J. Holleman, J.F. Verweij

MESA Research Institute, University of Twente, PO Box 217, NL-7500 AE Enschede, The Netherlands

Abstract

The crystallization behavior of polycrystalline silicon (Si) and germanium–silicon alloys ($\text{Ge}_x\text{Si}_{1-x}$) from SiH_4 and GeH_4 , where x is in the range of 0–0.32, has been investigated for thin film transistor (TFT) applications. Furnace anneals as well as rapid thermal anneal (RTA) and combinations of these two techniques have been used to crystallize amorphously deposited thin (≤ 100 nm) films. The effects of time and temperature for the furnace anneals and time, temperature and pulse rate for the RTA have been investigated. Smooth Si and $\text{Ge}_x\text{Si}_{1-x}$ layers with a surface roughness ≤ 0.6 nm have been obtained using an initial Si layer for the $\text{Ge}_x\text{Si}_{1-x}$ material, since $\text{Ge}_x\text{Si}_{1-x}$ shows a nucleation problem on oxide surfaces which influences the resulting surface roughness and grain size. For TFT applications the optimal film properties cannot be obtained with a single crystallization anneal. Conventional furnace crystallization results in smooth layers with Si furnace crystallized films exhibiting small grains with many intra-grain defects. An average grain size of approximately 300 nm for $\text{Ge}_{0.25}\text{Si}_{0.75}$ and slightly larger grains for $\text{Ge}_{0.32}\text{Si}_{0.68}$ with less defects is obtained at lower temperature. RTA results for Si and $\text{Ge}_x\text{Si}_{1-x}$ in fine grained material with lower defect density. © 1997 Elsevier Science S.A.

Keywords: Amorphous materials; Crystallization; Silicon; Germanium

1. Introduction

For the integration of thin film electronics and sensors and for large area applications on glass substrates it is essential that the process temperatures are well below the critical temperatures for the glass substrates (warping) and/or the sensors (stability). Until now, large area electronics for applications in active matrix liquid crystal displays (AMLCDs) were made in amorphous silicon (a-Si), which has sufficient electrical capacity for the next two generations of AMLCDs [1]. However, the driver circuits cannot be made in a-Si because of a lack of drive current. It has been suggested to use polycrystalline silicon (poly-Si) for driver circuits [2]. The drawback of poly-Si is that high process temperatures are needed, typically above 600 °C, and a relatively large leakage current exists [3]. Laser crystallization is now most commonly used for poly-Si TFTs eliminating the high temperatures but uniformity is an important issue here. Recently, polycrystalline germanium–silicon alloys (poly- $\text{Ge}_x\text{Si}_{1-x}$) have been under investigation [4–7] because these materials can be obtained in a polycrystalline form at temperatures as low as 400 °C. $\text{Ge}_x\text{Si}_{1-x}$ alloys have been found to grow faster, crystallize at lower temperature with larger grain size, nucleate with difficulty on SiO_2 surfaces [8,9] and can be electrically activated with lower acti-

vation anneals compared to Si. In general, and for thin film transistor (TFT) applications in particular, this comprises a challenge: the deposition of the poly- $\text{Ge}_x\text{Si}_{1-x}$ layer on gate oxides or glass substrates is difficult because the nucleation of the $\text{Ge}_x\text{Si}_{1-x}$ film is poor, resulting in rough interfaces, while smooth layers are required for reliable operation of TFTs.

In this study the crystallization of amorphously deposited thin (≤ 100 nm) films of Si and $\text{Ge}_x\text{Si}_{1-x}$ is optimized for TFT applications using conventional furnace anneals and rapid thermal anneals (RTA). The aim is to obtain a smooth film with a large grain size and a low intra-grain defect density.

2. Experimental

Amorphous Si and $\text{Ge}_x\text{Si}_{1-x}$ films have been deposited on oxidized 3" wafers using a conventional low-pressure chemical vapor deposition (LPCVD) reactor. Variation of the ratio of the (VLSI grade 100%) SiH_4 to GeH_4 gas flows allows the Ge content to be varied between 0 and 32%. The deposition temperature is 550 °C for Si to obtain the smoothest Si layer [10] and 485 °C for $\text{Ge}_x\text{Si}_{1-x}$. A smooth initial Si layer, effectively a few monolayers thick, is deposited at 485 °C to

Table 1

Initial experimental set-up. Crystalline state measured with XRD after furnace anneal steps (unless otherwise stated) for $\text{Ge}_x\text{Si}_{1-x}$ films without initial surface treatment

Ge (%)	As deposited	450 °C 3 h	450 °C 16 h	450 °C 66 h	500 °C 1 h	500 °C 3 h	500 °C 16 h	550 °C 1 h	550 °C 3 h	550 °C 16 h	RTA 700 °C 10 s	RTA 700 °C 60 s
0%	A	A	A	A	A	A	² P	² P	² P	² P	A	A
25%	A	A	A	A	¹ P	¹ P		² P	² P	² P	A	A
30%	A			A	² P	² P		² P	² P	² P		
32%	A	A	A	A	² P	² P		² P	² P	² P	A	² P

A, amorphous; ¹P, crystallization started; ²P, fully crystalline.

Table 2

Second experimental set-up. Crystalline state measured with XRD after furnace anneal steps (unless otherwise stated) for $\text{Ge}_x\text{Si}_{1-x}$ films with initial surface treatment

Ge content (%)	As deposited	500 °C 3 h	500 °C 16 h	550 °C 3 h	RTA pulse 750 °C	RTA continuous 700 °C
0%	A	A	² P	² P	² P	A
25%	A	A	A	² P	² P	² P
32%	A	A	¹ P	² P	² P	² P

A, amorphous; ¹P, crystallization started; ²P, fully crystalline.

improve the nucleation of $\text{Ge}_x\text{Si}_{1-x}$. Furnace anneals at 450, 500 and 550 °C for 1, 3, 16 and 66 h have been applied to crystallize the thin film. RTA is performed using a 35 kW arc lamp equipped Peak Systems RTP reactor. RTA crystallization recipes consist of a constant power supply at 700 °C for 1 min or a base temperature of 450 °C with 1–20 heat pulses at 750 °C of 1 s each. A summary of the experimental set-up is given in Table 1. The crystal orientation is obtained by X-ray diffraction (XRD) and the extent of crystallinity is measured by XRD and reflectometry. The surface roughness is compared using atomic force microscopy (AFM) and high-resolution scanning electron microscopy (HRSEM). Grain sizes are estimated using a crystal defect etch and HRSEM observation. The crystal defect etch is a modified Secco etch with the following composition: 200 ml 50% HF, 100 ml H_2O and 3.3 g CrO_3 . Samples were dipped in the etch for less than a second to delineate the crystal grain boundaries and the intra-grain dislocations. Optical properties are obtained using reflectometry and ellipsometry. The sheet resistance is measured with a four-point probe. The Ge content is measured by energy dispersive X-ray analyses (EDX) and verified by the XRD peak shift.

3. Results and discussion

In Fig. 1 the average deposition rate of amorphous and polycrystalline Si and $\text{Ge}_x\text{Si}_{1-x}$ as a function of deposition temperature for a total pressure of 1.0 mbar is given. It can be seen that for $\text{Ge}_x\text{Si}_{1-x}$ deposition comparable growth rates to Si can be obtained at lower temperatures while a higher Ge% results in higher growth rates. Also included is the

deposition rate of 500 °C at 1.0 mbar total pressure deposited Si at 0.4 nm min^{-1} showing that this process condition is impractical for production. Therefore Si is deposited at 550 °C and 1.0 mbar total pressure.

The $\text{Ge}_x\text{Si}_{1-x}$ films have been examined by XRD to verify the amorphous state, as shown in Tables 1 and 2. Since a 40% Ge film could not be deposited amorphously at 485 °C, even if a high pressure of 1.0 mbar is used, three variations have been investigated: 0, 25 and 32% Ge. In Fig. 2 the first signs of crystallization as obtained with XRD are plotted for (a) as-deposited $\text{Ge}_{0.32}\text{Si}_{0.68}$, (b) 1 h 550 °C furnace crystallized Si, (c) 3 h 550 °C furnace crystallized $\text{Ge}_{0.25}\text{Si}_{0.75}$ and (d) 16 h 500 °C furnace crystallized $\text{Ge}_{0.32}\text{Si}_{0.68}$. This shows that the highest Ge% can indeed be deposited amorphously. Lower Ge% are also amorphous for the same deposition conditions.

Fig. 1. The deposition rate of poly-Si (■) and poly- $\text{Ge}_x\text{Si}_{1-x}$. ♦: $x = 0.25$, ●: $x = 0.30$, ▲: $x = 0.32$.

Fig. 2. First signs of crystallinity measured by XRD for (a) as-deposited $\text{Ge}_{0.32}\text{Si}_{0.68}$, (b) Si after 1 h 550--360 °C, (c) $\text{Ge}_{0.25}\text{Si}_{0.75}$ after 3 h 550 °C, and (d) $\text{Ge}_{0.32}\text{Si}_{0.68}$ after 16 h 500 °C.

The $\text{Ge}_x\text{Si}_{1-x}$ seems to need a comparable to longer crystallization time and temperature than Si. We believe this difference is due to the initial Si layer deposited at 485 °C prior to the $\text{Ge}_x\text{Si}_{1-x}$ deposition, which is totally amorphous. Si deposited at 1.0 mbar and 550 °C exhibits crystals at the SiO_2/Si interface because it is deposited in the transition regime of amorphous and polycrystalline phase formation. These microcrystals can act as seeds which enhance the crystallization process. Amorphous Si deposited at 500 °C and 1.0 mbar total pressure shows no crystalline interface nuclei.

The time to crystallization from the amorphous state to full crystallization is determined by the density of initial crystallization nuclei, the rate of formation of new crystallization nuclei and the solid phase epitaxial growth rate and is given by Olson and Roth [11]. In the case of a-Si deposition at 550 °C a TEM investigation shows that at the Si-SiO₂ interface a large density of crystalline nuclei is found. These nuclei seem to be related to the initial growth rather than to the intrinsic nucleation. The crystallization at 550 °C for 1 h results in full crystallization. The solid phase epitaxial growth rate of Si at 550 °C is 360 nm h⁻¹ [11]. The shorter time needed for crystallization therefore has to be attributed to the initial crystalline nuclei. For a- $\text{Ge}_x\text{Si}_{1-x}$ a surface pre-treatment is always given for 5 min in SiH₄ at 485 °C and 1.0 mbar. This kills the long incubation time found for $\text{Ge}_x\text{Si}_{1-x}$ deposition on an oxide surface [9] and results in a smooth a-Si on which the $\text{Ge}_x\text{Si}_{1-x}$ continues its growth. So, for $\text{Ge}_x\text{Si}_{1-x}$ deposition no initial crystalline nuclei are present. The time to crystallization is now determined by the rate of crystalline nuclei

formation and the solid phase epitaxial growth rate. A higher Ge content results in a higher solid phase epitaxy and therefore decreases the time and/or temperature needed for crystallization.

The grain size is also determined by the rate of crystalline nuclei formation and the solid phase epitaxy. In Fig. 3 the surface of Si (a–b–c), $\text{Ge}_{0.25}\text{Si}_{0.75}$ (d–e–f) and $\text{Ge}_{0.32}\text{Si}_{0.68}$ (g–h–i) is shown as viewed by SEM after the modified Secco etch. The top three pictures (a, d, g) are for as-deposited films, the center three (b, e, h) for films annealed at 550 °C for 3 h in a furnace and the bottom three (c, f, i) for RTA films. The as-deposited films show almost no contrast indicating an amorphous state. The white spots found for $\text{Ge}_{0.25}\text{Si}_{0.75}$ cannot be explained yet, but it is apparent that the as-deposited $\text{Ge}_{0.25}\text{Si}_{0.75}$ film is also very smooth and amorphous. Clearly, both the furnace and the rapid thermal anneals change the films since many grain boundaries and dislocations are visible. For Si no strong difference can be observed between the two kinds of anneal; the grain boundaries and dislocations are of comparable sizes and quantities. This is again due to the initial crystalline nuclei which determine the morphology, instead of random nucleation and solid-phase epitaxy of newly formed nuclei. For $\text{Ge}_{0.25}\text{Si}_{0.75}$ large, flat grains can be seen for the furnace annealed sample with twin dislocations in the center of the grains. The dark areas consist of oxide because the $\text{Ge}_{0.25}\text{Si}_{0.75}$ film is etched away at those spots. The RTA sample shows more and smaller grains with less twin dislocations and intra-grain defects. The higher temperature obtained by the rapid thermal heat pulses effectively

Fig. 3. SEM pictures of the etched surface of Si (a–b–c), $\text{Ge}_{0.25}\text{Si}_{0.75}$ (d–e–f) and $\text{Ge}_{0.32}\text{Si}_{0.68}$ (g–h–i) as deposited (a, d, g), after a furnace anneal of 3 h 550 °C (b, e, h) and after an RTA (c, f, i).

removes many crystal defects. The $\text{Ge}_{0.32}\text{Si}_{0.68}$ film shows comparable results to the $\text{Ge}_{0.25}\text{Si}_{0.75}$ layer, although the grains show a slightly smaller size for both types of anneal. The crystallization temperature of 550 °C is believed to be too high for this Ge% for optimum film properties as mentioned earlier.

For TFT applications the interface roughness should preferably be as low as possible. The surface roughness of as-deposited and crystallized films has been investigated with AFM. The results are summarized in Fig. 4. The nucleation process of $\text{Ge}_x\text{Si}_{1-x}$ on the oxide surface results in rough films [4] due to the lower nucleation rate and higher growth rate. This is shown in the left part of Fig. 4. The initial Si layer yields a much improved surface roughness, even after crystallization as seen in the right part of Fig. 4. The surface roughness does not change significantly after the crystallization anneals, most probably due to the presence of a thin native oxide during annealing. The RTA shows the smallest variation in surface roughness between the different Ge%, although the difference falls within the uncertainty of the AFM surface roughness measurements.

A four-point probe is used to measure the sheet resistance $R_{\square}$. The sheet resistance of films changes as the layers are crystallized. Due to the isolating properties of the intrinsic Si and $\text{Ge}_x\text{Si}_{1-x}$ the sheet resistance can, however, not be quantified. This method is not useful for evaluation of the crystallization process.

4. Conclusions

The crystallization of thin Si and $\text{Ge}_x\text{Si}_{1-x}$ films has been investigated for application in TFTs. A smooth surface with a largest grain size of 300 nm is obtained for $\text{Ge}_{0.25}\text{Si}_{0.75}$ and $\text{Ge}_{0.32}\text{Si}_{0.68}$ by annealing for 3 h at 550 °C in a furnace. Applying an RTA with 1–20 750 °C pulses from a base temperature of 450 °C also results in a smooth surface but yields smaller grains. The defect density within the grains is lowered drastically with RTA. A combination of a furnace anneal with a subsequent RTA seems very promising and will be investigated in the future. Electrical characterization by sheet resistance is not possible due to the isolating properties

Fig. 4. Surface roughness values obtained with AFM. Films without an initial Si layer show a high surface roughness (left part) while using the initial Si layer results in a very smooth surface roughness (right part). No effect of the crystallization anneal on the surface roughness occurs.

of intrinsic Si and $\text{Ge}_x\text{Si}_{1-x}$. Application in TFTs is in progress.

Acknowledgements

All members of the MESA Research Center Clean Room staff are gratefully acknowledged. This project is financed by FOM, the Dutch Foundation for Fundamental Research on Matter.

References

- [1] R. Bruce, M. Hack, A. Lewis and I.-W. Wu, *Info. Displays*, 10/91 (1991) 14.
- [2] I. Washizuka, *IEDM*, 93 (1993) 937.
- [3] M.J. Thompson, *J. Non-Cryst. Solids*, 137&138 (1991) 1209.
- [4] J.B. Rem, J. Holleman and J.F. Verweij, *Proc. ESSDERC'95* (1995) 683.
- [5] T.-J. King and K.C. Saraswat, *IEEE Electron. Dev. Lett.*, 13 (1992) 309.
- [6] C. Salm, J. Klappe, J. Holleman, J.B. Rem and P.W. Woerlee, *Mater. Res. Soc. Proc.*, 343 (1994) 721.
- [7] T.-J. King and K.C. Saraswat, *IEEE Trans. Electron. Devices*, 41 (1994) 1581.
- [8] J. Holleman, A.E. Kuiper and J.F. Verweij, *J. Electrochem. Soc.*, 140 (1993) 1717.
- [9] J.B. Rem, C. Salm, J.H. Klootwijk, M.H.H. Weusthof, J. Holleman and J.F. Verweij, *Mater. Res. Soc. Proc.*, 387 (1995) 323.
- [10] J.H. Klootwijk, H. van Kranenburg, C. Cobianu, V. Petrescu, P.W. Woerlee and H. Wallinga, *Proc. ESSDERC'95* (1995) 383.
- [11] G.L. Olson and J.A. Roth, Kinetics of solid phase crystallization in amorphous silicon, *Mater. Sci. Rep.*, 3 (1988) 1–78.