High-Performance Deep SubMicron CMOS Technologies with Polycrystalline-SiGe Gates

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***Abstract*—The use of polycrystalline SiGe as the gate material for deep submicron CMOS has been investigated. A complete compatibility to standard CMOS processing is demonstrated when polycrystalline Si is substituted with SiGe (for Ge fractions below 0.5) to form the gate electrode of the transistors. Performance improvements are achieved for PMOS transistors by careful optimization of both transistor channel profile and p-type gate workfunction, the latter by changing Ge mole fraction in the gate. For the 0.18 μm CMOS generation we record up to 20% increase in the current drive, a 10% increase in the channel transconductance and subthreshold swing improvement from 82 mV/dec to 75 mV/dec resulting in excellent "on"/"off" currents ratio. At the same time, NMOS transistor performance is not affected by gate material substitution.**

***Index Terms*—CMOSFET's, MOS devices.**

I. Introduction

In recent years, the continuing miniaturization of Si MOS transistors for increased chip packing density and performance has resulted in significant research efforts in suppression of the so-called "short-channel effects" (SCE's). The SCE's are caused by an increased influence of the drain potential on the source depletion region in short devices. These effects are usually tackled by raising the substrate doping level to reduce the lateral extension of the drain depletion region. This, however, can result in significant deterioration of performance of the transistors: the reduced carrier mobility in a heavily doped region results in a decreased current drivability (I_{DS}^{sat} or I_{ON}) of the devices, while the subthreshold voltage swing is increased, resulting in higher levels of off-state leakage currents (I_{OFF}). A partial solution can be achieved by using vertical doping redistribution to reduce it in the channel region only ("super-steep retrograde" (SSR), or "ground plane" channel designs) [1]. Unfortunately, the removal of the dopants from the interface regions results in unacceptably high I_{OFF}, because of the low threshold voltage (V_T) values in this case. In this paper we demonstrate that a complete solution can be achieved by combination of the channel doping profiling with change in the gate workfunction. The threshold voltage is set by the chosen gate-to-semiconductor workfunction difference while the channel profile is engineered to control SCE and to obtain desired I_{ON}/I_{OFF} ratios.

Heavily-doped n- and p-type polycrystalline Si films (poly-Si), that are conventionally used in modern CMOS technologies as gate materials, have a fixed gate-to-semiconductor workfunction difference (Φ_{MS}), determined by the electron affinity and the band gap of the materials. It is well known, however, that the polycrystalline silicon-germanium alloy films (poly-SiGe) have good compatibility with standard CMOS processing. The dopant activation in poly-SiGe is comparable to poly-Si, and is actually better for p-type material. Most importantly for the work presented here, the p-type workfunction is decreasing with increase in the Ge mole fraction [1]–[7]. Poly-SiGe is therefore a promising material for p-type gate workfunction engineering. The workfunction change originates in band gap reduction caused mainly by the increase of the effective SiGe lattice constant with an increase in the Ge percentage. For high Ge concentrations it has also been reported [5] that a significant amount of stress in the poly-SiGe grains results in an extra reduction of the poly-SiGe gate workfunction.

When poly-Si is substituted by poly-SiGe as a gate material for the PMOS device, the change in the gate to semiconductor workfunction difference, $\Delta\Phi_{MS}$, for a given Ge mole fraction, can be calculated as the difference in the energy band gaps of two heavily-doped materials: $\Delta\Phi_{MS} = E_G^{\text{poly}-\text{Si}} - E_G^{\text{poly}-\text{SiGe}}$, since poly-SiGe has practically the same electron affinity as poly-Si. The change in Φ_{MS} can be coupled to the change of the V_T through the simple dependence on the uniform substrate doping level N_D [8]:

$$V_T = \frac{\Phi_{MS}}{q} - \frac{qN_{ox}}{C_{ox}} + 2\phi_B + K\sqrt{2\phi_B + |V_B|} \tag{1}$$

$$\phi_B = \frac{kT}{q}\ln\left(\frac{N_D}{n_i}\right), \quad K = \frac{\sqrt{2qN_D\varepsilon_{Si}\varepsilon_0}}{C_{ox}} \tag{2}$$

where q is an electron charge, N_{ox} and C_{ox} are the gate oxide charge and capacitance per unit area, and ϕ_B and V_B are the bulk Fermi potential and the substrate bias, respectively. K here is a body factor, ε_{Si} and ε_0 are the dielectric constants of Si and vacuum. Changing the workfunction difference without changing the channel profile results in an increase of the V_T of the devices and reduces I_{OFF} without changing the subthreshold swing value, S (determined by the doping in the channel region).

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Alternatively, one can explore the reduced $\Phi_{\rm MS}$ of p-type poly-SiGe gates to reduce the number of the dopants close to the surface, while retaining the V_T at the reference value. This is the approach we take in this paper. As a result of such channel profile manipulation, the following PMOS parameters are expected to be improved:

- The effective transverse electric field towards the Si-SiO_2 interface will be decreased, which, together with removal of the scattering centers from the channel, will lead to a higher hole channel mobility [9]. For PMOS devices $I_{\rm DS}^{\rm sat}$ is proportional to the hole mobility since, for a given generation of PMOS devices, the lateral electric field is not high enough for a complete velocity saturation to occur [10].
- The subthreshold swing (rate of subthreshold drain current increase with gate bias), S, is reduced as a result of a decrease in the depletion layer capacitance. Reduction in the subthreshold swing improves the $I_{\rm ON}/I_{\rm OFF}$ ratio.
- The body factor K (a coefficient describing the dependence of V_T on the substrate bias, see (2)) is reduced, a property which can be advantageous in CMOS applications to weaken the threshold voltage dependence on variations in the substrate potential.
- The saturation current is increased further by an increase of the saturation voltage $|V_{\rm DS}^{\rm sat}|$ (the drain bias at which drain current saturates, scales with the inverse body factor).

To avoid an increase of SCE when the channel doping is reduced a careful re-engineering of the doping profile is necessary. Ideally, one would need here a steplike profile to suppress these effects, with a SSR profile resembling it closest in reality. We show below that this approach works extremely well for poly-SiGe gates with less than 50% Ge content for 0.18 μm generation. For higher Ge percentages, the penalty of SCE increase becomes too big to be compensated by the increase in device performance.

The paper is organized as follows: Section II briefly describes the relevant properties of poly-SiGe films and technological aspects of poly-SiGe integration into mainstream silicon IC processing. Section III concentrates on the submicron MOSFET device design that is most beneficial for this gate material. A comparative study of deep submicron PMOS devices fabricated in a conventional way (with poly-Si gate) and with poly-$Si_{0.7}Ge_{0.3}$ as a gate material is presented. This demonstrates that a significant improvement in the PMOS performance can be achieved by a self-consistent engineering of both gate workfunction and channel profile. In Section IV we address the issue of CMOS integration and show the results of a successful integration of poly-SiGe gates into full 0.18 μm CMOS processing. Some final points on the limits of poly-SiGe CMOS integration and scaling with this gate material will be discussed in Section V and overall conclusions will be drawn in Section VI.

II. Poly-SiGe as a Gate Material

Recently, there have been quite a number of reports on the properties of heavily doped poly-SiGe films [2]–[6], [11]–[13]. Production scale integration of poly-SiGe into the CMOS processing flow will require the know-how of the following issues: deposition, pattern transfer, dopant diffusion and activation, gate oxide quality and $\Phi_{\rm MS}$ dependence on the Ge mole fraction. We will summarize below the experimental observations concerning these properties of poly-SiGe.

In our experiments we have used standard LPCVD furnaces to grow poly-SiGe layers on top of thin gate oxides using a mixture of silane (SiH_4) and germane (GeH_4) with inert N_2 as a carrier gas. A special care was taken to ensure that the deposited layers were smooth (less than 10 nm surface roughness RMS) with columnar polycrystalline grains of a characteristic size of 50–100 nm. The grain size control is of importance since, as has been shown recently in [14], it can significantly influence matching of the transistors, crucial for analog applications. Deposition temperatures down to 440 °C and total chambers pressures up to 1 torr have been used to enable growth of poly-SiGe material with these properties with up to 70% Ge content.

The etching chemistry of the poly-SiGe gate patterning was based on the standard polysilicon etch in HBr/HCl plasma with end-point detection on the gate oxide. Increase in Ge percentage results in an increase of the etching rate (up to ~3 times for 70% Ge as compared to poly-Si) which can hamper the uniformity of the etched profiles across the wafer for gates with high Ge content. In this regime (above ~50% Ge) a specially developed etching chemistry should be used [11].

The comparison of dopant diffusion in poly-Si and poly-SiGe have been extensively discussed elsewhere (see [4] and references therein) and there is a general understanding that boron diffusion in poly-SiGe is slower, while arsenic and phosphorus diffusions are faster than in poly-Si. These differences are increasing with Ge fraction. At the same time, boron activation is higher in poly-SiGe while arsenic is more difficult to activate in poly-SiGe, especially when the Ge percentage rises above ~50% (less than 30% of available arsenic atoms are electrically active for 50% Ge; this value is similar for phosphorus dopants) [4], [5], [12]. There is also a striking difference in the de-activation of dopants during additional thermal steps (the post-gate processing of the CMOS devices, for example, salicidation, intermetal dielectric deposition, etc.). Boron in poly-SiGe deactivates much slower than in poly-Si, e.g. only 20% of boron deactivates in poly-$Si_{0.7}Ge_{0.3}$ after extra anneal of 60 min at 750 °C while the deactivation level increases to 70% in poly-Si. Arsenic deactivation is similar in both materials [4]. These facts suggest that poly-SiGe allows for good dopant activation in p-type gates, while for higher Ge mole fractions n-type gate activation becomes problematic.

It has been reported that the use of poly-SiGe does not result in any gate oxide quality degradation [13], [16]. In fact, when furnace annealing is used for PMOS devices, the accumulated charge to gate oxide breakdown ($Q_{\rm BD}$) is significantly increased [13]. This is due to the smaller boron diffusion coefficient in poly-SiGe which reduces the number of charged states in the gate oxide associated with boron penetration. The reduction of the gate material bandgap naturally results in an increase in the Fowler–Nordheim tunneling current proportional to the reduction in the SiGe bandgap. Yet, the gate-substrate biases used in modern CMOS devices are much too low compared

to the potential differences required for Fowler–Nordheim tunneling to add significantly to the gate leakage currents.

Fig. 1 summarizes the impact of the Ge mole fraction change in the p-type poly-SiGe gate on the gate-semiconductor workfunction difference Φ_{MS} based on the data available from literature [2], [6], [7] and our own measurements. The change in Φ_{MS} is usually measured from the flatband voltage dependence on the gate oxide thickness, assuming that density of the interface states stays constant [8]. One can see that there is significant spread in the values which is most probably caused by the manner in which the flatband voltage has been measured, or by some ambiguity in the determination of the Ge mole fraction at the interface after the whole processing sequence. It is also known that Φ_{MS} depends on the poly grain-size [15]. That is why, for accuracy, only poly-SiGe films with similar grain structures should be compared (the data are not available in all cited references). The plot does provide, however, a general trend of Φ_{MS} shift with change in Ge fraction. For example, PMOS capacitors with 30% Ge content show an ~0.2 eV shift in the workfunction as compared to poly-Si. There is essentially no change in Φ_{MS} for n-type poly-SiGe [2], [6].

We have outlined in this section the material properties of poly-SiGe relating to its integration into a standard MOS processing flow. It is expected that poly-SiGe can substitute poly-Si as a CMOS gate material for Ge mole fractions not exceeding 0.5 (for both n- and p-type gates). For these lower Ge percentages only minor variations to the processing flow are needed; the electrical properties of n-type gates are not severely degraded, while the p-type gates show improvement in electrical performance and the change in Φ_{MS} is sufficient for gate workfunction engineering.

III. PMOS Device Design with Poly-SiGe Gates

A. Experimental Details

In order to measure the performance increase when the channel profile is adapted to the use of poly-SiGe gates, we have fabricated PMOS devices in the 0.18 μm technology with both poly-$\mathrm{Si_{0.7}Ge_{0.3}}$ and poly-Si gates. Channel profiles were designed to have the same V_T for both devices (Fig. 2, traces marked "default Si" and "SiGe"). The poly-$\mathrm{Si_{0.7}Ge_{0.3}}$ and poly-Si were deposited at 460 °C and 625 °C respectively. The rest of the standard 0.18 μm processing flow has been reproduced featuring LOCOS isolation, 4 nm gate oxide, $\mathrm{BF_2^+}$ implantations to form source/drain regions (LDD's and HDD's) and to dope the gate. Rapid thermal anneals (RTA's) were used to anneal implantation damage and to diffuse and activate the dopants [16].

As we have already mentioned, the activation of the poly-SiGe p-type gates can be better than their poly-Si counterparts. In order to have a valid comparison, not affected by the values of the poly-gate depletion, the devices with poly-$\mathrm{Si_{0.7}Ge_{0.3}}$ gates were subjected to somewhat lower thermal budget to ensure the same gate activation level (as confirmed by the capacitance–voltage (*C–V*) measurements presented in Fig. 3). One can readily see in the quasistatic *C–V* curves that there is noticeable difference in the flatband voltages and substrate doping levels for devices with poly-Si and poly-$\mathrm{Si_{0.7}Ge_{0.3}}$ gates, while the threshold voltage and gate depletion have the same values.

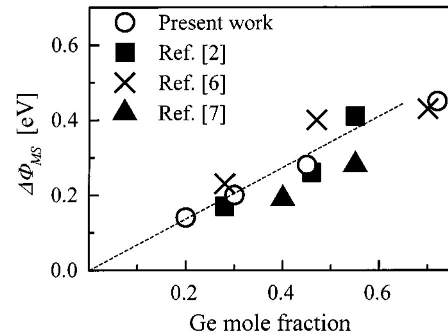

Fig. 1. Dependence of the p-type poly-SiGe gate to n-type semiconductor workfunction difference, $\Delta\Phi_{\mathrm{MS}}$, on the Ge mole fraction. The change in $\Delta\Phi_{\mathrm{MS}}$ is measured by the extrapolation of the flatband voltage to $t_{\mathrm{ox}} = 0$ [8]. Dashed line is a guide to the eye only.

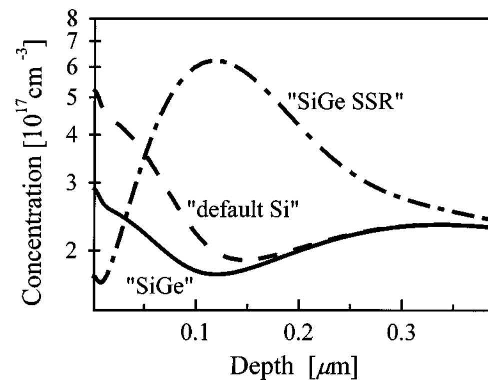

Fig. 2. Various PMOS channel doping profiles used in this study as measured by SIMS (arsenic and phosphorus dopants). The "default Si" and "SiGe" profiles are designed to result in the same V_T when used with poly-Si and poly-$\mathrm{Si_{0.7}Ge_{0.3}}$ gates respectively. "SiGe SSR" was used to improve SCE behavior of CMOS devices in Section IV.

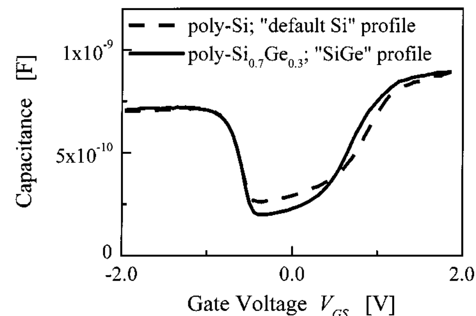

Fig. 3. Quasistatic *C–V* measurements of capacitors with poly-Si and poly-$\mathrm{Si_{0.7}Ge_{0.3}}$ gates. Thermal budget was reduced for poly-$\mathrm{Si_{0.7}Ge_{0.3}}$ to obtain the same amount of gate depletion (determined as percentile change of the capacitance in inversion as compared to that in accumulation).

B. Experimental Results

The body-factor K is significantly lower in the PMOS devices with poly-$\mathrm{Si_{0.7}Ge_{0.3}}$ gates due to the lower channel doping level. It is measured to decrease from 0.37 $\mathrm{V^{-1/2}}$ for the poly-Si device to 0.3 $\mathrm{V^{-1/2}}$ for the device with poly-$\mathrm{Si_{0.7}Ge_{0.3}}$ gate and "SiGe" profile, at gate length of 1.0 μm [16].

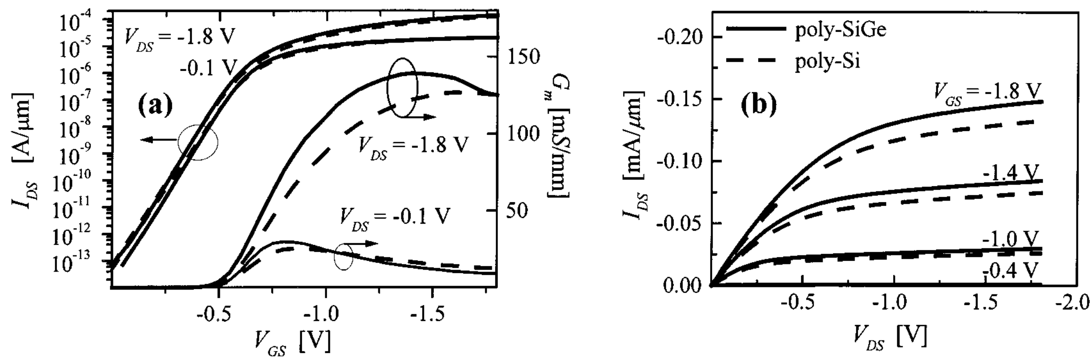

Fig. 4. Typical $I_{\rm DS}$-$V_{\rm GS}$ (a) and $I_{\rm DS}$-$V_{\rm DS}$ (b) characteristics of PMOS transistors with $L_{\rm eff} = 0.18$ μm for poly-Si and poly-Si$_{0.7}$Ge$_{0.3}$ gates. Transconductance ($G_m = \partial I_{\rm DS}/\partial V_{\rm GS}$) is also plotted in (a). Note that for both types of devices the V_T's are the same (both determined by using current criterion (see text), -0.48 V, and from transconductance extrapolation [17], -0.52 V). Because of that, the gate overdrive ($V_{\rm GS} - V_T$) in (b) is the same for both type of devices signifying that $I_{\rm DS}$ is improved intrinsically for poly-SiGe gated devices.

Fig. 4(a) and (b) shows typical transfer and output current–voltage (*I*–*V*) characteristics for poly-Si and poly-Si$_{0.7}$Ge$_{0.3}$ gates for PMOS devices with "default" and "SiGe" channel profiles, respectively. Effective channel lengths, $L_{\rm eff}$, determined by electrical extraction of the source and drain junctions extension under the gate using the MOS MODEL-9 method [17], are 0.18 μm for both devices. It is obvious that there is a significant increase in the drain current for devices with poly-SiGe architecture when compared to the poly-Si ones. At the same time, the long-channel saturation threshold voltages (determined by current criterion 25 nA $\cdot W/L$, where W and L are the effective width and length of the channel) for both type of the devices are measured to be the same (-0.48 V), suggesting that the current drive improvement is caused by an intrinsic improvement in the device performance. In fact, a 15–20% increase in $I_{\rm DS}^{\rm sat}$ is measured for PMOSTs with poly-Si$_{0.7}$Ge$_{0.3}$ for devices gate lengths in the range 10 μm to 0.15 μm. The current increase originates from the higher carrier channel mobility for reduced channel doping. This is clearly illustrated in Fig. 4(a) where channel transconductance G_m is plotted for two drain biases. $G_m^{\rm max}$ is improved from 125 mS/mm for poly-Si device to 140 mS/mm for poly-Si$_{0.7}$Ge$_{0.3}$ device, confirming intrinsic channel mobility improvement. Another noticeable improvement is in the subthreshold characteristics of the devices with poly-Si$_{0.7}$Ge$_{0.3}$. This is reflected in Fig. 5, where the subthreshold swing, S, is plotted against $L_{\rm eff}$. It is clear that $S_{\rm SiGe} < S_{\rm Si}$. This significantly improves the $I_{\rm ON}/I_{\rm OFF}$ ratio, since the decrease of S by 6 mV/dec results in a threefold decrease of the $I_{\rm OFF}$ current for devices with 0.18 μm channel length.

To summarize, 0.18 μm PMOS devices with poly-Si$_{0.7}$Ge$_{0.3}$ gates exhibit improved current drive and channel transconductance, reduced subthreshold swing, leakage currents and body factor. These results show that significant improvements to deep submicron PMOS transistors performance can be achieved by substitution of the poly-Si gates with poly-SiGe ones.

Extensive numerical simulations were carried out in order to estimate the performance improvements that can be achieved for different Ge mole fractions. We have used two-dimensional (2-D) process and device simulators TSUPREM-IV and MINIMOS6 to find the optimum SSR channel profile for the highest possible current drive for a given $I_{\rm OFF}$, Ge mole fractions in 0.18 μm and 0.13 μm PMOS devices, subjected to a full CMOS processing sequence. In the simulations, the SSR dose and energy matrix were varied for a given $\Delta\Phi_{\rm MS}$ value. The experimental results described in this section were used to calibrate simulations. A strong increase in the $I_{\rm ON}$ as compared to standard poly-Si gates is predicted for the same $I_{\rm OFF}$ (Fig. 6), e.g., more than 30% increase for 50% Ge content in the gate for a 0.18 μm generation. It is clear from the analysis that a significant improvement of the PMOS performance can be achieved,

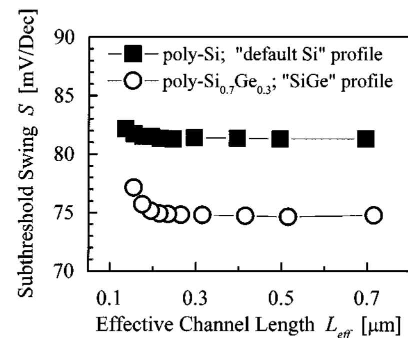

Fig. 5. Subthreshold swing improvement for poly-Si$_{0.7}$Ge$_{0.3}$ gated PMOST's with "SiGe" channel profile.

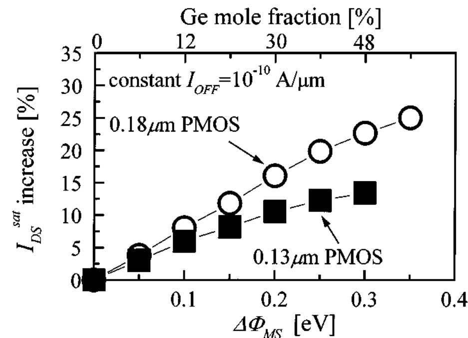

Fig. 6. The results of the 2-D numerical process and device simulations for PMOST's with varying of the Ge content in the poly-SiGe gates for 0.18 μm and 0.13 μm technologies. Dose and energy of SSR implant were optimized to give the maximum $I_{\rm DS}^{\rm sat}$ for constant $I_{\rm OFF}$.

without any degradation of the short-channel behavior of the devices, by consistent engineering of both the gate workfunction and channel profile. We will elaborate on this point in the next section where the experimental results, obtained from CMOS devices designed in such way, are presented.

IV. Full CMOS with Poly-SiGe Gates

A. Experimental Details

In the previous section we have shown that the use of poly-SiGe as a gate material can increase the PMOS performance. However, implementing poly-SiGe gates in full CMOS processing is attractive only if NMOS performance is not sacrificed in any way. It is widely accepted that so-called "double-flavored" poly-gated CMOS is advantageous over a single n- or p-type gated CMOS, since, in the latter case, one of the devices has to be of a "buried" type, with conducting channel situated away from the silicon-oxide interface. The drawbacks of buried channel devices, when used in deep submicrometer gate-length range, have been described previously (see, for example, [18]), and are largely the result of the weaker gate control of the remote channel in these structures. In our approach we only consider surface channel CMOS where both n- and p-type gates are used for NMOS and PMOS, respectively.

This puts some restrictions on the use of high Ge percentage that can be used for the poly-SiGe gated devices. As already mentioned in Section II, the activation as well as deactivation during the back-end processing of the n-type impurities in poly-SiGe gets worse with increase in the Ge mole fraction starting from approximately 20%. Above 50% Ge, the impurity activation is so low that the material becomes virtually unusable as an n-type conductor. Additionally, there are increasing deviations from the standard Si MOS processing regarding gate etching, post-etch oxidation [11] as soon as the Ge mole fraction exceeds 0.5. On the other hand, at 20% Ge in the poly-gate the n-type gate activation properties are at least as good as those of poly-Si [19] and PMOS performance can be significantly improved (see previous section). We have therefore chosen to integrate poly-$Si_{0.8}Ge_{0.2}$ gates into a full 0.18 μm CMOS process.

A full integration of "double-flavored" poly-SiGe gates into the CMOS flow requires self-aligned silicide (salicide) formation to reduce the gate and source/drain parasitic resistances and to ensure a good ohmic contact between the n- and p-type gate electrodes. Ti is used routinely for this purpose to form a low-resistivity $TiSi_2$ compound which is created upon annealing of a thin Ti layer deposited on top of Si. The reaction of Ti with poly-SiGe drastically differs from that of Ti with poly-Si [20]. To achieve a formation of the low-ohmic Ti(Si,Ge) compound the temperatures of the two-step anneal have to be brought down. This creates a problem of high resistance for the Si source/drain regions since the $TiSi_2$ formed at this reduced temperature is not in its low-resistance phase. $TiGe_2$ is much less stable than $TiSi_2$ and readily precipitates Ge atoms which cluster together and break up the low-resistivity layer. Self-alignment of the "salicidation" is also problematic: the etching solution which is meant to remove only non-reacted Ti, also removes the Ti(Si,Ge) phase. It seems therefore that it is extremely difficult to have good silicide-(germanide) both on the source/drain and the gate regions simultaneously.

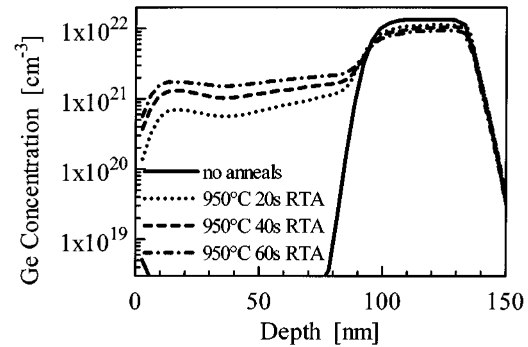

Fig. 7. SIMS profiles of Ge diffusion from the bottom poly-SiGe (50 nm, 32% Ge as deposited) layer into the top poly-Si (90 nm) layer during processing. A logarithmic scale is used for the vertical axis to observe the increase in the "up-diffusion" of Ge.

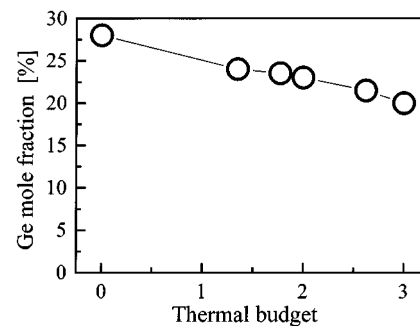

Fig. 8. Ge depletion in the bottom layer of the stacked gates (28% Ge as deposited) with the increase in thermal budget. Ge mole fraction is measured at the interface using combined SIMS and Rutherford back-scattering measurements. One unit of thermal budget corresponds to a 30 s anneal at 950 °C.

To avoid these problems we have used a "stacked-gate" structure consisting of two layers: beneath, a poly-SiGe layer to control the Φ_{MS} of the device, and the top poly-Si layer as a buffer for gate silicidation [21]. In this case the SiGe layer is covered by poly-Si from the top and by oxide spacers from the sides and does not react with Ti at all. The standard salicidation scheme can now be used.

However, the use of buffer poly-Si layer creates another issue which is illustrated in Fig. 7. During the post-gate processing, Ge atoms from the bottom layer diffuse into the top poly-Si thus reducing the Ge content in the bottom layer. The final Ge mole fraction determines Φ_{MS} and must be of known value. Once measured for a given thermal budget (see Fig. 8), it can be used in the controlled consequent device designs [21]. This Ge up-diffusion into the top layer (amounting to $\sim$3% in the top layer after full processing for the starting 32% in the bottom layer) does not influence the salicidation process. The sheet resistances after salicidation of the gate and source/drain are measured to be 15.4 $\Omega/\square$ (6.6 $\Omega/\square$) and 14.6 $\Omega/\square$ (4.5 $\Omega/\square$) for NMOS (PMOS) transistors respectively (as measured on 0.3 μm-wide structures)—equal to those with the standard poly-Si gates.

Apart from the gate formation, all other processing steps of the full 0.18 μm CMOS flow have been reproduced. This features a 4.5 nm-thick gate oxide (determined from *C–V* measurements), e-beam gate lithography, HDD source/drain low-energy implantations, Ti salicidation, etch-back planarization and a single metal level. The SSR channel profile [1] used here was based on the results of numerical simulations and achieved by As ion implantation before the gate oxide growth. The doses and energies were calculated in the optimization loop as described at the end of previous section, and for 20% Ge content were 9×10^{12} cm^{-2} and 200 keV, respectively. The resulting channel profile is shown as "SiGe SSR" trace in Fig. 2.

B. Electrical Results CMOS with Poly-SiGe Gates

We present here the results obtained with poly-Si/$Si_{0.8}Ge_{0.2}$ gates, where the Ge mole fraction was measured by the Rutherford back-scattering (RBS) measurements after full processing. Because of the superior diffusion and electrical activation of the dopants in p-type poly-SiGe compared to poly-Si, the resulting gate activation is excellent: these gates have less than 10% gate depletion after full processing.

Typical *I–V* curves of the transistors with poly-Si/$Si_{0.8}Ge_{0.2}$ gates with $L_G = 0.18\mu$m are presented in Figs. 9 and 10. In the sub-V_T region excellent voltage swing values of 80 mV/dec (PMOST) and 78 mV/dec (NMOST) are obtained ensuring a low level of "off"-state leakage currents (50 pA/μm and 5 pA/μm respectively). The maximum saturation currents for these devices are 240 μA/μm (PMOST) and 455 μA/μm (NMOST). High V_T values (0.42 V) and limited source and drain diffusion under the gates ($\Delta L \sim 10$ nm for NMOST and 30 nm for PMOSTs, MOS MODEL-9 determined [17]) are responsible for somewhat lower values of $I_{\rm DS}^{\rm sat}$ for the NMOST. At the same time, NMOST $I_{\rm ON}/I_{\rm OFF}$ ratios are comparable to the best values reported so far for this generation [22], as demonstrated in Figs. 11 and 12.

It is clear that a careful channel profile engineering (SSR well profile, localized pocket implants around source/drain) ensures that the short-channel effects, represented by the V_T roll-off behavior and the extent of the drain bias influence on the V_T, are well-controlled down to $L_{\rm eff} = 0.12$ μm (Fig. 13).

In Fig. 11 the current drive ($I_{\rm ON}$) of the NMOST is plotted for standard (poly-Si gates) and new (poly-Si/$Si_{0.8}Ge_{0.2}$ gates) technologies showing almost the same behavior. A slight improvement of the current drivability is caused by better n-type gate activation for 20% Ge content [19] while, at the same time, there is a noticeable (~15%) improvement in PMOST performance (Fig. 12). Our PMOS devices also compare favorably to those reported in [22].

We have already addressed the possible influence of poly-SiGe on the gate oxide quality in Section II. In Fig. 14 we present measurements of hot-carrier degradation of transistors with poly-Si/$Si_{0.8}Ge_{0.2}$ gates. Here, a maximum substrate current condition was used for NMOS and $V_{\rm GS} \cong 1/2\ (V_{\rm DS})$ for PMOS transistors, both being the worst stress conditions for the respective devices. For a supply voltage of 1.8 V, the device lifetimes are well beyond the ten-year limit that is conventionally used to characterize the long-term reliability of the process.

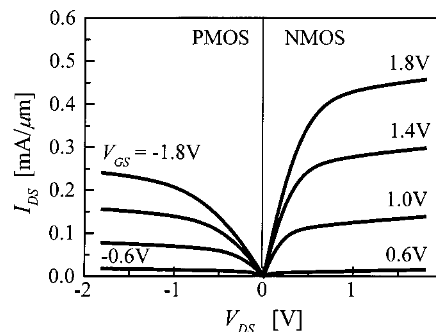

Fig. 9. Typical *I–V* characteristics of NMOS and PMOS transistors with $L_G = 0.18$ μm with poly-Si/$Si_{0.8}Ge_{0.2}$ gates.

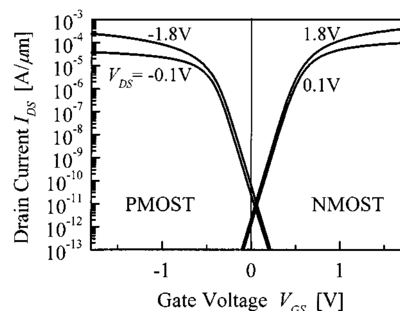

Fig. 10. Typical subthreshold characteristics of NMOS and PMOS transistors with poly-Si/$Si_{0.8}Ge_{0.2}$ gates. $L_G = 0.18$ μm.

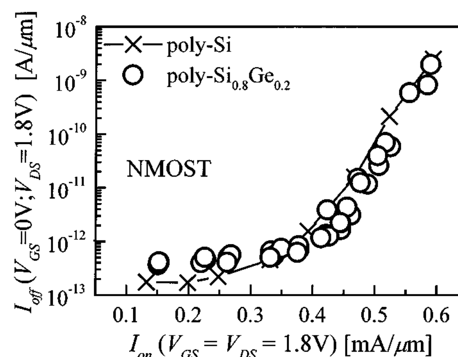

Fig. 11. Current drive against leakage current for NMOS devices with poly-Si/$Si_{0.8}Ge_{0.2}$ gates compared to the standard poly-Si gated transistors values. The CMOS processing with poly-Si/SiGe gates shows as good $I_{\rm ON}/I_{\rm OFF}$ ratios for NMOST's as in the standard technology.

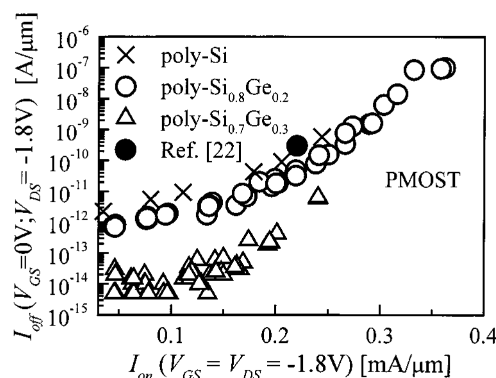

Fig. 12. Current drive against leakage currents for PMOS devices is significantly improved for devices with poly-Si/$Si_{0.8}Ge_{0.2}$ and poly-$Si_{0.8}Ge_{0.2}$ gates.

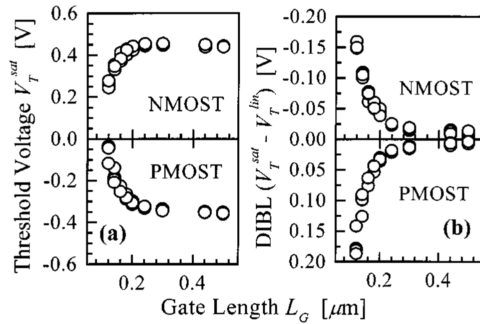

Fig. 13. (a) Saturation V_T ($V_{DS} = -1.8$ V) and (b) drain-induced barrier lowering (DIBL) for NMOS and PMOS transistors with poly-Si/$Si_{0.8}Ge_{0.2}$ gates.

We have presented here the results of the first successful integration of poly-SiGe gates into a full 0.18 μm CMOS process. Complete integration is achieved by using low Ge percentages (<30%). Both n- and p-type high-performance devices are demonstrated for poly-Si/$Si_{0.8}Ge_{0.2}$ gates. Significant improvements are observed for PMOS devices obtained by the controlled coupling of the change in the gate workfunction and the channel doping profile engineering.

V. Discussion

In presenting the experimental data, we have deliberately restricted ourselves to small Ge fraction poly-SiGe gates, mainly because of their relative ease of integration into standard CMOS processes. Let us briefly analyze the influence of the introduction of high Ge percentage gates on the device architecture. As predicted (see Fig. 6), the poly-SiGe gate engineering coupled to the "SSR profiling" scenario works very well for PMOS transistors in the 0.18 μm generation, for Ge fractions up to $\sim$50%. Current increase originates from an effective reduction of the channel doping. Above 50% Ge, the further reduction in the channel doping level results in a strong increase of the short-channel effects which cannot be contained any longer by As implanted SSR. This is also the reason why, for 0.13 μm PMOS devices, the increase in Ge fraction is not accompanied by such a dramatic increase in $I_{\rm DS}^{\rm sat}$, as seen in the 0.18 μm devices. This simple example shows that an extensive PMOS channel redesign might be required to benefit from the use of poly-SiGe with high Ge mole fractions beyond the 0.18 μm CMOS generations.

Another issue, which must be addressed to seriously consider using the poly-SiGe gates in production, is the limitation of the Ge mole fractions to below 0.45 in order to ensure sufficient n-type gate activation. It is highly unlikely that the single p-type gate CMOS is going to be used in production: NMOS devices are generally a technology driver because of the larger electron mobility and sacrificing NMOS performance cannot be tolerated. In order to achieve high performance for both device types, it is therefore most conceivable that n-type poly-Si and p-type poly-SiGe gates would be used for NMOS and PMOS devices respectively. Yet, even the low Ge mole fraction poly-SiGe gates are already an attractive choice for future CMOS technology, since they do not require significant changes to the standard poly-Si processing and can deliver improvement to device performance.

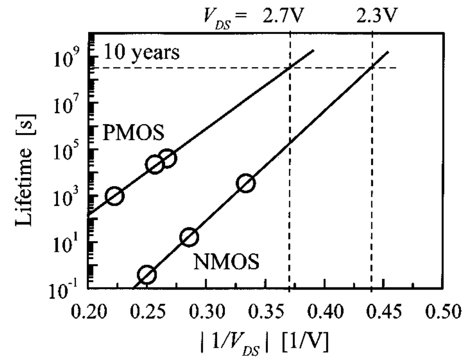

Fig. 14. Lifetime of the MOS transistors with gate oxide stressed under the worst scenarios. The lifetime is estimated from hot carrier degradation measurements where failure is detected when the transconductance changes by 10% under continuous stress. The manufactured devices can be safely operated for ten years at $V_{\rm DD}$ higher than 1.8 V (up to 2.3 V for NMOST and 2.7 V for PMOST).

VI. Conclusion

We have shown that low Ge fraction poly-SiGe can be successfully used in a modern CMOS technological flow. Changing from poly-Si to poly-Si/$Si_{0.7}Ge_{0.3}$ gates in 0.18 μm PMOS transistors yields a 20% increase in current drive and a significant improvement of the subthreshold swing, $I_{\rm ON}/I_{OFF}$ ratio and body factor. We have shown that inclusion of this gate material into the standard CMOS flow delivers a significant improvement to the PMOS device performance, without degrading NMOS devices performance. From analysis of the device parameters and technological issues of integration, we conclude that only Ge mole fractions below $\sim$50% present significant potential as a gate material into a sub-0.18 μm CMOS technologies.

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