Generating *All* Two-MOS-Transistor Amplifiers Leads to New Wide-Band LNAs

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***Abstract*—This paper presents a methodology that systematically generates *all* 2-MOS-transistor wide-band amplifiers, assuming that a MOSFET is exploited as a voltage-controlled current source (VCCS). This leads to new circuits. Their gain and noise factor have been compared to well-known wide-band amplifiers. One of the new circuits appears to have a relatively low noise factor, which is also gain independent. Based on this new circuit, a 50–900 MHz variable-gain wide-band low noise amplifier (LNA) has been designed in 0.35-μm CMOS. Measurements show a noise figure between 4.3 and 4.9 dB for gains from 6 to 11 dB. These values are more than 2 dB lower than the noise figure of the wide-band common-gate LNA for the same input matching, power consumption, and voltage gain. IIP2 and IIP3 are better than 23.5 and 14.5 dBm, respectively, while the LNA drains only 1.5 mA at 3.3 V.**

***Index Terms*—low noise amplifiers, LNAs, systematic generation, variable-gain amplifier, voltage-controlled current source, VCCS, wide-band amplifier.**

I. Introduction

WIDE-BAND low noise amplifiers (LNAs) are used in communication systems where several signal channels are processed simultaneously. For narrow-band LNAs, low noise figure, high gain and impedance matching are obtained at relatively low power consumption exploiting the quality factor of coil-based matching networks [1], [2]. This solution is not practical for wide-band applications requiring more than one decade of bandwidth such as for cable TV networks (i.e., 50–900 MHz bandwidth) due to the complexity of the required wide-band matching networks. In such cases, solutions exploiting the wide-band nature of transistors and resistors are typically used. Wide-band amplifiers in deep-submicron CMOS are attractive in order to enable the realization of low-cost highly integrated systems. Nevertheless, wide-band amplifiers are typically designed in silicon bipolar or GaAs technologies, while little work has been published in CMOS [3], [4].

Designers generally conceive new amplifier circuits exploiting their creativity, intuition, and experience. In contrast, this paper presents a *systematic* approach, which leads to new wide-band CMOS LNA circuits. Specifically, we have developed a methodology that *systematically* generates *all* the wide-band amplifier circuits with two MOS transistors, assuming that a MOSFET is exploited as a voltage controlled current source (VCCS). Important reasons to proceed in this way are:

- Wide-band amplifiers exploit the transconductance g_m of the MOSFET to define small-signal functional properties such as input impedance $Z_{\rm IN}$ and gain. This g_m dependence is essentially accounted for, modeling the small-signal operation of the MOSFET in saturation via a linear VCCS $I = g \cdot \mathrm{V}$ with $g = g_m$ [Fig. 1(a)]. This model is valid over a wide frequency range.
- Widely used textbook wide-band circuits [5] such as the common gate, common source, common drain, and the common source shunt-feedback amplifier stages can be seen as 1VCCS or 2VCCS circuits. They are used as simple wide-band LNAs or as building blocks for the construction of larger wide-band LNAs.

The aim of this paper is to answer the question, are there other useful two-MOS-transistor wide-band amplifiers than the well-known 1VCCS and 2VCCS circuits mentioned above? To find the answer, we have developed a systematic methodology generating *all* the wide-band amplifiers with 2VCCSs.

The paper is organized as follows. In Sections II and III, the systematic generation methodology is presented. Section IV deals with a comparison of the gain and noise performance of the generated amplifiers. The amplifier with the best noise performance is then selected and Section V presents the design of a wide-band LNA. Section VI deals with the measurements and in Section VII, conclusions are given.

II. The Systematic Approach

Our aim to find new wide-band LNA circuit topologies is pursued generating *all* the amplifier circuits with two MOS transistors. However, even if a MOSFET is considered as a three-terminal device (i.e., neglecting the bulk), many different two-port circuits with two transistors are possible! To manage this complexity, a systematic generation methodology has been conceived, which consists of two main parts:

1) *Generate All 2VCCS graphs*. A MOS transistor in saturation is modeled as a linear VCCS with a graph representation given by a v and i branch [Fig. 1(a)]. Graph theory is then applied to find *all* possible circuit topologies. Using a symbolic analysis program, *all* the graphs of two-port circuits with 2VCCSs (i.e., VCCS$_a$ and VCCS$_b$ with transconductances g_a and g_b) are generated and analyzed. This leads to 145 potentially useful cases: the 2VCCS graph database [Fig. 1(b)]. Linear two-ports of

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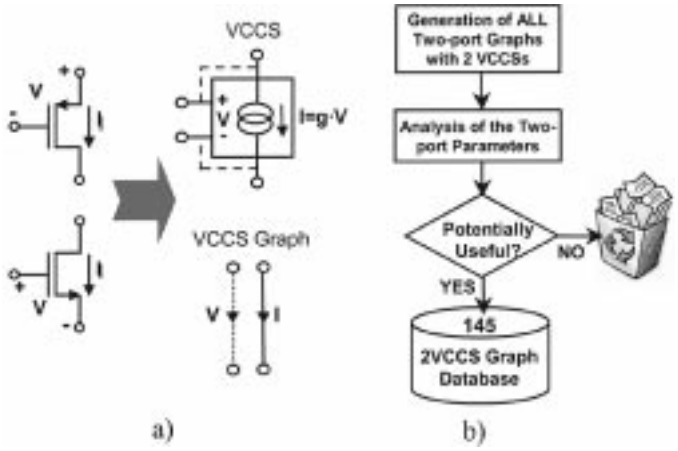

Fig. 1. (a) A MOSFET in saturation can be modeled as a linear VCCS. The topological properties of a VCCS can be represented by a graph with a v and i branch. (b) All potentially useful graphs of two-port circuits with 2VCCS have been generated (i.e., the 2VCCS graph database) [6], [7].

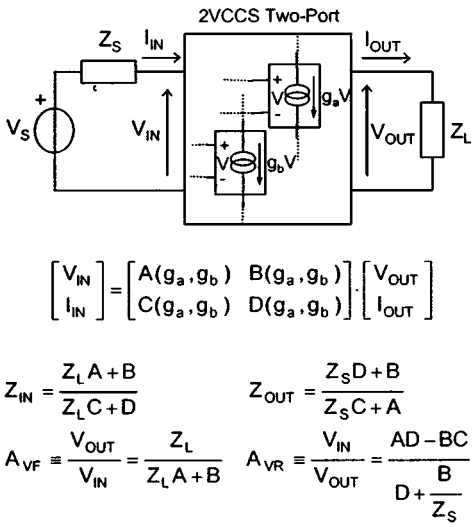

Fig. 2. A 2VCCS circuit as linear two-port described by $\{A, B, C, D\}$ parameters, which are function of the transconductances g_a and g_b of the 2VCCS. Two-port equations using $\{A, B, C, D\}$ parameters are also shown.

2VCCS graphs are described in terms of $\{A, B, C, D\}$ transmission parameters (see their definitions in Fig. 2).

2) *Select two-MOS-transistor wide-band amplifiers*. Graphs of 2VCCS circuits that functionally act as wide-band amplifiers are selected. Graphs that can be implemented as two-transistor circuits are ultimately considered.

The first part of this methodology is presented elsewhere [6], [7]. In this paper, the second part concerning the amplifier selection and design is presented.

III. Selection of Two-MOS-Transistor Amplifiers

The *functional* behavior (e.g.: $Z_{\rm IN}, Z_{\rm OUT}$, and $A_{\rm VF}$) of a linear two-port circuit is univocally defined if its two-port parameters and the source impedance Z_S and load impedance Z_L are known [Fig. 3(a)]. We select graphs of 2VCCS wide-band amplifiers reversing this chain of reasoning, that is [Fig. 3(b)]: upon assigned Z_S and Z_L, we first define the *functional*

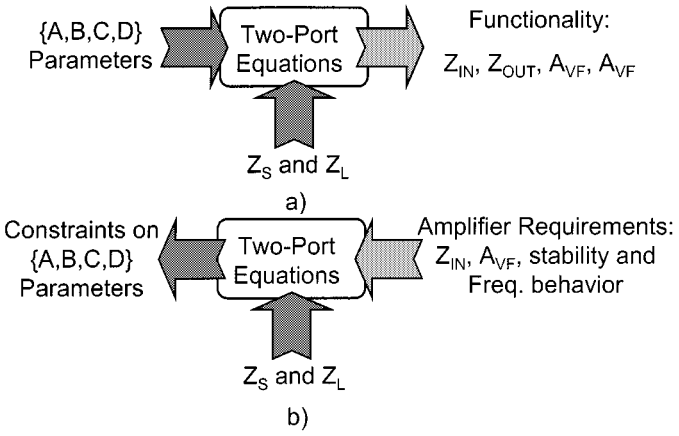

Fig. 3. (a) Two-ports parameters plus Z_S and Z_L define the functionality of a two-port. (b) The reverse reasoning is used for the systematic selection of wide-band amplifiers with two MOS transistors.

requirements of a wide-band amplifier. Then constraints on the $\{A, B, C, D\}$ parameters of 2VCCS two-ports are derived, which are used as selection criteria. Graphs of wide-band amplifiers are ultimately implemented as MOS transistor circuits. This concept is implemented in a four-step procedure. To do so, we have assumed a real source impedance $Z_S = R_S$ as we were interested in cable-modem-like LNA applications and a capacitive on-chip load impedance $Z_L = 1/(s \cdot C_L)$ (mixer input capacitance for a zero-IF receiver). In the next sections, each step of this procedure is discussed.

A. STEP1: Amplifier Functional Requirements

The following functional requirements are found important for a wide-band amplifier:

- *Forward gain* $(A_{\rm VF})$. A forward voltage gain $|A_{\rm VF}|>1$ is needed to boost weak input signals above the noise floor of the following stage.
- *Input impedance* $(Z_{\rm IN})$. Source impedance matching $Z_{\rm IN} = R_S$ is required to avoid signal reflections terminating the input coaxial cable.
- *Stability*. In RF/microwave designs, stability is typically required unconditional [8]. The latter means a stable amplifier for any value of passive source and load impedance.
- *Frequency behavior*. A two-port is assumed wide band if its transfer functions are frequency independent for more than one decade of frequencies (e.g.: 50–900 MHz for a cable TV network).

B. STEP2: Constraints on $\{A, B, C, D\}$ Parameters

The above requirements are translated into constraints on the $\{A, B, C, D\}$ parameters.

1) Useful Combinations of $\{A, B, C, D\}$*:* Useful combinations of two-port parameters are obtained studying the dependence of $Z_{\rm IN}$ and $A_{\rm VF}$ as a function of the $\{A, B, C, B\}$ parameters and Z_L. The aim is to obtain impedance matching and voltage gain over a wide range of frequencies. According to the $Z_{\rm IN}$ expression in Fig. 2, at least two nonzero transmission parameters are necessary to provide a $Z_{\rm IN}$ different from $\{\infty, 0\}$. This corresponds to nine combinations of transmission parameters, namely,

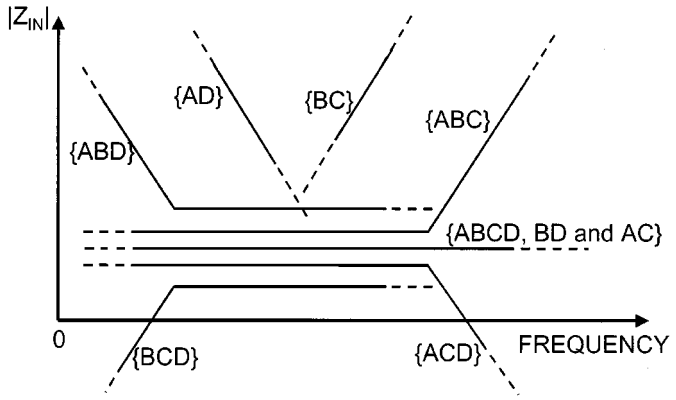

Fig. 4. Qualitative behavior of $|Z_{\rm IN}|$ versus frequency for different combinations of two-port parameters, assuming $Z_L = 1/(j\omega C_L)$.

$\{AC, AD, BD, BC, ABC, ABD, ACD, BCD, ABCD\}$, where the letters refer to nonzero transmission parameters (for instance $\{AD\}$ refers to a two-port with parameters $\{A, 0, 0, D\}$). Fig. 4 shows the qualitative behavior of $Z_{\rm IN}$ versus frequency for the cases selected above assuming $Z_L = 1/(j\omega C_L)$.

Clearly, the strong frequency dependence of $Z_{\rm IN}$ hampers a wide-band impedance matching for cases $\{AD\}$ and $\{BC\}$. For the other cases $\{AC, BD, ABC, ABD, ACD, BCD, ABCD\}$, a wide range of frequencies exists where $Z_{\rm IN}$ is real and can be matched to the source R_S. However, cases $\{BD\}$ and $\{BCD\}$ show a frequency dependent gain $A_{\rm VF} = 1/(B \cdot j\omega C_L)$, while case $\{ABD\}$ cannot simultaneously provide a wide-band $Z_{\rm IN}$ (i.e., requires $|A \cdot Z_L| \ll |B|$) and $A_{\rm VF}$ (i.e., requires $|A \cdot Z_L| \gg |B|$). Concluding, the defined wide-band amplifiers are two-ports with transmission parameters: $\{AC, ABC, ACD, ABCD\}$.

2) Value of $\{A, B, C, D\}$: The forward gain $A_{\rm VF}$ of a two-port driving a capacitive load $Z_L = 1/(j\omega C_L)$ can be written as

$$|A_{\rm VF}| = \frac{1}{|A + j\omega C_L B|} \leq \frac{1}{|A|} \quad \forall\omega. \tag{1}$$

From (1), $|A_{\rm VF}|$ is larger than 1 if $|A|<1$.

Conditions for the unconditional stability of a two-port network are [9]:

$$\Re\{Z_{\rm IN}\} \geq 0 \quad \text{and} \quad \Re\{Z_{22}\} \geq 0, \quad \forall Z_L \quad \text{and} \quad \forall\omega \tag{2}$$

where $\Re\{\cdot\}$ is the real part and Z_{22} is an impedance parameter of the two-port. Using $\{A, B, C, D\}$ parameters and for $Z_L = 1/(j\omega C_L)$, (2) leads to

$$\Re\{Z_{\rm IN}\} = \frac{A \cdot C + D \cdot B \cdot \omega^2 C_L^2}{C^2 + D^2 \cdot \omega^2 C_L^2} \geq 0, \quad \forall C_L \quad \text{and} \quad \forall\omega$$
$$\Re\{Z_{22}\} = \frac{D}{C} \geq 0. \tag{3}$$

It can be verified that to satisfy (3), it is necessary and sufficient to require $\{A, B, C, D\}$ parameters to have all the same sign.

C. STEP3: 2VCCS Graphs Selection

Graphs of 2VCCS wide-band amplifiers are now selected using the constraints on the $\{A, B, C, D\}$ parameters derived so far. This is done checking the availability of the desired two-port circuits within the 2VCCS database. However, only graphs that can be implemented as two-MOS-transistor circuits are ultimately considered. This means that only 2VCCS graphs using VCCSs with three terminals are considered. Starting from an initial set of 145 2VCCS graphs, 19 graphs corresponding to cases $\{ACD, ABC, ABCD\}$ are found while no $\{AC\}$ cases are present in this database. However, ultimately only one $\{ABC\}$ and three $\{ABCD\}$ cases fulfill all the requirements. Fig. 5(a) shows their representation in terms of VCCSs.

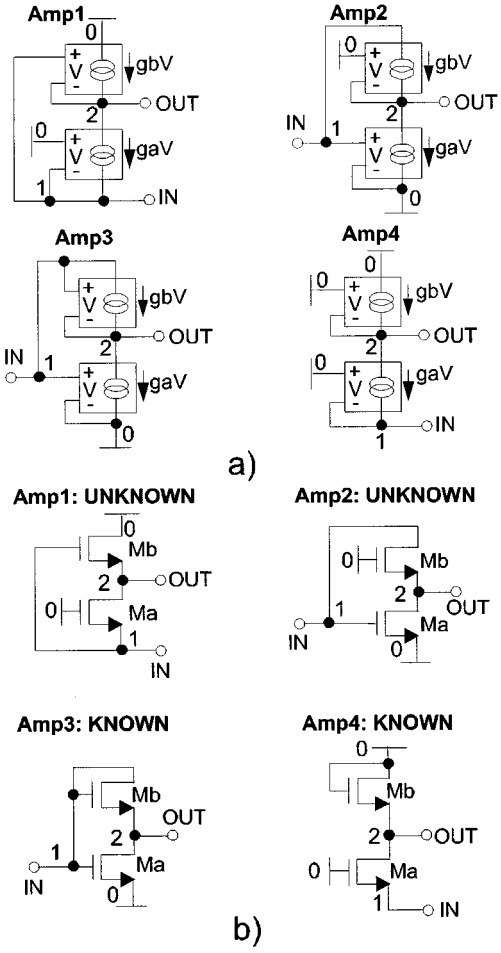

Fig. 5. Four generated wide-band amplifiers represented in terms of (a) VCCSs and (b) transistors.

D. STEP4: Transistor Circuit Implementation

The graphs of 2VCCS wide-band amplifiers are now implemented as follows. 1) VCCSs are replaced with nMOS transistors because they are faster than pMOS transistors. 2) Circuit arrangements that re-use dc currents are chosen to minimize the number of bias sources. This lowers power consumption or reduces the performance degradation due to bias circuitry (e.g., bias noise).

IV. Comparison of the Generated Amplifiers

The four generated wide-band amplifiers are shown in Fig. 5(b) (biasing not shown). Next to well-known wide-band amplifiers such as the common gate (Amp4) and the shunt feed-

TABLE I
AMPLIFIER'S SMALL SIGNAL PARAMETERS

Case	Z_{IN}	Z_{OUT}	A_{VF}	A_{VR}
Amp1	$1/g_a$	$1/g_b$	$1+g_a/g_b$	0
Amp2	$1/g_a$	$1/g_b$	$-g_a/g_b$	g_bR_S
Amp3	$1/g_a$	$(R_b+R_S)/(1+g_aR_S)$	$1-g_aR_b$	$g_bR_S/(g_aR_S+1)$
Amp4	$1/g_a$	R_b	g_aR_b	0

TABLE II
AMPLIFIER'S NOISE FACTOR ($\mathrm{NEF} = \mathrm{NEF}_a - \mathrm{NEF}_b$)

Case	Noise Factor F
Amp1	$1+\mathrm{NEF}_b+4\mathrm{NEF}_b/\lvert A_{VF}\rvert+2/\lvert A_{VF}\rvert^2$
Amp2	$1+\mathrm{NEF}_a+4\mathrm{NEF}_a/\lvert A_{VF}\rvert$
Amp3	$1+\mathrm{NEF}_a(2+\lvert A_{VF}\rvert)^2/\lvert A_{VF}\rvert^2+4\mathrm{NEF}_b(1+\lvert A_{VF}\rvert)/\lvert A_{VF}\rvert^2$
Amp4	$1+\mathrm{NEF}_a+4\mathrm{NEF}_b/\lvert A_{VF}\rvert$

back common source (Amp3) amplifiers, two other wide-band amplifiers (Amp1 and Amp2) are found. The latter, as far we know, are new two-MOS-transistors circuits. Nevertheless, Amp1 and Amp2 are related to Amp4 and Amp3, respectively. Amp1 can be derived from Amp4 if the $+$ terminal of VCCS_b is disconnected from the node (0) and connected to the node (1). Amp2 is obtained from Amp3 if the $+$ terminal of VCCS_b is disconnected from the node (1) and connected to the node (0). An important question now arises: Do these changes in the interconnection of VCCS_b lead to circuits that also have a better performance? To answer this question, we compare the small signal parameters and noise factor F of Amp1 versus Amp4 and Amp2 versus Amp3. For a first order estimation of the performance only the signal path is considered while a simplified modeling of the MOS transistors with VCCSs is used. This means that parasitic effects such as MOS output conductance g_d, body transconductances g_{mb}, and capacitances are neglected. This is because the node impedance of the generated wide-band amplifiers is dominated by the MOS gate transconductance g_m and the relation $g_m > \max\{g_{\mathrm{mb}}, g_d\}$ typically holds. Moreover, due to the low node impedance ($\propto 1/\mathrm{gm}$), the effect of capacitances can be neglected up to relatively high frequencies. As a final note on modeling, we state that narrow-band coils-based amplifiers are typically more sensitive to inaccuracies in the device modeling respect to the wide-band counterpart. This is because energy storing/dissipating parasitic elements decrease the quality factor Q of matching networks and shift the resonance frequency (reactive parasitic), strongly affecting the performance.

A. Small Signal Parameters: $Z_{\mathrm{IN}}, Z_{\mathrm{OUT}}, A_{\mathrm{VF}}$ and A_{VR}

In Table I, the small-signal parameters of the 4 wide-band amplifiers are shown as a function of the g_a and g_b. As far as $Z_{\mathrm{IN}}, A_{\mathrm{VR}}$ and Z_{OUT} are concerned, there is no basic difference between Amp1 and Amp4 (for $R_b = 1/g_b$). However, for Amp1 the voltage gain $A_{\mathrm{VF}} = A_{\mathrm{VF},1} + A_{\mathrm{VF},2}$ is the superposition of the gain of two sub-stages connected in feed-forward: a common gate stage Ma-Mb with gain $A_{\mathrm{VF},1} = g_a/g_b$ and a source follower stage Mb with gain $A_{\mathrm{VF},2} = 1$. This extra gain contribution, allows Amp1 to easily provide gain higher than 1. Amp2 provides a somewhat increased forward gain with respect to Amp3. Both circuits have a reverse gain in the order of $1/A_{\mathrm{VF}}$[1]. This may not be enough for applications requiring high isolation between the local oscillator and the LNA input. In this case, A_{VR} can be decreased cascading a second stage.

[1]$|A_{\mathrm{VR}}A_{\mathrm{VF}}| = 1$ can be obtained also using an ideal passive $1:n$ step-up transformer. However, practical implementations of on-chip wide-band transformers (e.g.: 50–900 MHz for cable TV modems) on standard CMOS processes suffer for relatively poor performance.

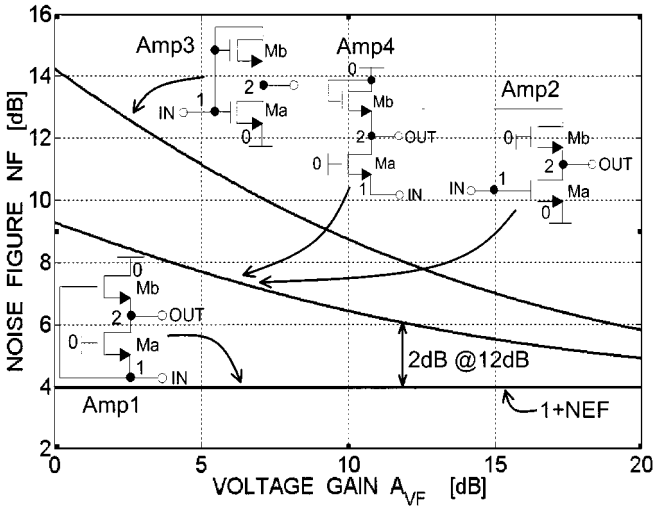

Fig. 6. Noise figure versus gain A_{VF} for the generated amplifiers upon input matching ($\mathrm{NEF}_a = \mathrm{NEF}_b = 1.5$).

B. Noise Figure

To analyze the noise figure (NF) of the amplifiers, a model for the thermal noise of the VCCS is needed. This is done placing a noise current source in parallel to the output port of the VCCS with a power spectral density $I_{n,x}^2/\Delta f$:

$$\frac{\overline{I_{n,x}^2}}{\Delta f} = 4kT \cdot \mathrm{NEF} \cdot g_x \tag{4}$$

where $g_x \in \{g_a, g_b\}$ and NEF is the noise excess factor of VCCS_x (i.e., the noise (4) divided by the noise current of a resistor with $R = 1/g_x$). For instance, if the VCCS is a deep-submicron MOS transistor, then $g = g_m$ and $\mathrm{NEF} = \gamma \cdot (g_{d0}/g_m) > \gamma > 1$ [10] holds, where γ and g_{d0} have the usual meaning.

The noise factor F of the four amplifiers is shown in Table II as a function of the gain A_{VF} upon input matching: $Z_{\mathrm{IN}} = R_S$. For all the amplifiers, F is limited to $1+\mathrm{NEF}_{a(b)}$ (i.e., for $|A_{\mathrm{VF}}|$ infinitely large). This occurs because the input matching $Z_{\mathrm{IN}} = R_S$ requirement imposes the transconductance g_a of the input VCCS to be equal to $1/R_S$. This limits the output signal-to-noise ratio (SNR) and so F. Nevertheless, differences among the amplifiers arise from the way this limit can be reached. This is shown in Fig. 6, where the noise figure $\mathrm{NF} = 10\log_{10}(F)$ is plotted versus the forward gain A_{VF} upon input matching $Z_{\mathrm{IN}} = R_S$ having assumed that $\mathrm{NEF}_a = \mathrm{NEF}_b = \mathrm{NEF} = 1.5$[2].

[2]Since NEF is bias dependent via both γ and the ratio g_{d0}/g_m, the identity $\mathrm{NEF}_a = \mathrm{NEF}_b = 1.5$ is an approximation.

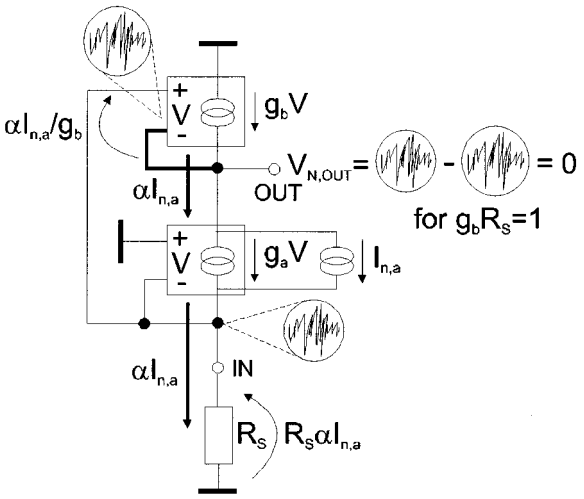

Fig. 7. Path of the noise current associated with VCCS$_a$ in Amp1: output noise voltage cancellation occurs for $g_b R_S = 1$.

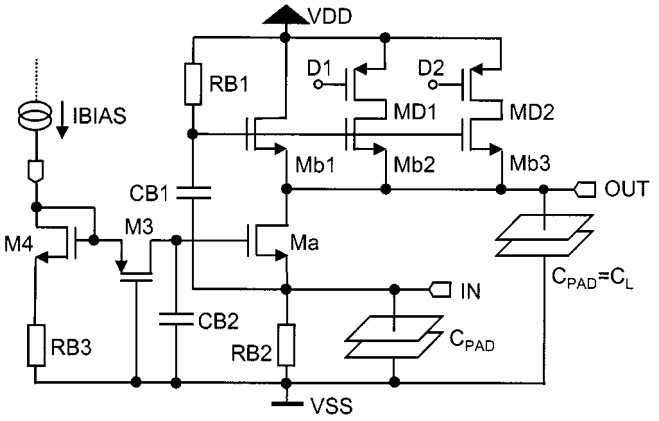

Fig. 8. A 50–900 MHz variable-gain wide-band LNA based on Amp1. The load is the on-chip bond pad capacitance $C_{\rm PAD}$.

We see that Amp2 has a better NF than Amp3. More interestingly, the NF of Amp1 is significantly lower than in all the other cases (i.e., more than 2 dB lower up to $A_{\rm VF} = 12$ dB) and it is *constant*. This behavior is uncommon for low noise amplifiers, which typically show a rather steep increase in NF for decreasing $A_{\rm VF}$. To understand this behavior we look at the NF of Amp1 in detail. The (spot) noise factor F of a linear two-port is related to its output noise power spectral density $V^2_{n,\rm OUT}/\Delta f$ and the gain $A_{\rm VF}$ as [2]

$$F = 1 + \frac{\overline{\frac{V^2_{n,\rm OUT}}{\Delta f}}}{\overline{\frac{V^2_{n,\rm RS}}{\Delta f}} \cdot \frac{A^2_{\rm VF}}{\left(1+\frac{R_S}{Z_{\rm IN}}\right)^2}}. \tag{5}$$

Equation (5) can be rewritten as

$$F = 1 + \frac{\overline{\frac{V^2_{n,\rm EQ,IN}}{\Delta f}}}{\overline{\frac{V^2_{n,\rm RS}}{\Delta f}}} \tag{6a}$$

$$\frac{V^2_{n,\rm EQ,IN}}{\Delta f} \equiv \frac{\left(1+\frac{R_S}{Z_{\rm IN}}\right)^2 \cdot \overline{\frac{V^2_{n,\rm OUT}}{\Delta f}}}{A^2_{\rm VF}} \tag{6b}$$

where F-1 can now be interpreted as the ratio between the equivalent input noise $V^2_{n,\rm EQ.,IN}$ of the two-port and the noise of the source $V^2_{n,\rm RS}$. For Amp1, the output noise power spectral density is

$$\overline{\frac{V^2_{n,\rm OUT}}{\Delta f}} = \frac{1}{g_b^2} \cdot \left[\overline{\frac{I^2_{n,b}}{\Delta f}} + \overline{\frac{I^2_{n,a}}{\Delta f}} \cdot \frac{(g_b R_S - 1)^2}{(g_a R_S + 1)^2}\right]. \tag{7}$$

Interestingly, for $g_b R_S = 1$ there is no output noise contribution coming from input device VCCS$_a$, regardless the value of $Z_{\rm IN}$! This noise cancellation mechanism can be better understood if one look at the path of the instantaneous noise current coming out from VCCS$_a$ as shown in Fig. 7.

Depending on the value of g_a and the source impedance R_S, an instantaneous noise current $I_{n,a} \cdot \alpha = I_{n,a}/(1 + g_a R_S)$ flows out from VCCS$_a$. This current produces two *fully correlated* noise voltages $R_S \alpha I_{n,a}$ and $\alpha I_{n,a}/g_b$ respectively across the source resistor R_S and the input voltage port of VCCS$_b$ (see Fig. 7). Since the output noise voltage $V_{n,\rm out}$ is equal to the instantaneous difference between $R_S \alpha I_{n,a}$ and $\alpha I_{n,a}/g_b$, exact *cancellation* of the output noise due to VCCS$_a$ $V_{n,\rm out} = \alpha I_{n,a}(R_S - 1/g_b)$ occurs for $g_b R_S = 1$. In this case, using (5), the noise factor F of the amplifier is easily shown to be equal to $1 + \rm NEF_b$.

Changing now the value of g_b (and so the forward gain $A_{\rm VF}$) one would expect the F of Amp1 to vary too. However, for $\rm NEF_a = NEF_b = NEF$ and upon input matching $Z_{\rm IN} = R_S$, (7) can be rewritten as

$$\overline{\frac{V^2_{n,\rm OUT}}{\Delta f}} = \frac{\rm NEF}{4} \cdot \overline{\frac{V^2_{n,\rm RS}}{\Delta f}} \cdot A^2_{\rm VF}. \tag{8}$$

Equation (8) says that the output noise power of Amp1 is proportional to $A^2_{\rm VF}$. Using (6b) upon $Z_{\rm IN} = R_S$, we find that F is equal to $1+\rm NEF$ for any value of g_b (i.e., any value of $A_{\rm VF}$).

It is because of this better noise factor compared to the other amplifiers that we have selected Amp1 for a silicon realization. In the next section, the design of a wide-band LNA based on Amp1 is discussed.

V. Design of a Wideband CMOS LNA

LNAs are nearly always found in any receiving systems where high sensitivity needs to be achieved. In such systems, wide-band LNAs with variable gain may be desirable in order to relax the linearity requirements of the following (active and so inherently noisy) mixer circuit. Moreover, there are applications where only a little increase in noise figure is acceptable at low gain in order to preserve the signal-to-noise-plus-distortion ratio (e.g.: [11]).

The new amplifier topology Amp1 represents a possible option if a noise factor in the order of $1+\rm NEF$ is acceptable. This is typically the case of a cable modem like application where a noise figure between 4–6 dB is found. In Fig. 8, the schematic of a variable gain 50–900 MHz wide-band CMOS LNA based on Amp1 is shown.

This LNA is designed to match a 75-Ω source while driving an on-chip capacitive load C_L of about 0.3 pF. For the test chip,

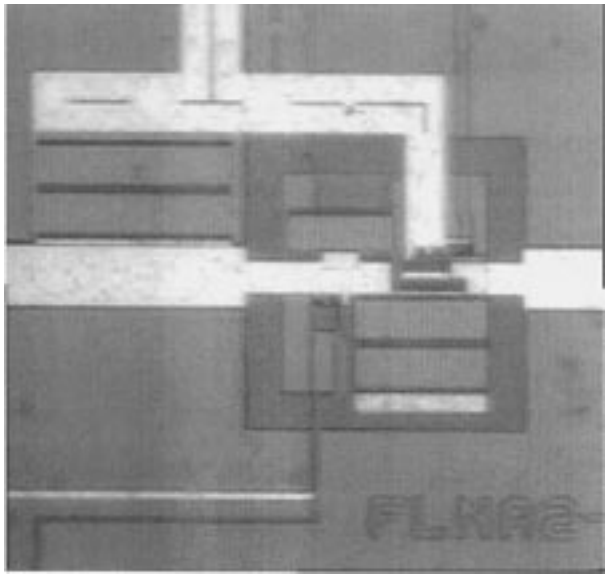

Fig. 9. Chip photo of the wide-band CMOS LNA.

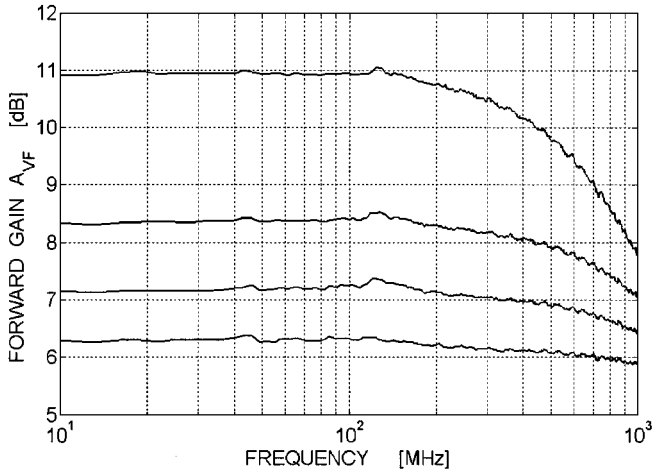

Fig. 10. Forward gain $A_{\rm VF}$ versus frequency.

the capacitance of the output bond pad $C_{\rm PAD}$ has been used. Variable voltage gain from 6 to 12 dB is obtained changing the width of transistor M_{b1} in four discrete steps using transistors M_{b2} and M_{b3}. This is done placing two pMOS switches M_{D1} and M_{D2} in series to the drains of M_{b2} and M_{b3}. These switches do not degrade the LNA performance being out of the RF signal path. The gates of transistors $M_{b1,2,3}$ are ac coupled to the RF input node by a simple C-R (C_{B1}-R_{B1}) high-pass filter with a +3-dB corner frequency much lower than 50 MHz. This allows also to set the dc voltage at the gates of $M_{b1,2,3}$ to $V_{\rm DD}$. From the biasing point of view, transistors M_4, M_a and resistors R_{B2}, R_{B3} operate as a current mirror, driven by an external source. Within the frequency band of interest, capacitance C_{B2} shunts the gate of M_a to $V_{\rm SS}$ while M_3 further decouples M_a from the biasing node. To save area, C_{B1} and C_{B2} are realized with MOS transistors.

The noise factor $F_{\rm LNA}$ of Amp1 can be written as

$$F_{\rm LNA} = F + (F_{\rm EXTRA} - 1) \tag{9}$$

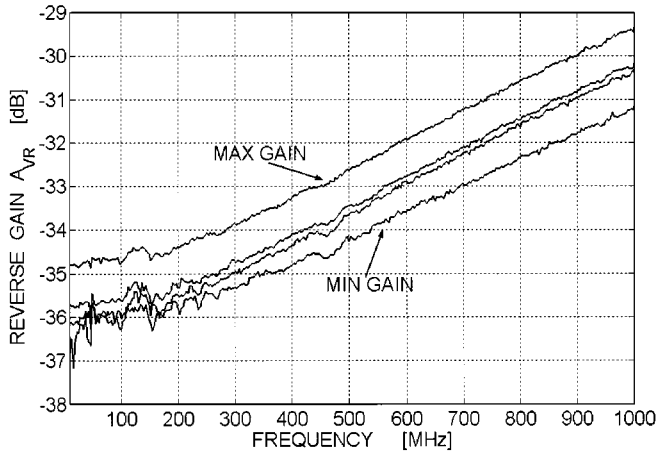

Fig. 11. Reverse gain $A_{\rm VR}$ versus frequency.

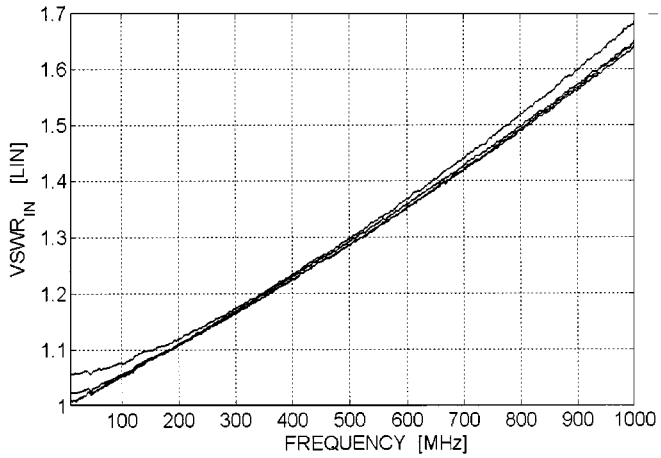

Fig. 12. $\rm VSWR_{IN}$ versus frequency.

where F is the NF of Amp1 as given in Table II while $F_{\rm EXTRA}$ accounts for the remaining independent thermal noise sources associated with the distributed poly-gate resistance of the MOS, the substrate resistance and the biasing devices. The distributed gate resistance can be minimized using a multifinger layout structure with the gate contacted at both the sides [12] while the effective resistance between the body of the nMOS and the external ground is reduced using a many substrate contacts near the device [1]. The bias circuitry has a less negligible impact on the overall noise factor $F_{\rm LNA}$. Specifically, R_{B1} and R_{B2} are the main contributors. For $R_{B1,2} \gg \max\{R_S/2, 1/(4g_b)\}$, neglecting other capacitances, $F_{\rm EXTRA}$ becomes

$$F_{\rm EXTRA} \approx 1 + \frac{R_S}{R_{B2}} + \frac{4R_{B1}}{R_S(A_{\rm VF}-1)^2} \cdot \frac{1+\omega^2 \frac{C_{B1}^2 A_{\rm VF}^2}{4g_b^2(A_{\rm VF}-1)^2}}{1+\omega^2 \frac{C_{B1}^2 R_{B1}^2 A_{\rm VF}^2}{(A_{\rm VF}-1)^2}}.$$

The first term represents the effect of the current mirror M_4, M_a, R_{B2}, R_{B3} assuming that C_{B2} effectively shunts the gate of M_a to $V_{\rm SS}$. It can be made small for $R_{B2} \gg R_S$. However, for $R_S = 75\,\Omega$ and a dc current of about 1.5 mA, the voltage across R_{B2} easily becomes large. As a compromise, $R_{B2} = 750\,\Omega$ is chosen, which limits the increase in noise factor to 0.1 while keeping enough voltage headroom for the circuit. The second term is associated with the noise of R_{B1}

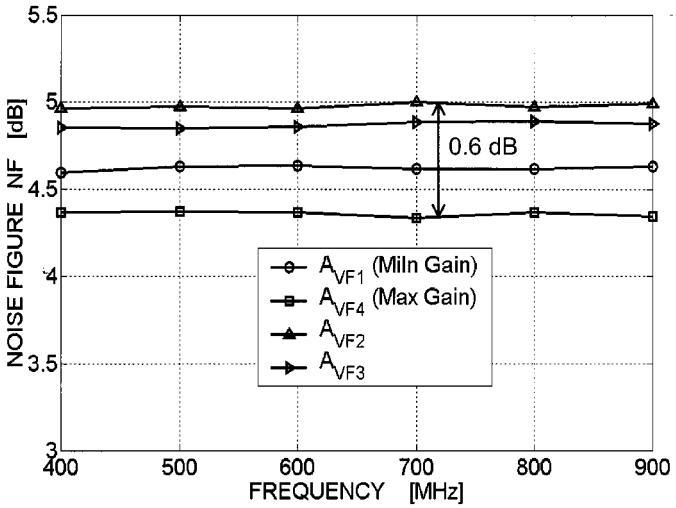

Fig. 13. NF versus frequency for different gain settings.

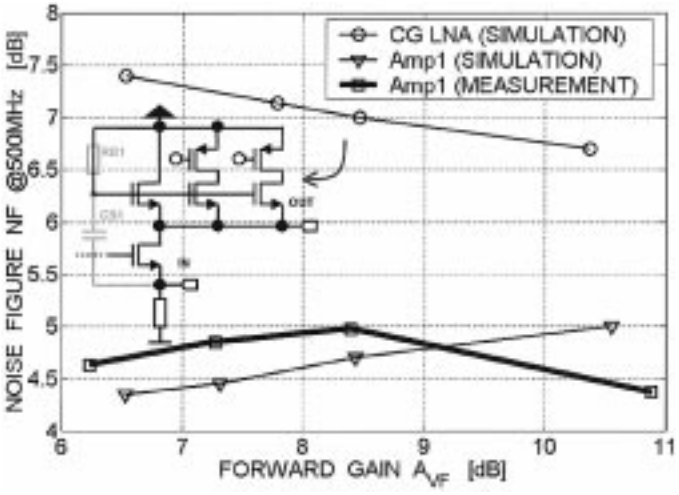

Fig. 14. NF at 500 MHz versus $A_{\rm VF}$ for Amp1 (both measured and simulated using MOS model 9) and a common-gate (CG) LNA obtained form Amp1 connecting the gate of $M_{b1,2,3}$ to $V_{\rm DD}$ and resizing them for the same gain. All the curves are referred to 50 Ω.

and prevalently degrades the NF at low/medium frequencies. Therefore, $C_{B1} = 2$ pF and $R_{B1} = 100$ KΩ have been chosen to achieve a good compromise between the reduction of the F in the low side of the frequency band, area consumption and the increase of F at high frequencies due the parasitic backplate of C_{B1} (between the input node to $V_{\rm SS}$).

VI. Measurements

The LNA has been realized in a 0.35-μm CMOS. In Fig. 9, the chip photo is shown. The LNA forward gain $A_{\rm VF}$, reverse gain $A_{\rm VR}$, and input VSWR$_{\rm IN}$ are shown in Figs. 10, 11, and 12, respectively. They were obtained from on-wafer measurements of S parameters.

Forward gain $A_{\rm VF}$ varies in four steps from 6.2 to 11 dB while the worst-case -3 dB bandwidth (i.e., maximum gain) is somewhat above 900 MHz and is mainly limited by the (dominant) output pole (i.e., $R_{\rm OUT}$ is about 240 Ω). Reverse gain $A_{\rm VR}$ is better than -30 dB over the whole band. At low frequency, $A_{\rm VR}$ is limited by the finite output conductance of M_a. At high frequencies, the gate–source capacitance of $M_{b1,2,3}$ creates a parasitic path to the input node that increases $A_{\rm VR}$. The input voltage standing wave ratio VSWR$_{\rm IN}$ is less than 1.6 over the whole band.

The noise figure measurement requires more care. The LNA is designed to match a 75-Ω source while driving a capacitive load. To measure the LNA noise figure (with HP8970B), two problems are faced. First, standard 50-Ω interfaces for the LNA are required. This is particularly important at the LNA output where the impedance can be as large as 240 Ω. Thus, a microwave tuner is used to match the LNA output to 50 Ω for each gain step and frequency point. At the LNA input, we do accept the relatively small mismatch $Z_{\rm IN} = 75\ \Omega$. Second, it can be easily shown that the available power gain $G_{\rm av,LNA}$ barely exceeds 0 dB. This leads to a sensitivity problem in the NF meter as the accuracy relation $\rm NF_{LNA} + G_{av,LNA} > 5\ dB + NF_{METER}$ is not fulfilled [13]. This problem is solved placing a wide-band LNA (Mini-Circuits ZFL-1000LN) behind the tuner. Using this measurement setup and after accounting for both the tuner and PCB losses, the noise figure of Amp1 has been extracted from measurements (Fig. 13) for frequencies from 400 to 900 MHz

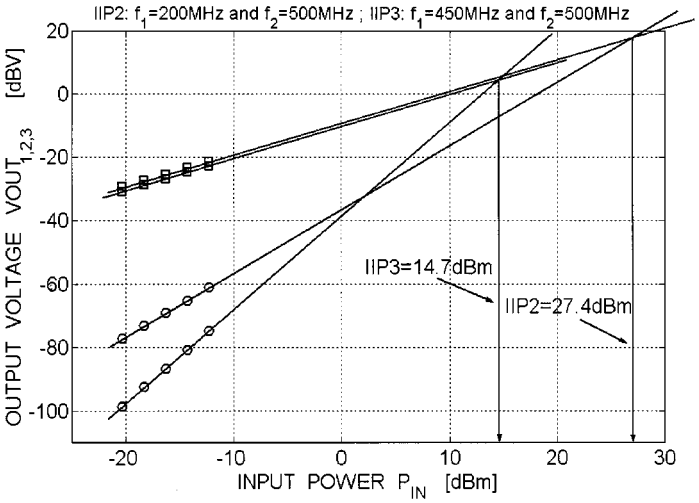

Fig. 15. IIP2 and IIP3 for maximum gain.

(the frequency limitation is due to the availability of only a high-frequency tuner).

Clearly, a relatively constant NF between 4.3 and 4.9 dB is observed for all gain settings. Residual variations of NF are attributed to the impedance mismatch at the LNA input,[3] body effect, and the bias dependence of γ[4]. Fig. 14 shows the NF of Amp1 at 500 MHz (both measured and simulated values) versus the gain $A_{\rm VF}$ together with the simulated NF of a common-gate (CG) LNA.

The wide-band CG LNA has been obtained from Amp1 in Fig. 8, connecting the gate of transistors $M_{b1,2,3}$ to $V_{\rm DD}$ and resizing them in order to obtain the same $A_{\rm VF}$. In good agreement

[3] F is constant for $Z_{\rm IN} = R_S$, which is not the case for our measurement setup ($Z_S = 50\ \Omega$ and $Z_{\rm IN} = 75\ \Omega$). A somewhat lower and more constant NF is expected for $Z_S = Z_{\rm IN} = 75\ \Omega$, as was verified by simulations.

[4] From simulation, a limited increase of all the NF curves is expected for frequencies approaching the -3 dB bandwidth of the amplifier. However, as the tuner resonates the capacitance at the output node, this effect is not observed during measurements.

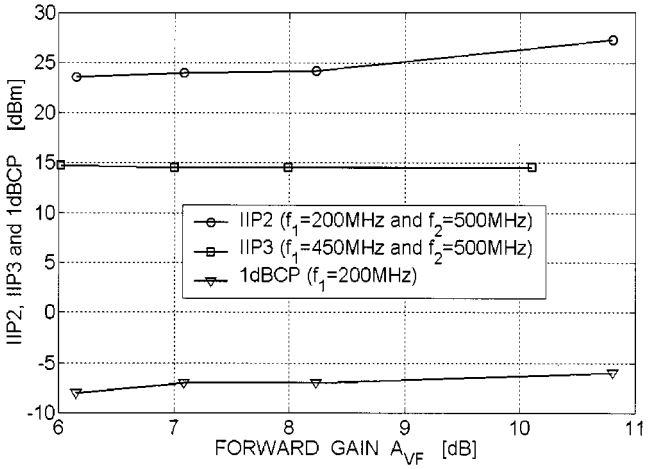

Fig. 16. IIP2, IIP3, and 1 dBCP versus A_{VF}.

TABLE III
MEASUREMENTS AT MAXIMUM GAIN.

A_{VF}	11 dB
-3dB Bandwidth	50-900 MHz
$VSWR_{IN}$	< 1.6
A_{VR}	< -30 dB
IIP2	27.4 dBm
IIP3	14.7 dBm
1dBCP	-6 dBm
NF	< 4.4 dB
Supply voltage	3.3 V
Supply current	1.5 mA
Technology	0.35 μm CMOS
Die area	0.06 mm^2

with simulations, the new wide-band LNA based on Amp1 provides a rather constant NF, which is at least 2 dB better than the (simulated) NF of the wide-band CG LNA for the same matching, power and gains.

Fig. 15 shows the input-referred second- and third-order intercept points (IIP2 and IIP3) extrapolated from measurement data at maximum gain.

In Fig. 16, IIP2, IIP3, and 1-dB compression point (1 dBCP) versus the forward gain A_{VF} are shown. IIP2 is between 23.6 and 27.4 dBm and IIP3 is between 14.5 and 14.7 dBm. The 1 dBCP is between -8 dBm and -6 dBm, which is about 20 dB smaller than the corresponding values of IIP3, while 9.6 dB is expected from simple theory [2]. These high values of IIP3 compared to the 1 dBCP suggest that some nonlinearity compensation effect occurs.

It is well known that a common-source amplifier stage with a MOS connected in diode configuration as load can have a very high IIP3 (i.e., the I–V conversion of the load is the inverse function of the input V–I conversion) but finite 1 dBCP (limited by biasing for class-A circuits). For the common-gate amplifier and Amp1, a similar behavior occurs.

The LNA drains only 1.5 mA at 3.3-V supply and the die area is 0.06 mm^2. A summary of the measurements at maximum gain is shown in Table III.

VII. CONCLUSION

A methodology generating systematically *all* two-MOS-transistor wide-band amplifiers has been presented, assuming that a MOSFET is exploited as a VCCS. The methodology renders two new circuits. Using a VCCS-based symbolic macromodel, gain and noise factors of the new amplifiers have been compared to well-known circuits. One of the new circuits (i.e., Amp1) has a relatively low noise factor, which is also gain independent. This amplifier has been used to design a 50–900 MHz variable gain wide-band LNA in a 0.35-μm CMOS technology. Measurements on the new LNA show a rather gain-independent noise figure below 5 dB. This value is at least 2 dB lower than the noise figure of the wide-band common-gate LNA for the same input matching, power consumption, and voltage gain. This demonstrates that our systematic methodology can be a viable approach to find new useful circuits.

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