Brief Papers

Intrinsic $1/f$ Device Noise Reduction and Its Effect on Phase Noise in CMOS Ring Oscillators

Sander L. J. Gierkink, Eric A. M. Klumperink, Arnoud P. van der Wel, Gian Hoogzaad, Ed (A. J. M.) van Tuijl, and Bram Nauta

***Abstract*—This paper gives experimental proof of an intriguing physical effect: periodic on–off switching of MOS transistors in a CMOS ring oscillator reduces their intrinsic $1/f$ noise and hence the oscillator's close-in phase noise. More specifically, it is shown that the $1/f^3$ phase noise is dependent on the gate-source voltage of the MOS transistors in the off state. Measurement results, corrected for waveform-dependent upconversion and effective bias, show an 8-dB-lower $1/f^3$ phase noise than expected. It will be shown that this can be attributed to the intrinsic $1/f$ noise reduction effect due to periodic on–off switching.**

I. Introduction

RING oscillators are widely applied in areas such as digital data processors and wireless communication circuits. In these applications, oscillator phase noise critically affects system performance. Recently, especially the close-in phase noise (which is largely determined by $1/f$ device noise in CMOS oscillators) has received increasing attention [1], [2].

As noise results from device physics, designers generally consider it something one cannot change (for a given transistor geometry and biasing) and has to live with. This paper demonstrates that this is not necessarily true for $1/f$ noise in MOS transistors: periodic on–off switching appears to interact with the physical noise-generating processes in an MOS transistor in such a way that its $1/f$ noise in the on-state is reduced. The amount of reduction strongly depends on the gate-source voltage in the off-state. The effect was reported in 1991 [3] but we seem to be the first to explore its implications.

In a ring oscillator, the transistors are switched by the oscillation itself. This paper shows that the $1/f^3$ phase noise of a CMOS ring oscillator benefits from this switching. However, it also appears that the effect can be counteracted by a change in upconversion and effective gate-source bias in the on-state.

The contents of this paper are as follows. In Section II, measurement results are presented of baseband MOS $1/f$ device noise under switched bias conditions. Sections III and IV discuss the ring oscillator's phase-noise measurements. After correcting the measured phase noise for 1) measured changes in upconversion and 2) changes in the effective bias of the MOS devices, the final results are shown be in good agreement with baseband $1/f$ device noise measurements.

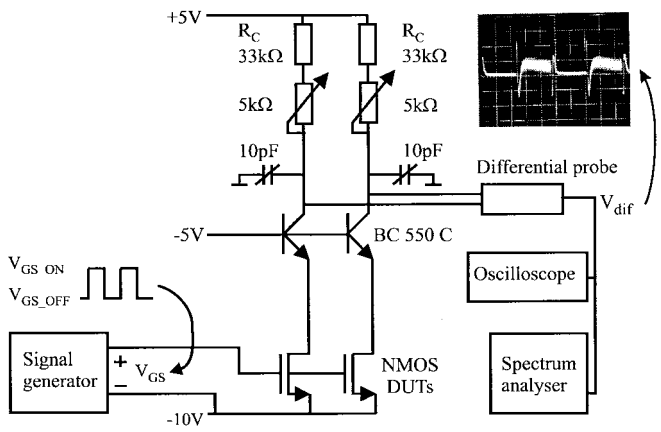

Fig. 1. Baseband $1/f$ noise measurement setup.

II. Baseband $1/f$ Device Noise Under Switched Bias Conditions

In this section, the influence of gate-source voltage switching on the baseband power spectral density of the $1/f$ noise current of an NMOS transistor is investigated. For this purpose, the experimental setup depicted in Fig. 1 is used [8], [9]. The gates of two NMOS transistors are driven by a square wave signal, which is characterized by a 50% duty cycle, a maximum voltage level $V_{\mathrm{GS\_ON}}$, and an adjustable minimum voltage level $V_{\mathrm{GS\_OFF}}$, which remains below the threshold voltage. To avoid overload of the spectrum analyzer by the large common-mode switching signal, the output noise voltage is measured using a differential probe. It was verified that the setup is such that the noise at the probe output is dominated by the drain current noise of the MOS transistors. At 50% duty cycle, the probe alternately measures MOS device noise and almost no noise (see the measured waveform in Fig. 1). The resistors and capacitors are adjustable to minimize the residual switching signal, caused by possible MOS transistor mismatch.

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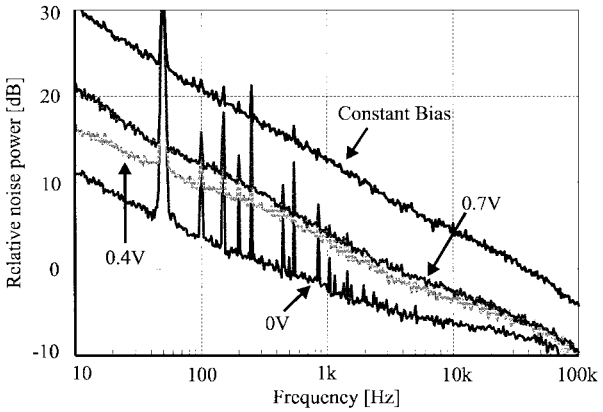

Fig. 2. Measured baseband $1/f$ noise for constant and switched bias conditions (HEF4007 NMOS, $f_{\rm switch} = 2$ MHz, 50% duty cycle, $V_{\rm GS\_ON} = 2.5$ V, $V_{\rm GS\_OFF}$ as indicated).

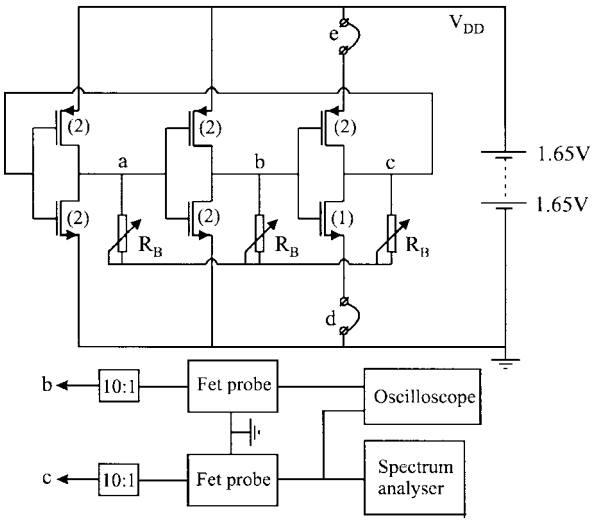

Fig. 3. Phase-noise measurement setup.

Fig. 2 shows the measured noise spectra for NMOS devices in commercially available HEF4007 MOS IC's. Bearing in mind that primarily the *changes* of the $1/f$ noise spectral density are of interest, an arbitrary reference power level was chosen in defining the vertical scale in this figure. The upper curve shows the noise spectrum measured with the MOS devices constantly biased at a gate-source voltage of 2.5 V ($V_T = 1.5$ V). The remaining curves show the noise spectrum of the devices, switched periodically between 2.5 V and $V_{\rm GS\_OFF}$ (indicated in the figure) with a 2-MHz, 50% duty cycle square wave signal. The spectral peaks are caused by 50 Hz related interference and residuals of the 2 MHz switching signal.

Modeling the 50% duty-cycle switching operation as a simple modulation action, 6 dB noise reduction is expected in the $1/f$ noise spectrum below the switching frequency. This is because the overall noise power is halved and distributed in the spectrum around dc and multiples of the switching frequency. However, the measurements show an *additional anomalous* reduction in the $1/f$ noise spectrum. The amount of noise reduction is dependent on the gate-source voltage in the off-state: the maximum additional reduction appears at minimum $V_{\rm GS\_OFF}$ and is about 8 dB at 1 kHz.

Fig. 2 leads to the remarkable conclusion that the gate-source voltage supplied to an MOS device in the off-state affects its $1/f$ noise in the on-state. This effect was reported first in 1991 by the physicists Bloom and Nemirovsky [3], who observed it in a weaker form, at a much lower switching frequency of 600 Hz. They showed that the noise reduction is maximized if the MOS transistor is cycled from strong inversion via weak inversion to accumulation. Our observations are in accordance with their conclusion. Shortly after, their results were reconfirmed [4] and related to random telegraph signals).

The explanation for the anomalous $1/f$ noise reduction has to be sought in the physics behind $1/f$ noise generation in MOSFET's. The $1/f$ noise is known for its long correlation time [5]. The physical process that is responsible for it has a "long-term memory" [5]. A process that likely plays a role in the generation of $1/f$ noise in MOSFET's is carrier (de)trapping in localized oxide states. In the literature [6], [7], several models of $1/f$ noise have appeared that relate $1/f$ noise in MOSFET's to a superposition of (random telegraph) signals, produced by many traps with different trapping times (or time constants). The memory involved with $1/f$ noise is associated with the long occupation time constants of the traps. The switching can be thought of as a means to reduce the correlation by interfering with the (de)trapping process, e.g., by forcing a trap to release its captured electron.

To allow for experimental freedom in both our baseband and phase-noise experiments, we use HEF4007 MOS transistors that are produced in rather old CMOS processes. However, the results presented in [4] show that the $1/f$ noise reduction effect appears also in submicrometer MOS transistors. Using HEF4007 IC's allowed us to perform measurements on MOSFET's from five different manufacturers. In all cases, a significant anomalous noise reduction was found, ranging from 6 to 8 dB (four to eight times less noise power).

III. Phase-Noise Measurements

Fig. 3 shows the experimental setup for the phase-noise measurements on a three-stage ring oscillator, built with HEF4007 IC's. To be able to adjust the off-voltage of the transistors during normal operation of the oscillator, the resistors R_B have been added. By lowering the resistor value, the gain of an inverter is decreased, resulting in a smaller oscillation amplitude and thus larger $V_{\rm GS\_OFF}$ values of the transistors.

To allow for easy comparison of the phase-noise measurements with the baseband noise measurements of the previous section, the channel width of the NMOS transistor in the third inverter (connected to node c in Fig. 3) is taken to be half that of the other NMOS transistors. In this way, the oscillation waveform exhibits maximum asymmetry at node c as compared to the other nodes, leaving the third inverter the dominant contributor to upconversion of $1/f$ noise [1], irrespective of the oscillation amplitude. This was verified by measurement by successively injecting a 1-μA, 10-kHz sinusoidal current into nodes a, b, and c and measuring the strength by which it reappeared in the sideband of the oscillator at 10-kHz distance from the carrier. When injected from

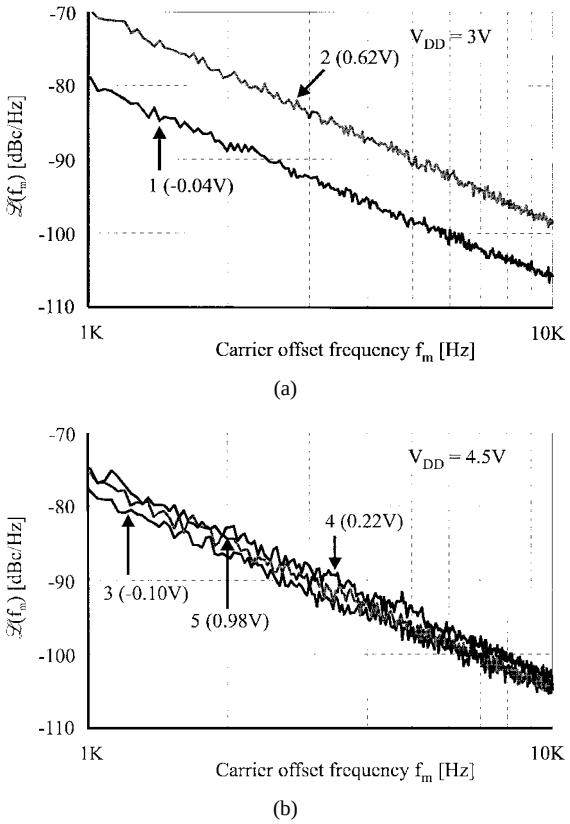

Fig. 4. Measured phase noise at different $V_{\mathrm{MIN},b}$: (a) $V_{\mathrm{DD}} = 3$ V and (b) $V_{\mathrm{DD}} = 4.5$ V.

node c, the sideband component appeared with roughly 10 dB more power (relative to the carrier) than when injected from the other nodes. Although upconversion efficiency has been increased deliberately in this experiment, in practice the unavoidable mismatch between the NMOS and PMOS transistor in each inverter will cause significant upconversion even in a well-designed oscillator.

To separate the contribution of the N- and PMOS transistor in the third inverter, a comparison of their upconversion was made at different amplitude settings. This was done by successively inserting a 0.3-mV, 10-kHz sinusoidal voltage at the source terminal of the N- and PMOS transistor (positions "d" and "e" in Fig. 3). The upconversion by the NMOS transistor exceeded that of the PMOS transistor by 10 dB or more.

As a result of the upconversion comparisons and the fact that the 4007-NMOS devices exhibit stronger $1/f$ noise than the PMOS devices, it can be concluded that the NMOS transistor in the third inverter is the dominant source of $1/f^3$ phase noise of the ring oscillator. According to Section II, the minimum value of the signal voltage at node b (which is equivalent to the $V_{\mathrm{GS\_OFF}}$ value of the NMOS transistor in the third inverter) is thus expected to be important for $1/f$ device noise reduction.

Fig. 4(a) shows the phase-noise spectra for different values of $V_{\mathrm{MIN},b}$ measured at $V_{\mathrm{DD}} = 3$ V. Table I lists the corresponding values of R_B, the oscillation frequency, and the maximum and minimum voltage of the waveform at node b (curve numbers 1 and 2). As a smaller $V_{\mathrm{MIN},b}$ is accompanied by a decrease in $1/f^3$ phase noise, this trend is apparently consistent with the $1/f$ noise reduction measured in baseband.

TABLE I
PARAMETERS FOR $V_{\mathrm{DD}} = 3$ V (CURVES 1 AND 2) AND $V_{\mathrm{DD}} = 4.5$ V (CURVES 3–5). THE CURVE NUMBERS CORRESPOND WITH THOSE IN FIGS. 4 AND 5

Curve nr.	R_B [kΩ]	f_{OSC} [MHz]	$V_{MAX,b}$ [V]	$V_{MIN,b}$ [V]
1	15	3.02	3.1	-0.04
2	2.5	3.27	2.8	0.62
3	15	6.17	4.5	-0.10
4	1.5	7.03	4.2	0.22
5	0.8	7.94	3.9	0.98

TABLE II
CORRECTION FIGURES DERIVED FROM MEASURED UPCONVERSION AND EFFECTIVE V_{GT} ($V_{\mathrm{GT,REF}} = 1$ V). THE CURVE NUMBERS CORRESPOND WITH THOSE IN FIGS. 4 AND 5

Curve nr.	Upconversion [dB]	$10\log\left(\frac{V_{GT\,EFF}^2}{V_{GT\,REF}^2}\right)$ [dB]	Correction [dB]
1	-33.5	1.5	33.5 - 1.5 = 32.0
2	-28.0	-0.6	28.0 + 0.6 = 28.6
3	-39.4	8.4	39.4 - 8.4 = 31.0
4	-39.7	7.3	39.7 - 7.3 = 32.4
5	-43.9	6.0	43.9 - 6.0 = 37.9

Fig. 4(b) shows the measured phase noise for biasing at $V_{\mathrm{DD}} = 4.5$ V, while Table I lists the corresponding relevant information (curves 3– 5). Here, at first sight, the trend does not seem to be consistent with the $1/f$ noise reduction found in baseband: curve 5 with the highest $V_{\mathrm{MIN},b}$ (0.98 V) lies in between curves 3 ($V_{\mathrm{MIN},b} = -0.10$ V) and 4 ($V_{\mathrm{MIN},b} = 0.22$ V). However, in the next section, it will be shown that after correction for upconversion and effective bias, the results agree well with the $1/f$ noise reduction measured in baseband.

IV. CORRECTION FOR UPCONVERSION EFFICIENCY AND EFFECTIVE BIAS LEVEL

Recently, it has been shown that changes in the waveform asymmetry affect the amount of low-frequency noise that is upconverted [1]. Also, changes in the effective levels of the gate-source bias voltage directly affect the $1/f$ noise of a MOS transistor. In this section, the influence of these effects will be examined quantitatively. By correcting the measured phase-noise spectra for these influences, an attempt is made to isolate the effect of the $1/f$ noise reduction, caused by periodic on–off switching.

The measurement of the amount of upconversion is carried out by injecting a 10-kHz sinusoidal current with fixed amplitude at node c in the running oscillator and measuring the relative strength of the resulting sideband component at 10-kHz offset from the carrier. The results obtained are listed in the second column of Table II.

The corrections on the phase-noise measurements that are required because of changes in the effective gate-source voltage bias are established as follows. As argued before, it is allowed to focus on the dominant noise contributor: the NMOS transistor in the third inverter. This transistor produces its maximum noise current during the time interval in which

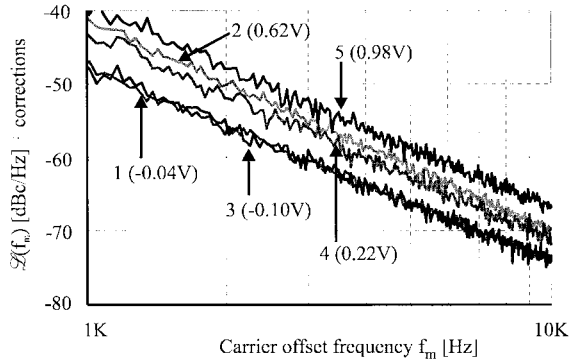

Fig. 5. Phase-noise measurement results plus corrections for changes in upconversion and effective bias level.

it discharges node c. As the discharging process determines oscillator timing, the noise current of the NMOS device in the third inverter is translated into timing jitter (phase noise) just when it is maximal. In the calculation of the device noise, it is therefore reasonable to assume an effective steady-state bias voltage at node b, which is equal to the flat maximum $V_{\mathrm{MAX},b}$ (see Table I) of the actual oscillation waveform at node b. Since the power spectral density of the $1/f$ noise current in steady-state MOS transistors is roughly proportional to V_{GT}^2 $(V_{\mathrm{GT}} = V_{\mathrm{GS}} - V_T)$, the ratio of the effective bias $V_{\mathrm{GT,EFF}}$ $(=V_{\mathrm{MAX},b} - V_T)$ to an arbitrarily chosen reference value $V_{\mathrm{GT,REF}} = 1.0$ V has been used to correct for amplitude-dependent biasing. Correction figures in decibels are listed in the third column of Table II.

The resulting total correction in decibels is shown in the fourth column of Table II. Fig. 5 shows the curves of Fig. 4 after correction. Remarkably, now a $V_{\mathrm{GS\_OFF}}$ decrease corresponds to a decrease in $1/f^3$ phase noise; a similar relation was found in Section II between $V_{\mathrm{GS\_OFF}}$ and the baseband $1/f$ noise. The decrease in $1/f^3$ phase noise is maximally about 8 dB at a carrier offset of 1 kHz and corresponds well with the baseband measurements. It is concluded that a strong agreement has been shown between $1/f$ device noise as obtained by 1) baseband measurements of switched devices and 2) inference from oscillator phase-noise measurements. The remaining differences could be caused by the assumptions about the effective bias level and the use of a first-order $1/f$ noise model.

V. Conclusion

The physical effect of intrinsic $1/f$ device noise reduction [3], [4] in periodically switched MOS transistors has been shown to occur also at high switching frequencies (>1 MHz). It is shown that this effect results in an 8-dB reduction of $1/f^3$ phase noise in a CMOS ring oscillator.

The reduction of intrinsic $1/f$ noise by periodically switching MOS transistors is expected to be useful for applications other than oscillators, as it attacks $1/f$ noise at its physical roots and can result in a reduction of power consumption as well.

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