A CMOS "Soft-Switched" Transconductor and Its Application in Gain Control and Filters

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Abstract— This paper presents a transconductor suitable for implementation in submicron CMOS technology. The transconductor is nearly insensitive for the second-order effects of the MOS transistors, which become more and more prevalent in today's submicron processes. The transconductor relies on a differential pair with variable degeneration resistance, while the degeneration resistors are "soft-switched" by means of MOS transistors. The transconductance is continuously tunable. A transconductor, using a device in which the degeneration resistors and "soft switches" are merged, is optimized for a maximum tuning range and can be used in variable gain stages like in an automatic gain control (AGC) circuit. Besides, a third-order 5.5 MHz low-pass filter has been realized in a 0.5-μm CMOS process using the "soft-switched" transconductor. At a 3.3 V supply voltage the filter dissipates 12 mW and the dynamic range equals 62 dB where the total harmonic distortion (THD) is -48 dB for an input voltage of 1 V_{pp}.

Index Terms— Amplifiers, circuit theory and design, CMOS devices, CMOS integrated circuits, continuous-time filters, integrators, transconductors, tuning.

I. INTRODUCTION

OVER the last three decades the integration of electronic circuits on a silicon substrate has made an enormous step forward, and nowadays the miniaturization has still not reached its end. High component density, particularly for digital CMOS circuits, can be obtained. Therefore, more and more signal processing functions are implemented by digital circuitry since it often requires less chip area and power compared to an analog implementation of the same function. Remaining analog functions on a mixed-signal IC realized in a submicron CMOS technology are, for example, A/D and D/A conversions, amplification, buffering, clock generation, and some filter functions.

Basic building blocks in many analog subsystems are transconductors, also called voltage to current (V-I) converters. Transconductors are well suited in variable gain stages required for automatic gain control (AGC) [1], [2], and in continuous-time filters implemented with the transconductance-C technique [3]–[6]. These kind of filters

can be used, for example, as an anti-aliasing filter before a high-speed A/D converter.

This paper presents a continuously tunable transconductor suitable for high-frequency applications. It has a very low sensitivity for the MOS transistors second-order effects, which makes it therefore suitable for realization in a submicron CMOS technology. In Section II the design considerations will be discussed. In Section III the operation principle of the "soft-switched" transconductor will be explained. The transconductor core can be implemented in a very compact way with a new device in a standard CMOS process without any extra process options. This merged device, in which the degeneration resistors and "soft switches" are combined, is shown in Section IV. The transconductor using the merged device and optimized for a maximum tuning range, which is required in an AGC circuit, is presented in Section V. Section VI deals with a third-order 5.5 MHz low-pass gm-C filter. The filter has been realized in a 0.5-μm CMOS process and can be used as an anti-aliasing filter before a high-speed A/D converter. Finally, in Section VII the conclusions are drawn.

II. DESIGN CONSIDERATIONS

Nearly every published analog tunable transconductor in CMOS technology relies on the MOS transistor characteristics and makes use of the linear [5] or square-law [7], [8] behavior between the drain current and the gate-source voltage. Unfortunately, in a submicron process with relatively low oxide thickness and high substrate dopes, the transistor's second-order effects like mobility reduction and velocity saturation become more and more prevalent. Therefore, the transistor characteristics deviate significantly from the ideal behavior. This results, especially for a square-law converter [7] and a passive triode converter [9], in relatively high distortion levels in combination with a reduced transconductance tuning range. However, the performance of an active triode converter [5] decreases mainly with respect to the linearity rather than the tuning range [10].

It is shown in [11] that mobility reduction linearizes a long tailed pair. However, it decreases the maximum transconductance. In order to maintain a certain tuning range, the long tailed pair must operate in moderate (or even weak) inversion at the lowest transconductance values. Consequently, the distortion increases for a constant input voltage amplitude.

To overcome these problems, basically three design strategies can be applied.

1) Compensation techniques can be used in order to compensate at least for the most dominant nonlinearity. Generally, compensation techniques are not robust against mismatch and usually decrease the dynamic range per unit of power. Furthermore, the cause of the most dominant nonlinearity is biasing and technology dependent. Although compensation techniques can improve the linearity [10], [12], [13], they are usually not preferable.

2) The signal voltage swing over a nonlinear device can be reduced so that a "small-signal" approach is valid. In this way, distortion is hardly generated and the effect of mismatch will be small. However, a small signal approach implies that the bias current is significantly larger than the signal current which can result in a noisy transconductor and a low dynamic range per unit of power as well. Special care has to be taken to avoid this problem [14].

3) Instead of MOSFET's, linear devices can be used such as resistors. The linearity of resistors is usually sufficient and much better than that of a MOS transistor. Besides, a resistor requires no bias current. As a disadvantage, the resistance is not electrically tunable.

A combination of the techniques mentioned under 2) and 3) is presented in [15] where a circuit containing resistors, MOSFET's, and op-amps is used. The MOSFET's only handle small signals in order to keep the distortion low. The tuning is achieved by shunting or subtracting input signals, however, this basically lowers the dynamic range for a given amount of power. In general, at high frequencies op-amps are not very useful due to their negative effect on the transconductor's phase behavior.

Considering the above-mentioned facts, a new transconductor was developed using resistors and transistors. The transistors are used in such a way that the small-signal approach is valid as much as possible resulting in a small nonlinearity contribution. The following section will describe the operation principle of the new "soft-switched" transconductor.

III. OPERATION PRINCIPLE OF THE "SOFT-SWITCHED" TRANSCONDUCTOR

The schematic diagram illustrating the transconductor principle is depicted in Fig. 1 and is basically a degenerated differential pair. The tuning of the circuit is realized via the voltage V_{GB}. The degeneration resistance can be gradually varied by means of "soft-switched" transistors M2 and M3, in this way a continuously tunable transconductance is obtained [16]–[18].

The gates of the "soft switches" (M2 and M3) are connected to the same node. Because of the dc-voltage drop over the resistors R3a,b, which is equal to $R3 \cdot I_o$, the effective gate source voltages of M2 and M3 differ in such a way that

$$|V_{GS_{eff2}}| > |V_{GS_{eff3}}|. \qquad (1)$$

This condition is always valid thanks to the topology of the circuit. Therefore, M2 conducts before M3 for increasing values of V_{GB}. Since the source and drain of the transistors M2 and M3 are symmetrically used, they are interchangeable.
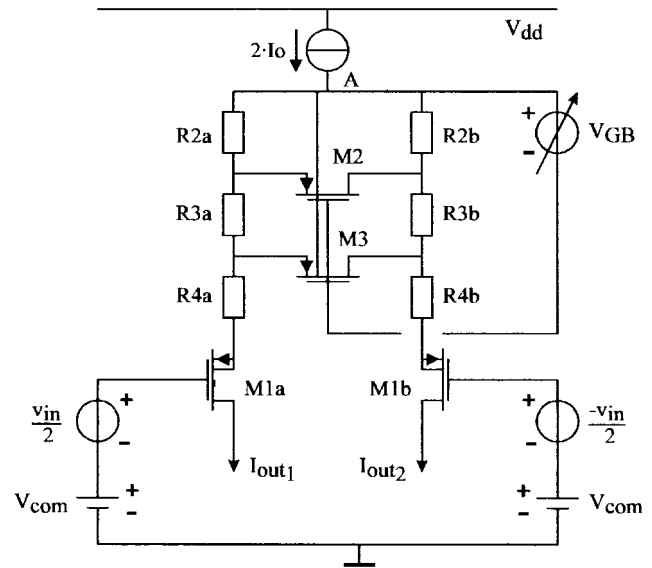

Fig. 1.   Schematic diagram of the "soft-switched" transconductor principle.

The back gates of these transistors are connected to node A. Due to the body-effect, the threshold voltage of M3 (V_{T3}) is larger than the threshold voltage of M2 (V_{T2}) since V_T is equal to

$$V_T = V_{T0} + \delta \cdot V_{SB} \qquad (2)$$

where V_{T0} is the threshold voltage at $V_{SB} = 0$ V and δ is the linearized body-effect parameter [19]. So, the body-effect of the "soft switches" further increases the differences of the effective gate source voltages but is *not* essential for a correct operation of the circuit.

For low values of V_{GB} where M2 and M3 do not conduct, the input transistors are maximally degenerated by $R2, R3$, and $R4$. For increasing values of V_{GB} when M2 starts to conduct, the resistors $R2a$ and $R2b$ are more or less shunted by M2. Therefore, the effective degeneration resistance decreases, resulting in a higher transconductance value. By further increasing $V_{GB}, R3a$, and $R3b$ are shunted by M3. The minimum degeneration resistance is determined by $R4$ and the lowest value of r_{ds3}. Only two "soft switches" are drawn in Fig. 1, but the number can be increased.

Now, the distortion behavior of the transconductor is discussed. For a V_{GS2} value close to V_{T2}, M2 turns on and is in nonsaturation for $v_{in} = 0$ V. A nonzero input signal will enforce v_{ds2} unequal to zero and brings transistor M2 into saturation, which causes a slightly too large signal output current compared to a perfectly linear device. The nonlinear current though M2 depends strongly on its drain-source voltage. Fortunately, v_{ds2} is only a fraction of v_{in} due to the resistive divider $R2/(R2 + R3 + R4 + 1/g_{m\_M1})$ keeping the distortion relatively low. However, for a very low value of $R2$ compared to the total degeneration resistance, the transconductance tuning due to M2 will also be small. For higher values of V_{GB}, M2 will stay in nonsaturation and is basically a linear device by itself.

A further increase of V_{GB} will turn on M3. Due to the drain-source resistance of M2, the voltage swing over the
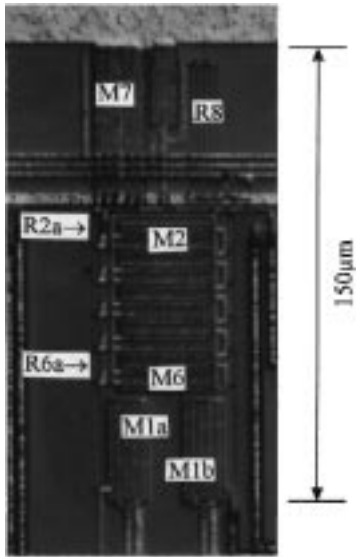
Fig. 2. Transconductor, realized with five "soft switches."

drain-source of M3 is lower than expected from the resistive divider $(R2 + R3)/(R2 + R3 + R4)$. The actual resistive division is nearly equal to $R3/(R3+R4)$, resulting in a fairly low overall distortion contribution of M3.

If all the "soft switches" are turned on, the effective degeneration resistance is lowered, resulting in a smaller input window of the converter. Consequently, for a constant input voltage amplitude, the distortion of the converter increases. This implies that tradeoff must be made between the maximum input voltage swing that can be handled and the tuning range. In an AGC this tradeoff is of minor interest since the input voltage swing decreases for increasing values of the transconductance.

Since the transistors are more or less used as switches, only the *first*-order characteristics of the transistors affect the *second*-order effects of the transconductor, whereas the *second*-order effects of the transistor are hardly of interest. This makes the transconductor suitable for implementation in a modern submicron CMOS process.

Realization

The transconductor has been realized in a 0.5-μm standard CMOS process. Five "soft switches" are used instead of two. It appeared from the simulation results that for the applied voltages, five "soft switches" were sufficient for a smooth transconductance tuning range. The schematic diagram of the realized circuit is shown in Fig. 2.

The circuit has been implemented with PMOS transistors. In an N-well CMOS process the back gate (N-well) of the PMOS transistors can be freely used, in contrast to NMOS transistors where the back gate is by definition equal to the substrate. The N-well can be connected to a dc and low impedance node, for example, the supply voltage V_{dd}. In that case, N-well shields the transconductor more or less from digital substrate noise.

The voltage source V_{GB} has been implemented by drawing a current through a resistor connected between node A and the gates of the "soft switches." A copy of the tune current I_{tune} flows through $R8$ to establish the tuning. The tune voltage V_{GB} of the "soft switches" is proportional to I_{tune}. The transistors M9, M11, and M12 are applied to compensate for the tune current through $R8$. In this way, the current through the degeneration resistors is not affected. The resistors $R2$ through $R6$ have the same value, and all the "soft switches" are equal. This way of dimensioning is just straightforward and easy to design. The circuit was dimensioned for a tuning range of a factor two, needed to overcome absolute process and temperature variations. The total maximal degeneration resistance is equal to 2×10 kΩ and can be tuned to an effective degeneration resistance of 2×5 kΩ. All resistors have been implemented using poly-silicon. The transconductance of M1 is about 1 mA/V. Although the circuit of Fig. 2 does not suggest to be a low voltage solution, it requires no more supply voltage compared to a nondegenerated MOS differential pair. In the latter case, the gate-source voltage needs to be significantly

Fig. 3.   Chip photograph of the converter given in Fig. 2.

Fig. 4.   (a) Measured transconductance versus input voltage for various tune currents. (b) Measured transconductance versus the tune current.

larger in order to keep the distortion low. The dc voltage drop over the resistors is only 0.7 V.

Fig. 3 shows the chip photograph of the circuit given in Fig. 2. The area of the "soft switches" and degeneration resistors is 2500 μm^2. The chip area of the complete converter core equals 6000 μm^2.

The transconductance (dI_{out}/dV_{in}) was measured versus V_{in} and versus I_{tune}; the results are shown in Fig. 4(a) and (b), respectively. Fig. 4(a) shows that for low and high transconductance values the curves are convex. In these situations the distortion of the circuit is mainly caused by the input transistors M1. For intermediate transconductance values, the shape of the curves is concave. The "soft switches" are forced into saturation by the input signal, resulting in a slightly too large output current and an increase of the transconductance versus V_{in}.

The total harmonic distortion (THD) figures are measured at 1 kHz for an input voltage of 1 $V_{pp\,diff}$, the results are given in Fig. 5 by the solid line. The maximum THD is −48 dB. The simulation results are also given in Fig. 5. The simulated and measured curves are somewhat shifted. This is mainly a result of the absolute resistance variation during processing. For a higher value of $R8$ the THD curve shifts to a lower tune current.

IV. THE TRANSCONDUCTOR IMPLEMENTED WITH A MERGED DEVICE

Taking a closer look at the CMOS process, it appears that both a diffusion resistor and the source and drain of a transistor are made of diffusion areas. This gives the opportunity to combine the degeneration resistors and the "soft switches" in a so-called "merged device" [16], [18]. The *total* degeneration resistance determines the minimum transconductance. However, it is less obvious how many discrete "soft switches" are needed for a smoothly varying transconductance. In fact, an infinite number of "soft switches" could be taken. It appears that the degeneration resistors and "soft switches" can be elegantly combined.
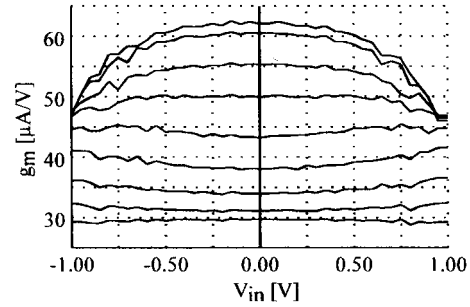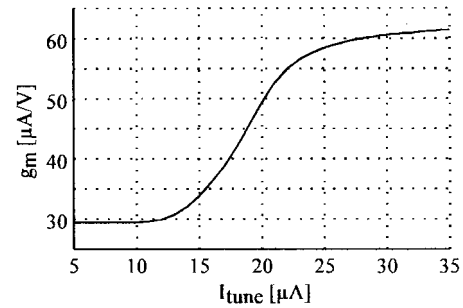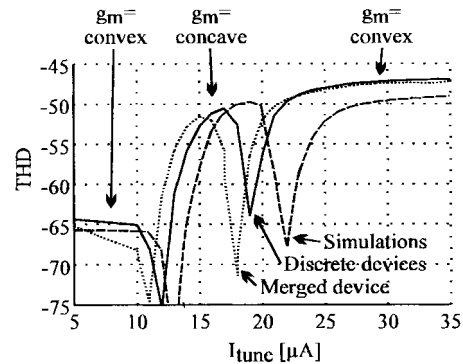

Fig. 5.   Measured and simulated THD of the transconductor implemented with discrete "soft switches" (Fig. 2) and implemented with a merged device (Fig. 6) versus the tune current, $f_0 = 1$ kHz.

The source and drain of a MOS transistor consists of highly doped diffusion areas. These diffusion areas are of N-type for NMOS transistors and P-type for PMOS transistors. Normally the diffusion areas are contacted over the entire area by a low ohmic layer, e.g., metal, in order to get a homogeneous current distribution along the width of the transistor. A diffusion resistor consists of the same N- or P-type diffusion areas as the source and drain of a transistor. However, a resistor is only contacted at the very ends of the structure. Without extra process options, it is possible *not* to cover the source and drain areas of the transistor with a low ohmic layer. Consequently, the source and drain can also simultaneously be used as resistors. This gives the opportunity to combine the degeneration resistor and the "soft switches."

Fig. 6 shows the transconductor with the merged tuning device. The merged device is drawn correspondingly to the top view of the chip layout. The source and drain at the left and

right side of the gate are used as degeneration resistors as well. These resistors $(R9)$ are only contacted at the top and bottom. The position of the gate contact is of less importance since no dc current flows through the gate. A construction with current flowing along the gate, and thus causing a voltage gradient, is imaginable but appears to be impractical and decreases the power efficiency.

Due to the current I_o, there is a voltage drop over the resistors $R9$, therefore, the absolute value of the effective gate-source voltage going from top to bottom decreases gradually. Besides, due to the body effect, the threshold voltage of the merged device increases along the resistors $R9$ from top to bottom. The N-well is connected to node A. For an increasing tune current, the potential of the gate decreases and an inversion layer underneath the gate occurs at the top first and "grows" to the bottom. The signal current flows vertically through the resistors $R9$ and horizontally through the inversion layer. Due to the small width of the merged device (which is conventionally the length of the transistor) compared to the length of the merged device (which is conventionally the width of the transistor), the vertical or diagonal currents through the inversion layer are negligible. Using the merged device, the transconductor has actually been realized with an *infinite* number of "soft switches." Similar structures of a gradually varying degeneration resistance are also known in bipolar technology [20], [21]. In these structures a control current flows through a resistive base or emitter of a bipolar transistor, resulting in a infinite number of "diodes" that continuously tap along the degeneration resistor.

In the previously described discrete version and the version using the merged device, both are dimensioned to have equal performances. Indeed, it appeared that the measured transconductance and tuning range are similar compared to the results of the converter with five discrete "soft switches" given in Fig. 4(a) and (b). The THD figures are given in Fig. 5 by the dashed line which also indicates the nearly equal performances of both transconductors at low frequencies.

The circuit cannot easily be simulated with a circuit simulator since normally no implicit model for the merged device is available. For a relatively small tuning range of a factor two, the approximation of the merged device with five "soft switches" appears to be sufficient. However, for a larger tuning range, the number of discrete "soft switches" must be increased. This implies that the merged device is well suited if a large tuning is needed, for example in an AGC.

V. A TRANSCONDUCTOR SUITABLE FOR GAIN CONTROL APPLICATIONS

The previous converters had a tuning range of a factor two in order to overcome temperature and process variations. In some applications the converter needs to have a larger tuning range, for example in a continuously tunable gain control. A transconductor with a merged tuning device appears to be a good candidate for these applications.

The circuit of Fig. 6 without the resistors $R7$ has been used to establish a converter with a maximized tuning range. Moreover, the back-gates of the input transistors are connected
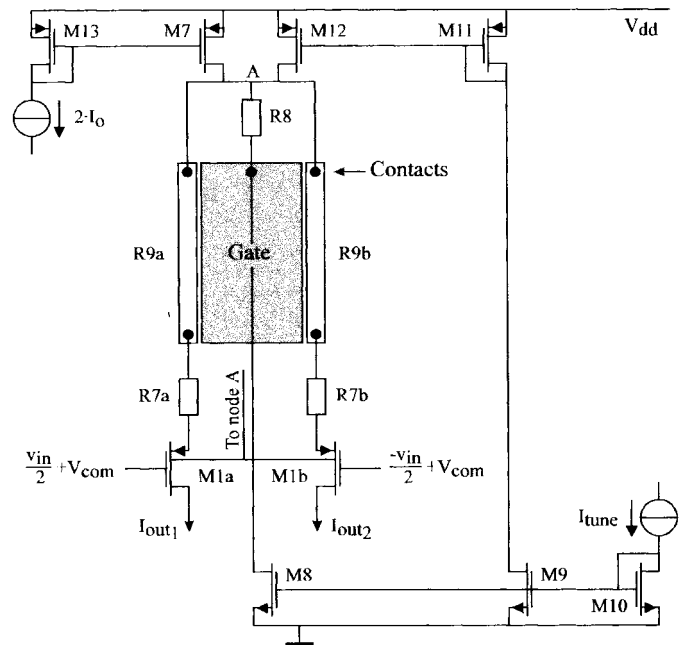

Fig. 6. Schematic diagram of the transconductor using a merged device; $R9a$ and $R9b$ are also the source and drain diffusions of the "soft switches."

Fig. 7. A transconductor using a merged device with maximized tune range, suitable for AGC applications.

to their own sources so that the body-effect of the input transistors does not lower the maximum transconductance value. Besides the merged device and $R7$, the dimensioning of the circuit is equal to that of the previously described transconductors. If there is no input signal, the voltage drop over the degeneration resistors is 0.9 V.

Fig. 7 shows the chip photograph of the converter. Two merged devices are connected in anti-parallel in order to compensate for mismatch due to asymmetry during processing. The transistor gate has a length of 0.5 μm. The total area of the converter core is 7000 μm^2.
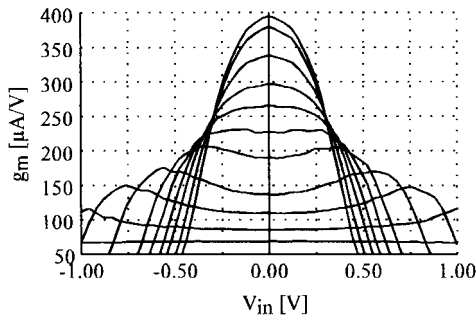
Fig. 8.　Measured transconductance versus the input voltage of the circuit of Fig. 7.

Fig. 9.　The THD and input voltage versus tune current at constant output signal, $f_0 = 1$ kHz.

The transconductance was measured versus V_{in}, and the results are given in Fig. 8. The transconductance can be tuned from 70 μA/V to 390 μA/V which is a variation of more than a factor five. The input window of the converter is large for a low transconductance value since the input transistors are strongly degenerated. For a high value of the transconductance, where the degeneration is minimal, the input window is small. In a gain control application, the amplification must be small for large input voltages and high for low input voltages. Therefore, the input window of the circuit must be large for large input voltages and might be smaller for small input voltages. Fortunately, the converter described here follows the requirements, in contrast to a long tailed pair where the input window decreases at low gain [2]. Besides, the input referred noise voltage is proportional to $1/\sqrt{g_m}$ which implies that it is low for a large transconductance value. So the input referred noise voltage is low at small input signals. These combinations result in a large signal-to-noise ratio over the entire tuning range which makes the transconductor applicable for this purpose.

For the THD measurements, the circuit is terminated with a differential resistance of 2 kΩ. The input amplitude is chosen in such a way that the output voltage has a constant amplitude for every measured point, i.e., $v_{out} = 60$ mV$_{diff\,RMS}$. Fig. 9 shows the measured THD on the left y-axis and the rms value of the differential input voltage in the right y-axis. The worst-case THD over the entire tuning range occurs at an input voltage of 200 mV$_{diff\,RMS}$ and is just smaller than -40 dB.

VI. THE THIRD-ORDER 5.5 MHz LOW-PASS FILTER

This type of transconductor is suited for filter applications in the low megahertz range. At very high frequencies no internal nodes are allowed [6] for optimal phase behavior. The transconductor is used in a 5.5-MHz low-pass filter. The filter can be used as an anti-aliasing filter for a video A/D converter [4]. Since the cutoff frequency is constant, the tuning-range of the filter must be sufficient to overcome absolute process and temperature variations. Taking the spread of transistors, resistors, and capacitors into account, the tuning range must be plus and minus 50%.

The transconductor schematic used in the filter is given in Fig. 10(a). The core consist of the "soft-switched" structure. A folded cascode and a common-mode control circuit are added. The transistors M9 and M10 operate in the nonsaturation
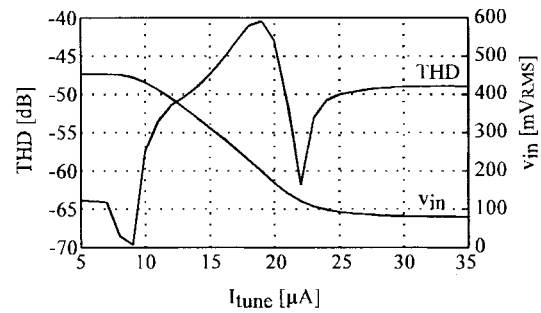
region. The bias voltages V_{B1} and V_{B2} are properly applied by means of a bias circuit.

The implementation of the voltage source V_{tune} is given in Fig. 10(b). The tuning is realized via I_{tune}. The tail current I_o is compensated for I_{tune} so that the biasing of the circuit does not change. For increasing transconductance values, the current modulation of the input transistors M1a,b increases. Without extra measures these transistors would dominate the overall distortion figures. Therefore, extra dc currents, proportional to the tune current, are injected in the sources of the input transistors. The four extra current sources [dashed lines in Fig. 10(a)] are copies of I_{tune} and have a maximum value of 50 μA.

In this design, the noise of the transconductor is mainly determined by the current sources of the folded cascodes and the common-mode circuit. The noise current of the core of the transconductor is relatively low. The "soft switches" produce only thermal noise and no $1/f$ noise since the dc current is zero. If $v_{in} \neq 0$, the voltage noise at the gates of the "soft switches" introduces some current noise in the signal path.

The transconductance was measured versus V_{in}, the measurement results are given in Fig. 11. The transconductance is tunable over a factor three, which is equal to plus and minus 50%. Thanks to the extra bias currents at relatively high transconductance values, the transconductance rolloff is somewhat reduced. The worst case THD of the transconductor for an input voltage of 1 V$_{pp\,diff}$ and a frequency of 1 kHz is -48 dB.

The third-order 5.5-MHz low-pass Bessel filter has been realized in a 0.5-μm double-poly N-well CMOS process. A passive prototype circuit is given in Fig. 12. The filter has an extra notch for improved stop-band damping, the notch is implemented with $C3$. Furthermore, the group delay variation is small which is required for the application. Fig. 13 shows a balanced active implementation using the "soft-switched" transconductors.

A chip photograph of the filter implementation is given in Fig. 14, the filter area is 0.15 mm^2. The capacitors were made with double poly.

The gain of the filter was measured versus frequency for different values of I_{tune}, the results are shown in Fig. 15. The -3 dB cutoff frequency was tuned manually from 2.2 to 6.7 MHz by means of the tune current. The depth of the notch depends on the tuning due to the varying phase-shift of the transconductor, which is less than $0.4°$ at 5.5 MHz
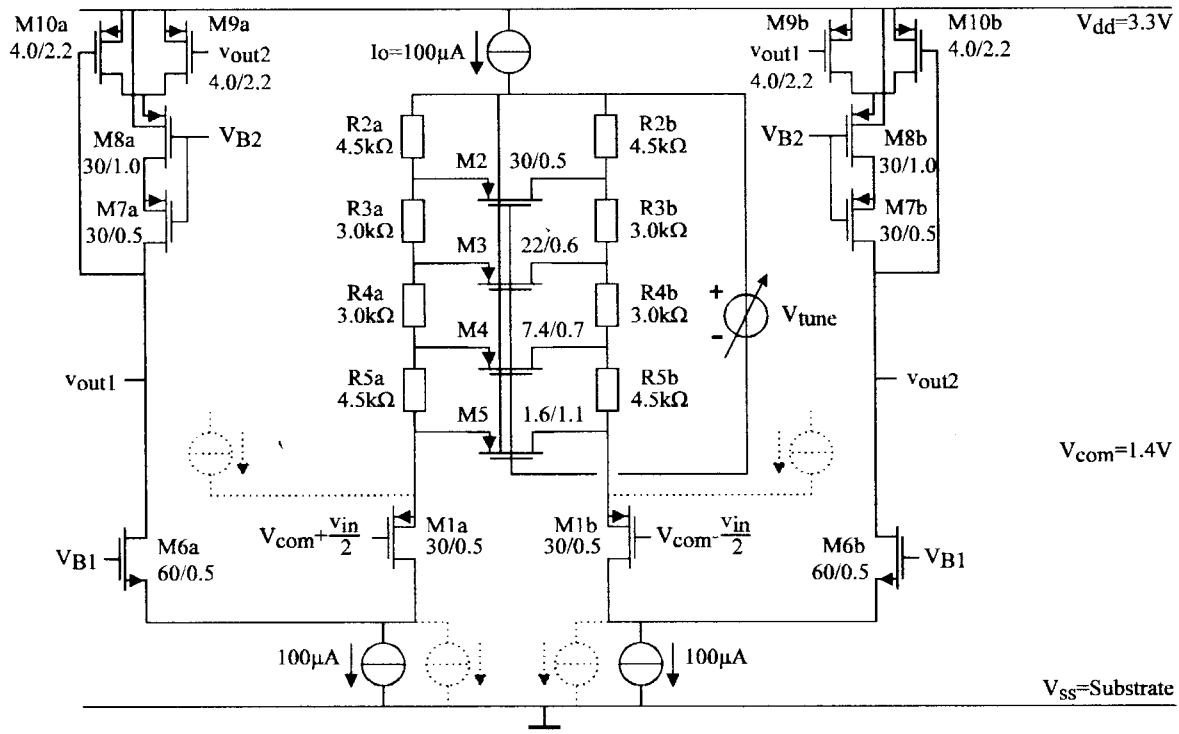
(a)

(b)

Fig. 10. (a) The schematic diagram of the transconductor used in the 5.5-MHz low-pass filter. (b) The implementation of the tune voltage source: V_{tune}.
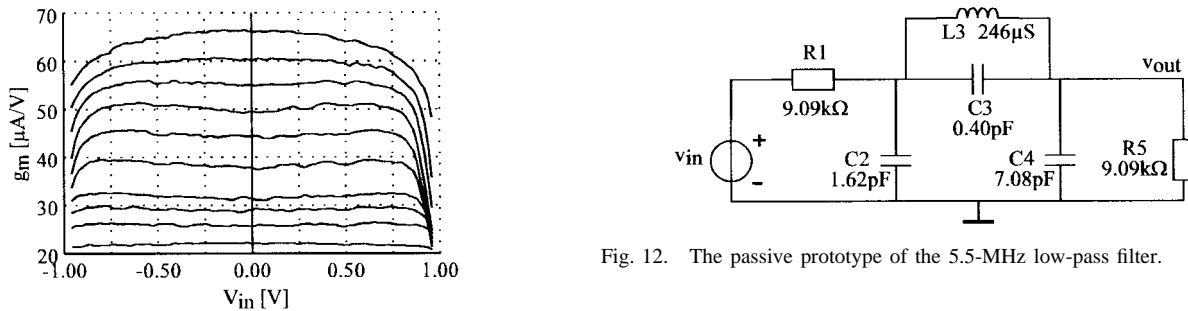

Fig. 11. The transconductance versus input voltage for various tune currents of the transconductor shown in Fig. 10(a).

Fig. 12. The passive prototype of the 5.5-MHz low-pass filter.

for the nominal transconductance value. The filter gain rolls off somewhat smoothly at the cutoff frequency. Thanks to the smooth frequency response, the group delay variation remains small. The gain rolloff in the pass-band will be corrected in the digital domain after the A/D converter.

The measured nominal gain of the circuit given in Fig. 13 is given in Fig. 16(a). The gain simulated with the ideal filter of Fig. 12 has been normalized to 0 dB and is also given in Fig. 16(a). These two lines match closely. Due to a finite quality factor and noise of the transconductor, the notch depth

is finite, where in simulations using the ideal filter the notch depth is infinite. The stop-band damping equals −32 dB.

The measured and simulated phase and group delay of the nominal transfer are given in Fig. 16(b), the simulation results are obtained with the ideal filter (Fig. 12). The measurement results are in good agreement with the simulation results obtained with the ideal filter. The maximum group delay variation in the pass-band is 13 ns.

Intermodulation measurements have been carried out in order to measure the distortion of the filter. Since the third-order intermodulation products manifest in a small frequency band around the fundamentals, the filter characteristic hardly effects the distortion measurement, in contrast to THD mea-
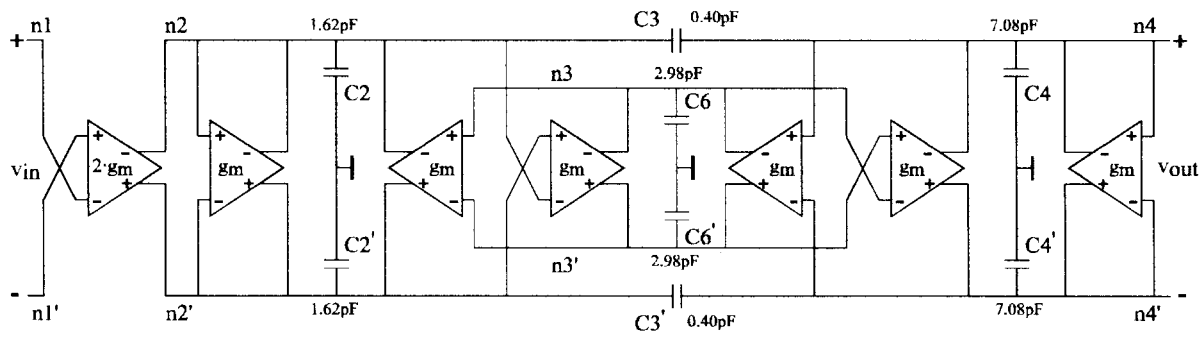
Fig. 13.   The balanced active gm-C implementation of the filter.
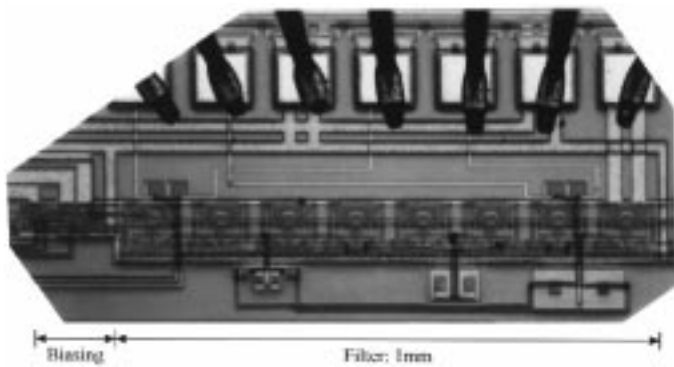

Fig. 14.   Chip photograph of the filter implemented with the "soft-switched" transconductor.
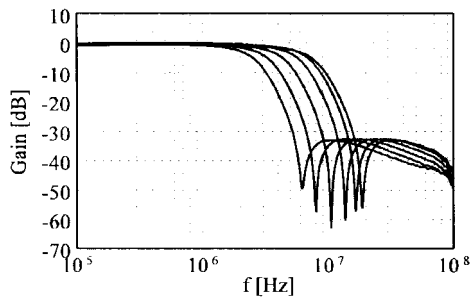

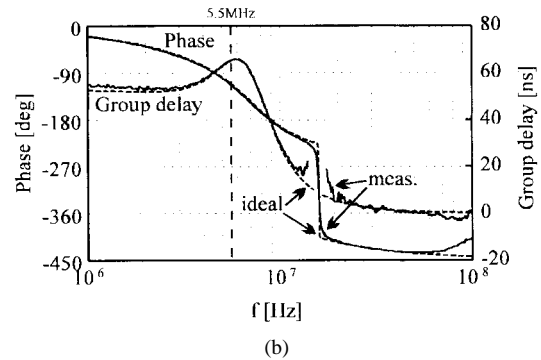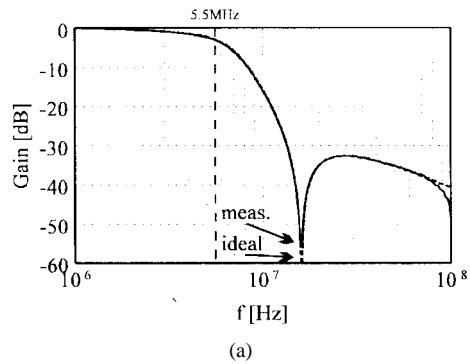Fig. 15.   The measured filter gain versus frequency for various tune currents.

Fig. 16.   (a) The measured nominal gain and simulated normalized gain of the ideal filter versus frequency. (b) The nominal phase and group delay versus frequency, measured and simulated with the ideal filter.
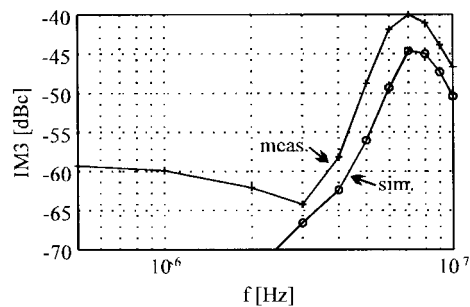

Fig. 17.   Intermodulation distortion versus frequency, measured and simulated at the nominal transfer. $v_{\mathrm{in}} = 1\ \mathrm{V_{pp\ diff}}$.

surements. Fig. 17 shows measured and simulated IM3 results obtained with the circuit of Fig. 13 for the nominal transfer. At low frequencies, mutual distortion cancellation of the transconductors occurs. In simulations, these cancellations are perfect, therefore the simulated IM3 for low frequencies is zero. In measurements, some distortion at low frequencies remains due to mismatch. For frequencies close to the cutoff frequency of the filter, the IM3 increases due to two facts. First, at these frequencies the capacitive currents are no longer negligible, resulting in a phase-shift between the internal filter nodes. Therefore the mutual distortion cancellation of the transconductors does not occur at these frequencies since the currents are out of phase. Second, the voltage amplitudes at some internal nodes increase about 6 dB close the cutoff frequency. This means that close to the cutoff frequency some transconductors have an input signal twice as large as the input signal at lower frequencies.

The output noise voltage of the filter has been measured. The noise voltage over a frequency range of 1 kHz to 5.5 MHz equals 268 $\mu\mathrm{V_{RMS}}$ which is slightly higher than simulated, i.e., 190 $\mu\mathrm{V}$. It appeared that due to absolute processing spread the

TABLE I
FILTER CHARACTERISTICS

Parameter	Value
f_{-3dB} nominal	5.5 MHz
Stop-band rejection	–32 dB
f_{-3dB} tuning range	2.2–6.7 MHz
Output noise, 0–5.5 MHz (nominal)	268 μV_{RMS}
THD (In pass-band, $v_{in\,max} = 1V_{pp\,diff}$)	–48 dB
IM3 (In pass-band $v_{in\,max} = 1V_{pp\,diff}$)	–45 dB
Dyn. Range ($v_{in\,max} = 1V_{pp\,diff}$)	62 dB
CMRR, $v_{in} = 0V$	–50 dB
Group delay variation	13 ns
Power dissipation (Vdd=3.3 V)	12 mW
Chip area, (0.5-μm CMOS, double poly)	0.15 mm^2

common-mode circuit [M7–M10, Fig. 10(a)] produces slightly more noise than in simulation.

The filter characteristics are summarized in Table I.

VII. CONCLUSION

A continuously tunable "soft-switched" resistor-based transconductor has been presented. The *second*-order effects of the transconductor are determined by the *first*-order transistor characteristics. This is owing to the fact that the V–I conversion relies basically on a resistive degenerated differential pair while the MOS transistors, used for the V to I conversion, are only used for "soft switching" the degeneration resistors. The *second*-order effects of the transistor therefore hardly affect the transconductor performance which makes the circuit also suitable for future submicron CMOS technologies.

The transconductor has also been realized using a merged device, in which the degeneration resistors and the "soft switches" are merged. The transconductor using the merged device has been optimized with respect to its tuning range. This converter is a good candidate for variable gain stages required in automatic gain control loops.

A 5.5-MHz low-pass filter using the "soft-switched" transconductor has been realized in a 0.5-μm CMOS process. The transconductor used in the filter has a tuning range of ±50% in order to compensate for temperature and process variations. The input voltage of the filter can be 1 $V_{pp\,diff}$, whereas the THD is less than −48 dB in the whole pass-band. The filter consumes 12 mW on a 3.3-V supply voltage.

REFERENCES

[1] E. A. M. Klumperink, "Cascadable CMOS current gain cell with gain insensitive phase shift," *Electron. Lett.*, vol. 29, no. 23, pp. 2027–2028, Nov. 11, 1993.

[2] C. H. J. Mensink and R. F. Wassenaar, "A programmable voltage gain-cell," *IEEE Circuits & Dev. Mag.*, vol. 10, p. 42, Mar. 1994.

[3] F. Krummenacher and N. Joehl, "A 4-MHz CMOS continuous-time filter with on-chip automatic tuning," *IEEE J. Solid-State Circuits*, vol. 23, pp. 750–758, June 1988.

[4] V. Gopinathan, Y. Tsividis, K. Tan, and R. Hester "Design considerations for high-frequency continuous time filters and implementation of an antialiasing filter for digital video," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1368–1378, Dec. 1990.

[5] J. L. Pennock, "CMOS triode transconductor for continuous-time active integrated filters," *Electron. Lett.*, vol. 21, no. 18, pp. 817–818, Aug. 29, 1985.

[6] B. Nauta, "A CMOS transconductance-*C* filter technique for very high frequencies," *IEEE J. Solid-State Circuits*, vol. 27, pp. 142–153, Feb. 1992.

[7] A. Nedungadi and T. R. Viswanathan, "Design of linear CMOS transconductance elements," *IEEE Trans. Circuits Syst.*, vol. CAS-31, no. 10, pp. 891–894, Oct. 1984.

[8] K. Bult and H. Wallinga, "A class of analog CMOS circuits based on the square-law characteristic of an MOS transistor in saturation," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 357–365, June 1987.

[9] Y. Tsividis, Z. Czarnul, and S. C. Fang, "MOS transconductors and integrators with high linearity," *Electron. Lett.*, vol. 22, no. 5, pp. 245–246, Feb. 27, 1986.

[10] C. H. J. Mensink, E. A. M. Klumperink, and B. Nauta, "On the reduction of the third order distortion in a CMOS triode transconductor," in *1996 IEEE Int. Symp. Circuits Syst.*, May 1996, vol. 1, pp. 223–226.

[11] P. K. Chan and G. Wilson, "Mobility degradation effects in CMOS differential pair transconductors," *Analog Integrated Circuits and Signal Processing 2*. Boston: Kluwer Academic, pp. 27–31, 1992.

[12] R. R. Torrance, T. R. Viswanathan, and J. V. Hanson, "CMOS voltage to current transducers," *IEEE Trans. Circuits Syst.*, vol. CAS-32, pp. 1097–1104, Nov. 1985.

[13] S. Szczepanski, A. Wyszynski, and R. Schaumann, "Highly linear voltage-controlled CMOS transconductors," *IEEE Trans. Circuits Syst.*, vol. 40, pp. 258–262, Apr. 1993.

[14] C. H. J. Mensink and B. Nauta, "CMOS tuneable linear current divider," *Electron. Lett.*, vol. 32, pp. 889–890, May 9, 1996.

[15] U. K. Moon and B. S. Song, "Design of a low-distortion 22-kHz fifth-order Bessel filter," *IEEE J. Solid-State Circuits*, vol. 28, pp. 1254–1264, Dec. 1993.

[16] C. H. J. Mensink, "Analogue transconductors for sub-micron CMOS technology," Ph.D. dissertation 1996.

[17] C. H. J. Mensink, B. Nauta, and H. Wallinga, "A 5.5 MHz CMOS low-pass filter using a 'soft-switched' transconductor," in *22nd Euro. Solid-State Circuits*, Sept. 1996, pp. 84–87.

[18] C. H. J. Mensink and B. Nauta, "Tuneable degenerated differential pair," European Patent 96 201 256.3, May 9, 1996.

[19] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*. New York: McGraw-Hill, 1988.

[20] E. Schatter, "Monolithic TV if system tab 440," *IEEE Trans. Broadcast Television Receivers*, vol. 18, pp. 158–163, Aug. 1972.

[21] N. J. Baars, "Symmetrical arrangement for forming a variable alternating-current resistance," U.S. Patent 4 131 809, Dec. 1978.

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