Flip-Flops for Accurate Multi-Phase Clocking: Transmission Gate versus Current Mode Logic

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Abstract— Dynamic Transmission Gate (DTG) and Current Mode Logic (CML) flip-flops are compared targeting power efficient multi-phase clock generation with low phase-error. The effect of component mismatches on multi-phase clock timing inaccuracies is modeled and compared, using the product of mismatch-induced jitter variance and power consumption as a Figure of Merit (FoM). Analytical equations are derived to estimate the Jitter-Power FoM for DTG and CML flip-flop based dividers. Simulations confirm the trends predicted by the equations and show that DTG Flip-Flops achieve a better FoM than CML Flip-Flops. The advantage increases for CMOS processes with smaller feature size and for a lower input frequency compared to f_T .

Index Terms—Timing, Phase error, Mismatch, Jitter, Multi-Phase Clock, Dynamic Transmission Gate Logic, Current Mode Logic, Divider, Flip-Flop Design, Low Power, Power Efficiency.

I. INTRODUCTION

Accurate multi-phase clock generation (MPCG) is essential for applications such as time interleaved Analog-to-Digital Converters [1] and wireless transceivers with high image rejection and harmonic rejection [2]. Phase errors degrade performance, e.g. by generating spurious tones [3] or limiting the achievable image and harmonic rejection [4].

Phase errors originate from delay deviations in MPCG blocks, e.g. delay elements in a delay locked loop or Flip-Flops (FF) in a shift-register or divider based MPCG [5]. Delay deviation can originate from the intrinsic properties (mismatch, noise) of the FF in a divider itself, or be caused by external influences like supply noise. To reduce the effect of supply noise, CML logic is often used. However, if the power supply noise can be adequately reduced by regulation and decoupling capacitors, the question is which type of FF offers the lowest jitter for a given amount of power. At the International Solid-State Circuits Conference we increasingly see DTG and standard CMOS logic dividers being used in PLLs and other jitter critical applications (e.g. refs [6, 7]). Good achieved results make it plausible that the supply decoupling problem can be solved to a sufficient degree. Among the intrinsic error sources, the timing errors due to mismatch are much larger than from device noise [8]. As mismatch is static, it adds a skew to a one-phase clock.

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However, if multiple clock phases contribute to one output at different moments in time, deterministic “mismatch jitter” results [5, 9]. Although mismatch-jitter can be reduced by digital calibration, this adds considerable cost and complexity.

As discussed in [5, 9], putting identical circuits in parallel (W-scaling, admittance/impedance scaling) reduces mismatch jitter at the cost of higher area and power consumption. Therefore, just comparing mismatch-jitter without considering power will give a highly sizing dependent result. Hence, we normalize jitter-variance to power consumption, as in [5] and use the Jitter-Power Figure of Merit (FoM):

$$FoM = \sigma_m^2 P_d \quad (1)$$

where σ_m is the timing variance due to mismatch and P_d is the power dissipation. This FoM has a fundamental basis and allows for comparing differently sized circuits fairly, similar to normalizing Oscillator Phase Noise or filter SNR to Power.

In [7], DTG-FFs were used and able to achieve very low phase errors at much lower power consumption than CML. Explorative simulations in [10] confirmed that DTG-FFs have significant advantages over CML-FFs for MPCG. However, we would like to understand under which conditions (frequency, number of phases) this is true and how technology affects the conclusions. Although the speed, power and power-delay has been analyzed fundamentally extensively for several FF topologies (e.g. [11, 12]), there is not much work to optimize Jitter-Power performance. This paper hence derives analytical equations to estimate Jitter, Power and FoM for both DTG and CML-FFs. Such analytical equations are valuable for insight, to guide the initial design of FFs.

In Section II the mismatch jitter and power consumption are modeled for DTG and CML-FFs and in Section III, the Jitter-Power FoMs are compared and verified by simulations. Section IV draws conclusions.

II. FLIP-FLOP POWER AND MISMATCH JITTER MODELING

We will now model the mismatch jitter and power consumption, for an N -phase MPCG/divider implemented using DTG-FFs and CML-FFs as depicted in Fig. 1 and 2 for the case $N=4$. The differential divider outputs (e.g. pair I+, I-) will be analyzed, so that a fair comparison can be made with a CML-FF which has a differential output. To provide insight, we keep the equations simple and use first order device equations rather than the more complicated short channel models. Evaluating (1) for a MPCG with N DTG-FFs we find:

$$FoM_{DTG-MPCG} = \sigma_{DTG-FF}^2 (N \cdot P_{DTG-FF} + P_{DTG-INBUF}) \quad (2)$$

where σ_{DTG-FF}^2 is the mismatch-jitter variance (variation in FF delay) and N is the number of phases.

Fig. 1a. MPCG using DTG-FFs ($N=4$)

Fig. 1b. One DTG-FF

P_{DTG_FF} and P_{DTG_INBUF} are power consumptions of a FF and input clock buffer respectively. As we aim for insight in FF design (used in a MPCG), we chose to analyze ‘FoM per flip-flop’. Thus we divide (2) by N to find a FF FoM, assuming all FFs are identical and contribute the same mismatch jitter:

$$FoM_{DTG-FF} = \frac{FoM_{DTG-MPCG}}{N} = \sigma_{DTG-FF}^2 \left(P_{DTG-FF} + \frac{P_{DTG-INBUF}}{N} \right) \quad (3)$$

For a MPCG with CML-FFs as in Fig. 2, however, only $N/2$ FFs are required because differential outputs are already available. Thus its expression of FoM per FF becomes:

$$FoM_{CML-FF} = \frac{FoM_{CML-MPCG}}{(N/2)} = \sigma_{CML-FF}^2 \left(P_{CML-FF} + \frac{2P_{CML-INBUF}}{N} \right) \quad (4)$$

We assumed that the presence of start-up initialization switches can be neglected, and that all FFs are triggered by the same edge of a shared clock. Thus a deterministic time shift in that clock edge is common for all the FFs and does *not* contribute to phase errors *between* clock phases. So, even if a large number of cascaded buffers is used *in front* of a FF to drive N big FFs, buffer timing errors fall out and the phase error is dominated by the FF. In contrast, if buffers are added *after* the FF, both the FF and the buffer contribute mismatch errors. To minimize total jitter, buffers should be added before the FF in case it has to drive a large capacitive load. As such buffers are generally scaled up (“tapered buffer chain”), the overall power consumption is dominated by the FFs and the *last* buffer preceding the FF, justifying just one clock buffer stage in the FoM model. In a master-slave D-FF the slave-latch drives the load and thus its delay variation renders mismatch-jitter. To improve FoM, the master-latch can be scaled down compared to the slave-latch. As this is possible for both logic families, for simplicity we keep the master and slave latch identical. We derive FoM equations for DTG-FFs in sub-section A and for CML-FFs in sub-section B.

A) FoM of a Dynamic Transmission Gate Flip-Flop

The mismatch-jitter of a DTG-FF (Fig. 1b) is the variation of clock-to-output delay. The critical delay path is drawn in Fig. 3. First we model the transmission gate delay modeled by its equivalent RC-time constant [13]. Here we take a

Fig. 2: MPCG with CML-FFs for $N=4$ (top),

simplified first order TG delay where the equivalent resistance is assumed to be constant over the transition range (Fig. 6.48 in [14]). Using the simple square-law MOS transistor model, the equivalent TG resistance can be obtained. From the TG equivalent resistance, the delay from the 50% input level to the 50% output level can be written as:

$$t_{TG} = \frac{2(\ln 2)V_{DD}(C_L + C_{int})}{K_n(V_{DD} - V_{Tn})^2 + K_p(V_{DD} - |V_{Tp}|)^2} \quad (5)$$

where C_L is the output capacitance, $K = \mu C_{ox} W/L$, V_T is the threshold voltage, while suffices n and p refer to nMOS and pMOS transistors respectively. Equation (5) is valid for both high-to-low (H-L) and low-to-high (L-H) transitions.

We modify the equivalent resistance by adding the driving inverter resistance (see Fig. 3) to estimate the delay better. For a L-H output transition, the pMOS in the inverter is active and operates in the triode region. The same is true for the nMOS for a H-L transition. Adding these resistances, the delay for the differential (anti-phase) output, which is the average of an H-L and L-H delay, can be written as:

$$T_{TG-t_AVG} = \ln 2 \left\{ \frac{\frac{2V_{DD}}{K_n(V_{DD} - V_{Tn})^2 + K_p(V_{DD} - |V_{Tp}|)^2} + \frac{1/2}{K_n(V_{DD} - V_{Tn})} + \frac{1/2}{K_p(V_{DD} - |V_{Tp}|)}}{1} \right\} (C_L + C_{int}) \quad (6)$$

where C_{int} is the load capacitance due to the transmission gate itself. The last two resistance terms in (6) model inverter triode resistances for equally sized inverter and TG transistors. In practice also: $V_{Tn} \approx V_{Tp}$ and $K_n \approx K_p$ (7)

Using (7) and defining the ratios below, (6) can be written as:

$$T_{TG-t_AVG} = \frac{(\ln 2)L^2(\gamma_c + 0.5 + r_l)(1 + r_\mu)(2V_{DD} - V_{Tn})}{\mu[(V_{DD} - V_{Tn})^2]} \quad (8)$$

where r_l is the loading ratio of a FF, i.e. its C_L expressed in terms of its input capacitance,

Fig. 3: Clock input to the output delay path of a DTG-FF

Fig. 4: Clock-to-output delay of DTG-FF; model and simulations.

Ratio r_μ is the pMOS to nMOS width-ratio (W_p/W_n , typically 2.5, equal to the electron-to-hole μ -ratio), μ is the mobility of an nMOS transistor, γ_c is the ratio of drain to gate capacitance of a MOS transistor (bias independent for simplicity). Although the delay equation (8) neglects the effect of finite rise/fall time, it gives a reasonable estimate (see Fig. 4).

Mismatch jitter is now obtained taking partial derivatives of (6). Applying approximation (7) and after some algebra we can obtain the mismatch-jitter variance:

$$\sigma_{t_{DTGFF}}^2 = \frac{(\ln 2)^2 V_{DD}^4 L^4 (\gamma_c + r_l + 1.5)^2}{4 \mu^2 r_\mu (1 + r_\mu)^{-3} (V_{OD})^4} \left[(1 + d_o^2) \frac{\sigma_{K_n}^2}{K_n^2} + \frac{(4 + d_o^2) \sigma_{V_{Tn}}^2}{(V_{OD})^2} \right] \quad (9)$$

Here $\sigma_{V_{Tn}}$ and σ_{K_n} are the standard deviation of V_{Tn} and K_n mismatch respectively, assumed to be the same for a pMOS. The overdrive $V_{OD} = (V_{DD} - V_{Tn})$ and d_o is the normalized overdrive ratio of V_{OD} w.r.t. V_{DD} . As the total equivalent device size at the output node is bigger than the flipflop size, its capacitive mismatch is less important than K mismatch and it is neglected. When used inside an MPCG, each FF's output drives another FF along with the external load. To take this into consideration, we replaced r_l by $(r_l + 1)$ in (9).

The power consumption of a CMOS inverter can be approximated in terms of its nMOS gate capacitance, C_{gn} as,

$$P_{INV} = f_o V_{DD}^2 C_{gn} (1 + r_\mu) (\gamma_c + r_l) \quad (10)$$

where f_o is the output clock frequency. This assumes that the dynamic charging/discharging power is dominant over short-circuit-power and leakage power. The dynamic power consumption of a DTG-FF (Fig. 1b), can be expressed as:

$$P_{DTG-FF} = f_o V_{DD}^2 C_{gn} (1 + r_\mu) [2(3\gamma_c + 1) + r_l] \quad (11)$$

And the input buffer power consumption per FF is:

$$P_{DTG-INBUF} = 2 f_o V_{DD}^2 C_{gn} (1 + r_\mu) N \quad (12)$$

where the input clock frequency, f_i is expressed as $N f_o$. With the help of (1), (3), (9) and (12), and some algebra we get:

$$FoM_{DTG-FF} = \frac{f_o V_{DD}^4 L^4 C_{OX}}{\mu^2 (V_{OD})^4} F_{DTG}(r) \left[\frac{(4 + d_o^2) A_{V_{Tn}}^2}{(V_{OD})^2} + (1 + d_o^2) A_{K_n}^2 \right] \quad (13)$$

where $A_{V_{Tn}}$ and A_{K_n} are the technology dependent mismatch constants and $F_{DTG}(r_l)$ is a function which depends on the circuit topology used in the DTG-FF. For Fig. 1 it is:

$$F_{DTG}(r_l) = \frac{[2(3\gamma_c + 1 + N) + r_l](\gamma_c + r_l + 1.5)^2}{4(\ln 2)^{-2} r_\mu (1 + r_\mu)^4} \quad (14)$$

Here we approximate the MOS gate capacitance as $C_{OX} \cdot W \cdot L$. As the FoM is by its definition independent of admittance scaling, it only makes sense to optimize the FoM of the FF by changing width-ratios such as r_μ and r_l . We used $r_\mu = 2.5$ to match the rise and fall delays of the FF. The clock-buffer size is chosen to be close to its optimum 2.5 [15] for minimum power and mismatch-jitter product.

To optimize FoM, we see that lowering V_{DD} is very effective, while short channels (small L) are also very beneficial. When N is increased, the FoM increases via F_{DTG} according to (13) assuming f_o is constant. This is expected since for constant f_o and higher N , f_i goes up, increasing dynamic power proportionally, whereas mismatch jitter remains the same according to (11). However, if we keep the f_i constant and increase N , f_o will decrease and thereby decrease the dynamic power and hence the FoM.

B) FoM of a Current Mode Logic Flip-Flop (CML-FF)

The CML-FF in Fig. 2 (top) consists of two identical CML master-slave latches. The delay variation of CML-FF, same as that of a CML latch (Fig. 2, bottom) is derived in analogy to that of a CML buffer as in [5]. For cascaded CML buffers the output load capacitance is dominated by the input transistors of the next CML stage. To minimize the load capacitance for the previous stage, the width of the nMOS has to be just enough to flip the bias current from one load resistor R_b to the other, see CML buffer in Fig. 2, bottom. In that case, input transistor overdrive voltage is the same as the voltage swing V_s . Thus the bias current of a CML buffer (I_B) or a CML latch (I_L) in a CML-FF can be related to its voltage swing (V_s) as:

$$I_B = \mu C_{OX} \frac{W_B}{2L} V_s^2, \quad I_L = \mu C_{OX} \frac{W_L}{2L} V_s^2 \quad (15)$$

where W_B and W_L is the width of input transistor of the buffer and the latch respectively. Using (15), the mismatch jitter of the FF given in [5] can be re-written as:

$$\sigma_{t_{CML}}^2 = t_{CML}^2 \left[\frac{\sigma_{\delta C_L}^2}{C_L^2} + \frac{\sigma_{\delta R}^2}{R^2} + \frac{1}{(\ln 2 V_s)^2} \left\{ \sigma_{V_{Tn}}^2 + \frac{V_s^2}{4} \left(\frac{\sigma_R^2}{R^2} + \frac{\sigma_{K_n}^2}{K_n^2} \right) \right\} \right] \quad (16)$$

As power consumption of a CML buffer is $V_{DD} I_B$, we obtain the CML buffer FoM from (16) in terms of basic technology, design and mismatch parameters as:

$$FoM_{CML_buf} = \frac{V_{DD} C_{OX} L^2 (\gamma_c + r_l)^2}{2\mu} \left\{ \frac{4 A_{V_{Tn}}^2}{V_s^2} + A_{K_n}^2 + \frac{3 A_R^2}{r_{RM}} \right\} \quad (17)$$

Where r_{RM} is the ratio of resistor and the input nMOS device area and A_R is a resistor mismatch constant. Here we ignore load capacitance mismatch (see Section-IIA) for simplicity. The load capacitance is modeled via load ratio r_l .

Fig. 5a: Power consumption of DTG and CML

Fig. 5b: Mismatch-jitter of DTG and CML

Fig. 5c: MPCG FoM for DTG and CML

Table I: Parameters for Jitter-Power Estimations in a 90 nm CMOS Process

Parameter	Value	Parameter	Value
f_o	1 GHz	γ_c	0.5
$V_{Th}=V_{Tp}$	350 mV	μ (nMOS)	$8.5E-3 \text{ m}^2/(\text{Vs})$
C_{ox}	$18 \text{ fF}/\mu\text{m}^2$	r_μ	2.5
L (Effective)	75 nm	A_{Vi}	$3.7 \text{ mV}^*\mu\text{m}$
V_S	400 mV	A_k	$1 \%*\mu\text{m}$
r_{RM}	4.6	$A_R(n+poly)$	$1.4 \%*\mu\text{m}$

To get the CML-FF FoM used in a MPCG, we need to know the relation between I_L and I_B . The ratio of I_L and I_B is designed such that both buffer and FF have the same output slew-rate. This is to have an equal distribution of mismatch-jitter among cascaded stages. The clock buffer drives $N/2$ CML-FFs or N CML latches and the latch drives $(r_l+2+\gamma_c)$ times its total input-capacitance. Thus the buffer and CML-FF input transistor width ratio (also current ratio) is:

$$\frac{I_B}{I_L} = \frac{W_B}{W_L} = \frac{N}{r_l + 2 + \gamma_c} \quad (18)$$

Hence, the total power consumption per FF is:

$$P_{CML-FF} + \frac{2P_{CML-INBUF}}{N} = \left(2I_L + \frac{2I_B}{N}\right)V_{DD} \quad (19)$$

Changing (17) according to the load condition of a CML-FF in a MPCG and using (4) and (19) we obtain:

$$FoM_{CML-FF} = \frac{V_{DD}C_{ox}L^2}{\mu} F_{CML}(r_l) \left\{ \frac{4A_{VTn}^2}{V_S^2} + A_{Kn}^2 + \frac{3A_R^2}{r_{RM}} \right\} \quad (20)$$

where F_{CML} is a function of r_l specific to CML MPCG:

$$F_{CML}(r_l) = \left\{ \frac{r_l + 4\gamma_c + 3}{r_l + 4\gamma_c + 2} \right\} (r_l + 2\gamma_c + 2)^2 \quad (21)$$

Two design choices can improve the FoM in (20): increasing the voltage swing (reduces V_T -mismatch effect), and reducing the load ratio (reduces the load capacitance and delay). We simulated with 1.2 V of power supply in a 90 nm CMOS technology and used 0.4 V of voltage swing which keeps all transistors more or less in saturation. The load ratio affects FF-delay and the mismatch-jitter variance in a similar manner, so that FoM and delay are proportional when V_{DD} and V_S is fixed. Thus low delay is preferred as in [5].

III. COMPARISON OF MPCG WITH DTG-FF AND CM-FF

To compare model with simulation, we calculated the power, mismatch-jitter and FoM using the values in Table for a 90 nm CMOS process. We simulated 4-phase MPCGs for an input frequency $f_i = 4 \text{ GHz}$ and slew-rate of 48 V/ns . The DTG-FF nMOS width is $16 \mu\text{m}$ and the CML-FF

($R = 67 \text{ ohm}$, $I_L = 6 \text{ mA}$) input device is $55 \mu\text{m}$ so that the input capacitance considering ratio r_μ is equal for both FFs.

For mismatch jitter, we did Monte Carlo simulations with 100 iterations for ‘only mismatch’ variations. The power consumption (P_d) and the mismatch-jitter (Mj) model results are compared with simulation results in Fig. 5a and Fig. 5b respectively with changing load capacitance. The power consumption has some deviation from the model due to the square-law-model inaccuracy. Simulated DTG-FF Mj is less than modeled, as we assumed equal A_{VT} for the pMOS and nMOS (actually pMOS mismatch is less). In contrast, simulated CML-FF Mj is more than modeled due to the approximated first order delay equation used. We accept these model errors to keep model equations simple. The simulated delay, power, Mj and FoM are shown in Table 2 for $r_l=1$ for both FFs. A column for $r_l=1/8$ is added for DTG, where device width is increased keeping the load capacitance the same. It demonstrates that DTG Mj can be pushed down by W-scaling at the cost of power, at relatively constant FoM.

Table II: Comparison of MPCG for $C_L=50\text{fF}$, $N=4$ (simulation)

Parameter	DTG, $r_l=1$	DTG, $r_l=1/8$	CML, $r_l=1$	Unit
Delay	19	17	22	ps
P_d	6	67.4	42.5	mW
Mj (std.)	54.5	18.8	87	fs
FoM	17.5	23.7	321	Wfs^2

As both power and mismatch comparison is device size dependent, we compare FoM to get size independent comparison. The FoM is compared to in Fig. 5c. Deviations in FoM exist up to about a factor of two, however the difference between the two logic families is significantly more than the model error. Expressed analytically, the FoM-ratio can be found from (13) and (20):

$$\frac{FoM_{CML-FF}}{2FoM_{DTG-FF}} = \frac{\mu(V_{OD})^4 F_{CML}}{2f_o V_{DD}^3 L^2 F_{DTG}} \frac{\left\{ \frac{4A_{VTn}^2}{V_S^2} + A_{Kn}^2 + \frac{3A_R^2}{r_{RM}} \right\}}{\frac{4 + d_o^2}{V_{OD}^2} A_{VTn}^2 + [1 + d_o^2] A_{Kn}^2} \quad (22)$$

taking into account that a DTG-MPCG needs N FFs whereas the CML-MPCG needs only $N/2$ (see Fig. 1a and 2). The ratio in (22), say R_{FoM} , can also be written as:

$$R_{FoM} = \frac{\pi f_T V_{OD}^5 F_{CML}}{f_o V_{DD}^3 V_S^2 F_{DTG}} \frac{\left\{ 4A_{VTn}^2 + V_S^2 A_{Kn}^2 + \frac{3V_S^2 A_R^2}{r_{RM}} \right\}}{(4 + d_o^2) A_{VTn}^2 + V_{OD}^2 (1 + d_o^2) A_{Kn}^2} \quad (23)$$

where f_T is nMOS unity gain frequency, defined as:

$$f_T = \frac{\mu g_m}{2\pi C_{gs}} = \frac{\mu V_{OD}}{2\pi L^2} \quad (24)$$

Fig. 6a: DTG, CML-MPCG FoM vs. frequency

Fig. 6b: FoM ratio with changing N Fig. 6c: Simulated FoM for fixed C_{in} and C_L

In (23) the ratio of the FoMs can be separated in three parts: the first part has strong technology dependence and its proportional to f_T . With CMOS technology downscaling the f_T increases, and so does the ratio, explaining why DTG MPCGs indeed become relatively better compared to CML in scaled CMOS technologies. The 2nd F -ratio term is a function of design parameters related to circuit topology. The low capacitance in a DTG-FF as there is no cross-coupled pair, and its fast path from clock to output helps to boost the ratio through smaller F_{DTG} . The third term in (23) is a function of the mismatch parameters and close to one, so it does not affect the comparison result significantly.

Fig. 6a shows this advantage for wide output frequency range. In this case the simulation was done for a load capacitance of 10 fF and $r_i=1$. When we change the number of phases, we can either keep the input frequency constant or the output frequency. From (23) FoM ratios for both scenarios are plotted in Fig. 6b for $f_o=100$ MHz and $f_i=4$ GHz. DTG-FF performs better (ratio > 1). In Fig. 6c we compare the simulated FoM for changing FF sizes, with fixed input (at INCLK+ and INCLK- in Fig. 1 and 4) and output capacitances, also shows an order of magnitude better FoM for DTG. In this case, extra buffers have been added in the clock path when larger FF devices are used. Although the CML-FF FoM is more robust to temperature (~5% for -10 to 85°C) and process variations (~15%) than the DTG-FF (~10% and 55% respectively), a big advantage remains.

Therefore for low power and jitter performance, DTG logic is preferred for wide-band operation, e.g. for flexible software defined radio applications. This is because its power and FoM are automatically reduced for lower frequency (1st term in (13)) whereas CML always dissipates the current that required at the highest frequency of operation.

IV. CONCLUSIONS

DTG and CML flip-flops have been compared fundamentally with respect to their potential to realize accurate multi-phase clocks in a power efficient way. The comparison is based on a FoM which quantifies the product of mismatch induced timing jitter variance and power dissipation, normalized for admittance scaling effects. First order analytical expressions are derived and confirmed by simulations to model mismatch jitter, power dissipation and Jitter-Power FoM. The analytical expressions are used to compare flip-flops and also to design them for low FoM.

Comparison shows that DTG flip-flops outperform CML in Jitter-Power FoM in 90 nm CMOS technology. This is mainly because DTG flip-flops only consume power during switching. Moreover, they have less capacitance (no need for a cross-coupled pair) which reduces both power and jitter. The advantage scales roughly with f_T/f_o so technology scaling benefits DTG logic compared to CML (23). These equations can be useful in selecting flip-flop for multiphase generation, for different technology and frequency of operation.

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