A 300–800 MHz Tunable Filter and Linearized LNA Applied in a Low-Noise Harmonic-Rejection RF-Sampling Receiver

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***Abstract*—A multiband flexible RF-sampling receiver aimed at software-defined radio is presented. The wideband RF sampling function is enabled by a recently proposed discrete-time mixing downconverter. This work exploits a voltage-sensing LNA preceded by a tunable *LC* pre-filter with one external coil to demonstrate an RF-sampling receiver with low noise figure (NF) and high harmonic rejection (HR). The second-order *LC* filter provides voltage pre-gain and attenuates the source noise aliasing, and it also improves the HR ratio of the sampling downconverter. The LNA consists of a simple amplifier topology built from inverters and resistors to improve the third-order nonlinearity via an enhanced voltage mirror technique. The RF-sampling receiver employs 8 times oversampling covering 300 to 800 MHz in two RF sub-bands. The chip is realized in 65 nm CMOS and the measured gain across the band is between 22 and 28 dB, while achieving a NF between 0.8 to 4.3 dB. The IIP2 varies between +38 and +49 dBm and the IIP3 between −14 dBm and −9 dBm, and the third and fifth order HR ratios are more than 60 dB. The LNA and downconverter consumes 6 mW, and the clock generator takes 12 mW at 800 MHz RF.**

***Index Terms*—Aliasing, amplifier, anti-aliasing, CMOS, cognitive radio, CR, discrete-time mixing, distortion, filter, harmonic rejection, LC filter, low-noise amplifier, LNA, matching, nonlinearity, oversampling, pre-filter, receiver, RF sampling, sampling, sampling receiver, software-defined radio, SDR, software radio, SWR, tunable filter, voltage-sensing LNA, voltage-sensing receiver, voltage mirror, wideband, wideband receiver.**

I. Introduction

RECENTLY, there has been a growing research interest into RF-sampling receivers [1]–[6]. Moving the sampling closer to the antenna can be viewed as an intermediate step in the direction of a software-radio receiver with the full ADC close to antenna, targeting at greater flexibility. To serve software-defined radio (SDR) applications, wideband sampling receivers are desired to cover many RF bands. However, most of the reported RF-sampling receivers are dedicated to narrowband applications such as Bluetooth [3], GSM [4], [6] and WiMax [5]. In fact, compared to mixing, the traditional RF-sampling techniques present some extra challenges when used in wideband applications, such as maintaining quadrature over a wide band [7] and aliasing of wideband noise and interference.

Recently, a wideband sampling technique, i.e., discrete-time (DT) mixing, has been proposed [8], [9, Ch. 3] which can deliver constant phase shift over a wide band for frequency-independent quadrature demodulation and wideband harmonic rejection (HR) for reduced aliasing. Thus, DT mixing can be suitable to wideband SDR applications. However, the downconverter in [8] and [9] has a few critical performance limitations. Without a low-noise amplifier (LNA), the gain is low (2.5 dB) and the noise figure (NF) is high (18 dB). Furthermore, the first unrejected harmonic is the seventh, which may still cause aliasing which results in degraded NF and signal-to-interference ratio. Moreover, the HR ratio is severely affected by amplitude and phase accuracy, and the worst-case HR ratio is around 25 dB (among multiple samples) while at least 60 dB is often required in practice, e.g., for the television broadcasting applications [10].

To further reduce the aliasing, in this paper we apply a front-end tunable *LC* filter technique which simultaneously provides passive voltage pre-gain[1] and harmonic filtering while consuming no power. Pre-gain can improve the NF and the HR at the same time. However, it can degrade the receiver linearity. Therefore, we will also present a simple voltage amplifier topology namely an enhanced voltage mirror, applied in the LNA stage, to improve the third-order linearity. This work aims at an explorative study of new circuit techniques and does not focus on a specific standard.

Integrated with a HR downconverter [8], [9], the complete sampling receiver can cover the band of 300 MHz to 800 MHz which serves as the television broadcasting band and the recently proposed cognitive radio band [11]. The receiver can achieve a NF as low as 0.8 dB due to the pre-gain, reduced source noise folding, and reduced LNA noise folding. The total HR is also improved from the worst case of 25 dB for the basic downconverter to at least 60 dB for the complete receiver. In the mean time the receiver achieves a moderate third-order input intercept point (IIP3) of higher than −14 dBm. The combination of the *LC* filter and the LNA can also add more than 20 dB gain

Manuscript received October 02, 2009; revised November 24, 2009; accepted January 13, 2010. Current version published April 23, 2010. This paper was approved by Guest Editor Albert Wang.

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Digital Object Identifier 10.1109/JSSC.2010.2041403

[1]We refer to this voltage gain as a passive "pre-gain" meaning that it is achieved before the first active amplification stage, i.e., the LNA.

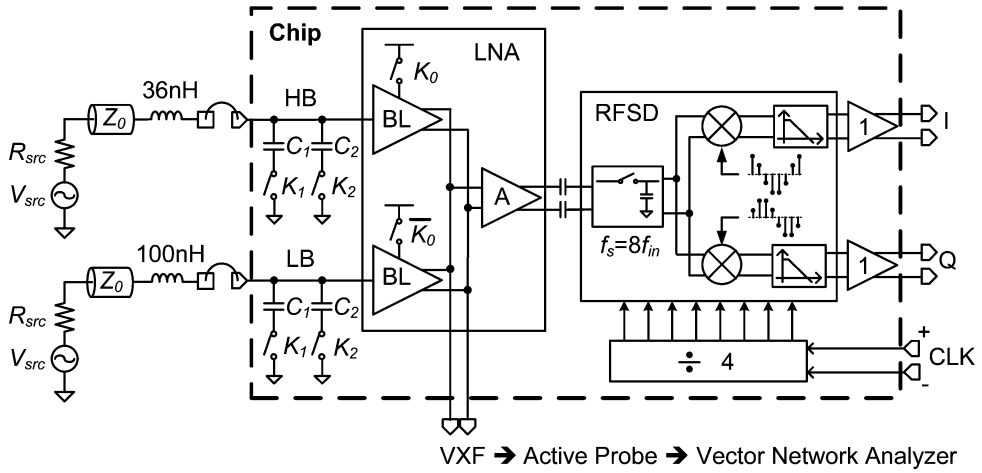


Fig. 1. The multi-band RF-sampling receiver.

before downconversion thereby reducing the noise contribution from the later stages.

Compared to [12], this paper extends the analysis for the *LC* filter especially its effect on HR and discusses its transfer function under practical non-ideal conditions, and also extends the analysis for the LNA linearity. We will present additional measurement results to address the robustness of the IIP3-enhancement technique. Compared to [8] which presented the downconverter only, this paper describes a complete RF-sampling receiver with an emphasis on the tunable *LC* pre-filter and the LNA and presents measurement results for the complete receiver.

The architecture of the complete RF-sampling receiver is described in Section II, with a brief review of the DT-mixing downconverter. Section III focuses on the *LC* filter, analyzing its characteristics and implementation issues. Section IV focuses on the LNA, analyzing its gain behavior and the mechanism of distortion compensation. The measurement results of the complete receiver are presented in Section V and conclusions are drawn in Section VI.

II. RF-Sampling Receiver Architecture

Fig. 1 shows the multi-band zero-IF sampling receiver architecture, in this case for two sub-bands. It consists of two *LC* filters, an LNA, and an RF-sampling downconverter (RFSD) driven by a frequency divider. Two input signal paths are used to cover a 300–800 MHz bandwidth in two sub-bands, the high band (HB) and the low band (LB). These paths can be connected to different antennae as shown, *but can also be connected to a single antenna which can cover the full bandwidth*. The antennae deliver signals to a pair of *LC* networks which are followed by the receiver circuit. The inductors are off-chip while the rest of the components are on-chip such as two switchable capacitor banks, an LNA with two selectable single-input differential-output baluns (BL), and an RFSD with second to sixth-order HR driven by a divide-by-4 circuit producing an eight-phase local oscillator (LO) signal.For measurement purposes, after the RFSD, the quadrature baseband outputs are buffered via source followers with a voltage gain of 1. The differential VXF nodes are used to test the voltage transfer function of the *LC* filter together with the balun stage, via an active probe.

The RFSD in Fig. 1 employs a recently proposed DT mixing architecture [8], [9]. The first stage is an oversampler with an effective sample rate of 8 times the input carrier frequency, i.e., $f_s = 8f_c$. The second stage contains I/Q DT mixers which down-convert the RF signal to zero-IF with second to sixth-order HR. Oversampling and HR relaxes RF pre-filtering and reduces noise and interference folding. The third stage consists of infinite-impulse response (IIR) low-pass filters, which remove undesired interference and serve as antialiasing filters before decimation to a lower sampling rate.

The RFSD alone has a measured gain of -0.5 to 2.5 dB, an NF of 18 to 20 dB, and an IIP3 of $+10$ dBm [9, Ch. 3]. Due to mismatches, the minimum HR ratio is around 25 dB. The achieved NF is amongst the best published for voltage sampling downconverters, thanks to the reduced noise folding by employing oversampling and HR. However, the number of rejected harmonics is limited by the number of LO phases and the unrejected harmonics (seventh, ninth, etc.) still cause noise aliasing which degrade the NF. For the rejected harmonics (e.g., second to sixth), larger HR ratios are desired to counter strong interference.

III. Tunable *LC* Filter

To improve the HR ratio and to further reduce the noise aliasing, we apply a simple series *LC* filter structure as the first receiver stage, which can also provide voltage gain to reduce the NF.

A. Filter Concept

RF pre-filtering is often desired for two main reasons: 1) to attenuate strong out-of-band interferers to a level that can be handled by on-chip electronics; 2) to prevent mixer harmonic images to fold over the wanted signal.

It is well known that a series inductor and a capacitor to ground (Fig. 2) define a second-order low-pass filter, with peaking around resonance and attenuation at high frequencies. To suppress the LO harmonics it is sufficient to just use a

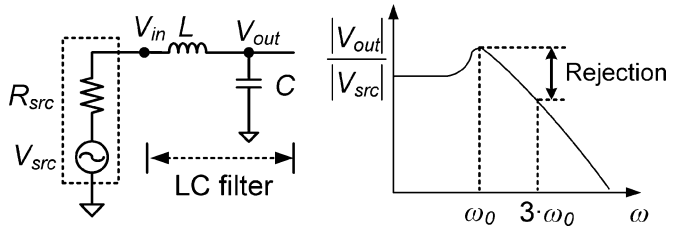


Fig. 2. A *simple* second-order *LC* filter with transfer function (logarithmic axis).

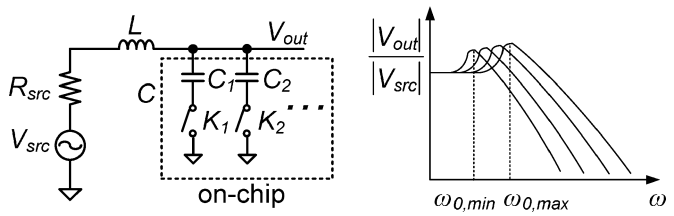


Fig. 3. A *tunable* second-order *LC* filter with transfer function (logarithmic axis).

low-pass filter. In addition, the peaking effect of the filter can be useful to boost the desired signal before an LNA [13], [14]. Here we make the filter tunable by means of switched capacitors (see Fig. 3) and apply it to create a flexible sampling receiver with improved NF and HR. Next we will derive expressions for the (harmonic) rejection as indicated in Fig. 2 and the gain over the tuning range as indicated in Fig. 3.

Assuming the source impedance is $R_{\rm src}$, the magnitude of the voltage transfer function of the filter in Fig. 2 can be derived as

$$\left|\frac{V_{\rm out}}{V_{\rm src}}\right|^2 = \frac{1}{(1-\omega^2\cdot LC)^2+(\omega\cdot R_{\rm src}C)^2} = \frac{1}{\omega^4\cdot L^2C^2+\omega^2\cdot(R_{\rm src}^2C^2-2LC)+1}. \quad (1)$$

The peak value of (1) over frequency can be found via the derivative of its denominator:

$$\frac{\partial(|V_{\rm src}/V_{\rm out}|^2)}{\partial\omega} = 4\omega^3\cdot L^2C^2+2\omega\cdot\left(R_{\rm src}^2C^2-2LC\right) = 0. \quad (2)$$

Besides the trivial solution at $\omega=0$, the other solution to (2) is

$$\omega_p = \sqrt{\frac{2L-R_{\rm src}^2C}{2L^2C}} = \frac{1}{\sqrt{LC}}\cdot\sqrt{1-\frac{1}{2}\cdot\left(\frac{L/C}{R_{\rm src}^2}\right)^{-1}} = \omega_0\cdot\sqrt{1-\frac{1}{2Q^2}} \quad (3)$$

where Q is the quality factor of the series *RLC* network ($Q=\sqrt{(L/C)}/R_{\rm src}$), $\omega_{\rm p}$ is the peaking frequency and ω_0 is the resonance frequency of the *LC* tank. From (3), we can see that $\omega_{\rm p}$ lies below ω_0, where Q defines how much the difference is between them.

Substituting (3) into (1), the magnitude of the transfer function at $\omega_{\rm p}$ can be derived as

$$\left|\frac{V_{\rm out}}{V_{\rm src}}\right|_{\omega=\omega_p} = \frac{1}{\sqrt{\left(1-\omega_p^2\cdot LC\right)^2+(\omega_p\cdot R_{\rm src}C)^2}} = \frac{1}{\sqrt{\frac{1}{4Q^4}+\frac{1}{Q^2}\left(1-\frac{1}{2Q^2}\right)}} = \frac{Q}{\sqrt{1-\frac{1}{4Q^2}}}. \quad (4)$$

Based on (1) we can see that the gain at the resonance frequency ω_0 is exactly Q. For high Q the difference between ω_0 and $\omega_{\rm p}$ becomes small and the peak gain at $\omega_{\rm p}$ is close to Q. Even for a low Q of 2, we still have $\omega_{\rm p}=0.935\omega_0$ based on (3) and $|V_{\rm out}/V_{\rm src}|=1.03Q$ at $\omega_{\rm p}$ based on (4), which is only 3% larger than the gain at ω_0. Therefore, we may use the gain at ω_0 which is easier to define.

In Fig. 2, at the resonance frequency $\omega_0=1/\sqrt{(LC)}$, the *LC* input voltage $V_{\rm in}$ is equal to 0 since the series *LC* tank is a short circuit at ω_0. Therefore, the current flowing into the *LC* filter is $V_{\rm src}/R_{\rm src}$, and the voltage magnitude on the capacitor can be written as

$$|V_{\rm out}|_{\omega=\omega_0} = \frac{|V_{\rm src}|}{R_{\rm src}}\cdot\frac{1}{\omega_0 C} = |V_{\rm src}|\cdot\frac{\omega_0 L}{R_{\rm src}} = \frac{\sqrt{L/C}}{R_{\rm src}}\cdot|V_{\rm src}| = Q\cdot|V_{\rm src}| = 2Q\cdot|V_{\rm match}| \quad (5)$$

where the actual source voltage $|V_{\rm src}|$ is twice as large as the voltage $|V_{\rm match}|$ in case of impedance matching, i.e., $V_{\rm match}=V_{\rm src}/2$.

To benefit from resonant peaking ($|V_{\rm out}|>|V_{\rm src}|$) we want $Q>1$. To get a coarse estimate of the required L and C, we suppose that the desired gain is $G_{\rm d}=Q$ at ω_0, and then find $L=G_{\rm d}\cdot R_{\rm src}/\omega_0$ and $C=1/(G_{\rm d}\cdot R_{\rm src}\cdot\omega_0)$. For $G_{\rm d}=2$ and $R_{\rm src}=50\Omega$, at frequencies below 1 GHz, this leads to inductors larger than 15 nH and capacitors larger than 1.5 pF. Clearly, such inductors are not easily realized on chip and even if practical their Q is low. Off-chip inductors can be small, e.g., surface-mounted device (SMD), and with higher Q, and also they are relatively low cost compared to, for instance, SAW filters. If the receiver has a single-ended RF input, only one external inductor is needed for each sub-band.

If $R_{\rm src}$ is defined by the antenna impedance in a radio receiver (usually 50Ω), for a sufficiently high *L/C* ratio, Q can be larger than 1 and thus this filter can realize "passive" voltage gain around ω_0. It can improve the receiver sensitivity, without adding noise and power consumption. This property is favorable compared to SAW filters, which often introduce significant loss.

As shown in Fig. 2, since inductors conduct DC signal, the attenuation on the low-frequency side is limited. A simple second-order *LC* filter does not show a characteristic as sharp as most SAW filters, so the suppression of out-of-band interference is less. Whether this is acceptable depends on the application, the antenna characteristic and the linearity of the receiver.

Such an *LC* filter *does not* provide impedance matching, but *does* give useful voltage pre-gain around the resonance frequency. Moreover, the low-pass transfer function provides significant attenuation for RF signals at multiples of the sampling frequency, hence improving HR. The voltage pre-gain can boost the wanted signal and the improved HR reduces noise and interference aliasing. *Both features improve the NF of a wideband sampling receiver*.

One step further from the filter transfer function, we may quantify the improvement of HR ratio. Via (1), the gain for the nth harmonic of the *LC* resonance frequency can be written as

$$\left|\frac{V_{\rm out}}{V_{\rm src}}\right|_{\omega=n\cdot\omega_0} = \frac{1}{\sqrt{(1-n^2\cdot\omega_0^2\cdot LC)^2+(n\cdot\omega_0\cdot R_{\rm src}C)^2}} = \frac{1}{\sqrt{(n^2-1)^2+n^2/Q^2}}. \quad (6)$$

Since the gain at the fundamental harmonic $(n=1)$, i.e., ω_0, is equal to Q according to (6). For the nth harmonic $(n=2,3,4\ldots)$, we can achieve a HR improvement of

$$\begin{aligned}{\rm HR}_n &= 20\log_{10}(Q\cdot\sqrt{(n^2-1)^2+n^2/Q^2}) \\ &\approx 20\log_{10}[Q\cdot(n^2-1)]\left(\text{if } Q\gg\frac{n}{n^2-1}\right). \end{aligned} \quad (7)$$

Even for a low Q of 2, we can still get ${\rm HR}_3 = 24$ dB and ${\rm HR}_5 = 34$ dB. Please note that both the resonant peaking (Q) and the filter's second-order roll-off contribute to the HR ratio, as indicated in Fig. 2.

The filter in Fig. 2 is dedicated to one resonance frequency. To cover a wider frequency range, we would like to have a tunable ω_0. In theory, an arbitrary bandpass characteristic can be made by a combination of inductors and capacitors. For a high-order filter, tuning to another frequency, while maintaining the bandpass shape involves tuning all or at least many of its components. Hence, for simplicity of implementation it seems prudent to stick to low-order tunable filters. As inductors are not easily tunable and varactors often introduce nonlinearity, we aim to exploit MOS switches and linear metal capacitors for tuning, which can be digitally controlled, as shown in Fig. 3.

Switching the capacitor to tune the filter to another frequency also changes its gain, but this gain variation can be acceptable. If we keep the frequency tuning range[2] smaller than 40%, i.e., $\omega_{0,\max}/\omega_{0,\min} < 1.5$, the gain variation can be less than 3 dB. The gain variation depends on the fact that the tuning is achieved whether via switching inductors or capacitors.

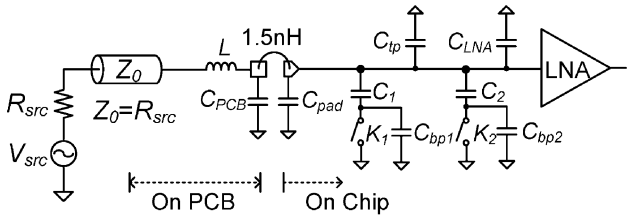
Based on (5), we can derive that if purely switching the capacitor, i.e., fix the inductor, the gain variation is

$$G_a/G_b = \omega_{0,a}/\omega_{0,b} = \sqrt{C_b/C_a}. \quad (8)$$

That means the gain is proportional to the resonance frequency. Yet, by switching the inductor and fixing the capacitor, the gain variation is

$$G_a/G_b = \omega_{0,b}/\omega_{0,a} = \sqrt{L_a/L_b}. \quad (9)$$

[2]The tuning range is defined as the ratio of the absolute tuning bandwidth to the middle frequency of the tuning band, i.e., $2(\omega_{0,\max}-\omega_{0,\min})/(\omega_{0,\max}+\omega_{0,\min})$.



$C_{fix}=C_{LNA}+C_{pad}+C_{tp}+C_{PCB}=0.17+0.1+0.17+0.25=0.69$pF

K_1K_2	C_{fix} (pF)	C_{tune} (pF)	C_{tot} (pF)
00	0.69	0.36+0.24	1.29
01	0.69	0.36+0.5	1.55
10	0.69	1.2+0.24	2.13
11	0.69	1.2+0.5	2.39

Fig. 4. Sources of parasitic capacitance in the *LC* filter.

That means the gain is inversely proportional to the resonance frequency in case of switching inductors to tune the working band (Section III-B).

B. Implementation

Fig. 1 shows the schematic of the implemented *LC* filter. Two on-board SMD inductors, 36 nH for high-band (HB) and 100 nH for low-band (LB), with two metal–oxide–metal (MOM) capacitors ($C_1 = 1.2$ pF, $C_2 = 0.5$ pF) for each inductor, are included to demonstrate the multi-band function. Which signal path in use is determined by enabling one of the balun-LNAs by setting K_0 to be 0 or 1. The band selection is achieved in two steps, a coarse selection and a fine tuning. The coarse selection is inherent in the LNA stage (K_0) which can be powered on/off to select which filter bank in use. The fine tuning is achieved by varying the capacitor values of the *LC* tank via digital bits (K_1, K_2).

Via the combination of selecting inductors and capacitors, we can set eight resonance frequency points (f_0) of the filter, i.e., controlling via three bits "$K_0K_1K_2$". These resonance frequencies are discrete points but the filter can continuously cover a large bandwidth by operating over a small bandwidth around each f_0 (Fig. 3).

However, the resonance frequency and the Q are heavily affected by the parasitic capacitance, as modeled in Fig. 4. The model includes the input capacitance of the LNA ($C_{\rm LNA}$), the pad capacitance ($C_{\rm pad}$), and the PCB capacitance ($C_{\rm PCB}$). $C_{\rm tp}$ indicates the top-plate parasitic capacitance of C_1 and C_2 together. $C_{\rm bp1}$ and $C_{\rm bp2}$ indicate the bottom-plate parasitics of C_1 and C_2 respectively, as well as the parasitics of their switches.

The parasitics of C_1 and C_2 are about 10% of their nominal values and the parasitics of switches are about 0.4 pF due to large switches used for low on-resistance (1 Ω). Via simulation and estimation, we get $C_{\rm LNA} = 0.17$ pF, $C_{\rm pad} = 0.1$ pF, $C_{\rm tp} = 0.17$ pF, $C_{\rm bp1} = 0.52$ pF, and $C_{\rm bp2} = 0.45$ pF; $C_{\rm PCB}$ is about 0.25 pF (fitted after experiments). The table in Fig. 4

TABLE I
CALCULATED PARAMETERS OF THE IMPLEMENTED *LC* FILTER (FIG. 1)

	$K_0K_1K_2$	Total L (nH)	Total C (pF)	f_0 (MHz)	Q [a]	Gain=2Q (dB)	3rd|5th Harmonic Rejection (dB)	
HB	000	36	1.29	740	3.3	16	28	38
	001	36	1.55	670	3.0	16	27	37
	010	36	2.13	570	2.6	14	26	36
	011	36	2.39	540	2.5	14	26	35
LB	100	100	1.29	440	5.6	21	33	43
	101	100	1.55	400	5.1	20	32	42
	110	100	2.13	340	4.3	19	31	40
	111	100	2.39	320	4.1	18	30	40

[a] Refer to a 50Ω real impedance.

summarizes the total capacitance $C_{\rm tot}$ in each configuration of K_1K_2.

Table I lists the resonance frequency, the Q, and the HR ratio for each of the filter 3-bit settings $(K_0K_1K_2)$, calculated via (5) and (7)–(9). Please note that the voltage gain here is equal to $2Q$, referred to $V_{\rm match}$ in (5). The lowest Q in the whole band is 2.5, for $K_0K_1K_2 = 011$. The bondwire of 1.5 nH and the switch-on resistance of 1 Ω have a negligible effect to the filter performance. Also the quality factors of the on-board inductors are in the order of 30 to 40, which can only slightly affect the filter performance.

At resonance, the *LC* filter input impedance is 0 (short) instead of $R_{\rm src}$. Receivers without input matching have been proposed before, e.g., in [14]–[16]. Although this may complicate RF pre-filter design and may introduce issues with respect to reflections, it also has advantages. Note that for input matching there is a maximum power transfer, but it degrades the voltage by half, i.e., $V_{\rm match} = V_{\rm src}/2$ as shown in (5). For voltage sensing devices such as a MOSFET at $f \ll f_{\rm T}$, the maximum voltage transfer is more of interest, and an unmatched input may have advantages, e.g., lower NF, lower power consumption, and higher Q (no extra R from the matching device).

The inductors are placed very close to the chip, and 50 Ω transmission lines are used to connect the inductors to the antennae. If there is no impedance mismatch between the antenna and its connection lines, the voltage amplitude sensed by the LNA input is still well defined by (5), independent of the line length [15]. Moreover, since here we deal with frequencies below 1 GHz, it is often possible to use PCB lines between the antenna and the chip which are much shorter than the wavelength. In that case, the transmission line effect can be made negligible.

The reflection due to the impedance mismatch at the input of the *LC* filter will create standing waves on the transmission line. If the transmission line has a negligible length or is well matched with antenna, the antenna will absorb the reflected wave and radiate it back into the air. But this reflection should not violate the radio regulation, since any obstacle in the surroundings may cause the same consequence.

According to (5), the gain is well defined if the source impedance is well defined. However, antenna impedance is usually not purely resistive but involves reactive parts such as inductance and capacitance. Nevertheless, for a well-designed antenna, its impedance in the desired band can be approximated as purely resistive while the reactive parts resonate in that band. The resonant effect of the antenna can provide attenuation of interference and hence further improve the HR ratio.

In practice, the antenna impedance can also vary with the environment, e.g., due to the reflection of electromagnetic waves by surroundings. If an antenna is aimed at achieving $\rm S_{11} < -10$ dB referred to a 50Ω source, the real part of the antenna impedance varies in the range of 25Ω to 100Ω. This variation represents a change of Q by 0.5 to 2 times from the nominal 50Ω case.

According to (5), the pre-gain variation is directly proportional to the Q variation. However, for the NF the variation is less because the antenna noise voltage also changes when its impedance varies. This effect can be seen from the overall noise at the output of the *LC* filter:

$$\frac{\overline{v_{n,{\rm after}LC}^2}}{\Delta f} = 4kTR_{\rm src}\cdot\left(\frac{\sqrt{L/C}}{R_{\rm src}}\right)^2 = 4kT\cdot\frac{L/C}{R_{\rm src}}. \quad (10)$$

If the antenna impedance changes by a factor of 2, the gain changes by 6 dB and the NF changes by 3 dB in the worst case, i.e., when the antenna noise is much smaller than the noise from the receiver (the LNA and the downconverter). In general, the NF variation is less than 3 dB, depending on how much the antenna noise is boosted by the passive pre-gain. If the antenna noise is dominating due to a high passive pre-gain, then the NF variation can be negligible. In case that the variation is not acceptable, additional measures might be taken to adaptively transform the antenna impedance. Anyhow, the variation of antenna impedance can also be problematic in a receiver *with* input impedance matching.

IV. AMPLIFIER WITH DISTORTION COMPENSATION

Since the presented *LC* filter provides pre-gain before the LNA stage, the required linearity of the LNA is hence raised. Now we will propose a simple amplifier topology to construct a balun-LNA, which can provide IIP3 enhancement.

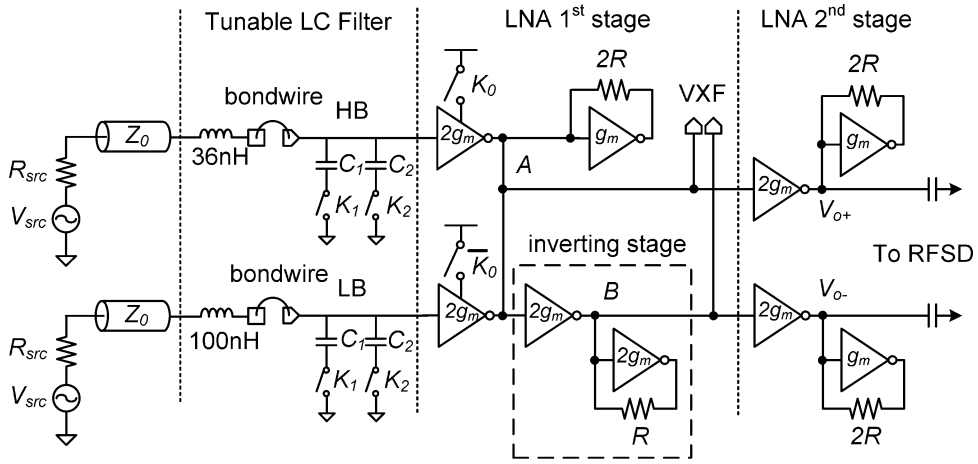


Fig. 5. Implemented *LC* filter and LNA.

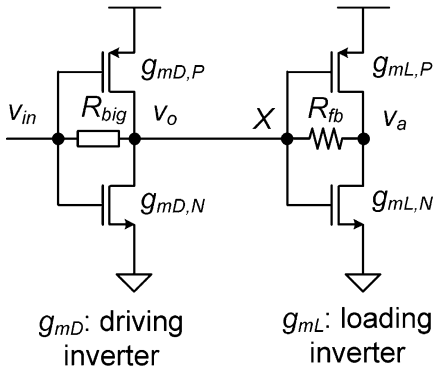


Fig. 6. Schematic of a unit amplifier used in the LNA.

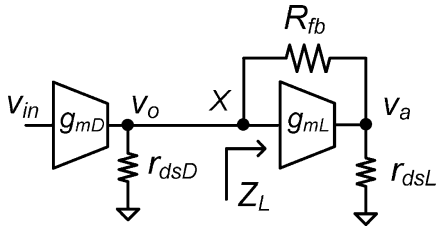


Fig. 7. Model for the unit amplifier.

A. LNA Topology

As shown in Fig. 5, the balun-LNA is constructed using inverters as transconductors. Compared to common-source amplifiers with a single nMOS or pMOS as the transconductor, inverters can provide a large $\mathrm{g_m/I_d}$ ratio as the bias current of the pMOS is reused by the NMOS, while also tolerating large voltage swings which is advantageous for handling large interference.

In fact, all inverters in Fig. 5 are self-biased via feedback resistors, so that no extra bias circuitry is needed. Fig. 6 shows the schematic of a unit amplifier used in the LNA where $\mathrm{g_m} = \mathrm{g_{mN}} + \mathrm{g_{mP}}$. It includes both the feedback resistor (R_{big}) for the driving inverter and the feedback resistor (R_{fb}) for the loading inverter. The absolute value of R_{big} is not critical but is large enough (1 M Ω) only for DC biasing purpose without affecting the transconductance function. Therefore, in Fig. 5, R_{big} of all driving inverters are not shown for figure clarity.

To understand the basic functionality of the LNA in Fig. 5, let's first consider all feedback resistors of the loading inverters as shorts, realizing an impedance of $1/\mathrm{g_m}$ or $1/2\mathrm{g_m}$ where $\mathrm{g_m}$ is the unit transconductance in use. Driven by a transconductance of $2\mathrm{g_m}$, an inverting gain is realized. The gain is -2 in all cases except for the "inverting stage" whose gain is -1. Thus, the first stage realizes a balun function with a 6 dB gain from the input to each of the differential outputs (the single-to-differential gain is 4), and the second stage is a pseudo-differential amplifier with another 6 dB gain.

As can be seen from Fig. 5, the loading inverters have their inputs and outputs connected via a feedback resistor, either R or 2R, for the purpose of nonlinearity compensation (Section IV-B). The feedback resistors and the output impedance of the inverters can affect the amplifier behavior. To analyze the gain and noise performance, we model the unit amplifier (Fig. 6) as Fig. 7, including the output resistance of the driving inverter (r_{dsD}) and the loading inverter (r_{dsL}) and the feedback resistor R_{fb}. The equivalent input impedance of the loading inverter can be written as

$$Z_L = \frac{R_{\mathrm{fb}} + r_{\mathrm{dsL}}}{1 + g_{\mathrm{mL}} \cdot r_{\mathrm{dsL}}} \approx \frac{1}{g_{\mathrm{mL}}} \left(\text{if } \mathrm{g_{mL}} r_{\mathrm{dsL}} \gg 1 \text{ and } r_{\mathrm{dsL}} \gg R_{\mathrm{fb}}\right). \quad (11)$$

In our design, $\mathrm{g_{mL}} = 10$ mS, $r_{\mathrm{dsL}} = 1.5\ \mathrm{k}\Omega$, and $R_{\mathrm{fb}} = 2/\mathrm{g_{mL}} = 200\ \Omega$, and therefore the approximation in (11) holds. Then the voltage gain can be written as

$$\frac{v_o}{v_{\mathrm{in}}} = g_{\mathrm{mD}} \cdot \frac{r_{\mathrm{dsD}} \cdot Z_L}{r_{\mathrm{dsD}} + Z_L} \approx g_{\mathrm{mD}} \cdot \frac{r_{\mathrm{dsD}}}{1 + r_{\mathrm{dsD}} \cdot g_{\mathrm{mL}}} \approx \frac{g_{\mathrm{mD}}}{g_{\mathrm{mL}}} (\text{if } \mathrm{g_{mL}} r_{\mathrm{dsD}} \gg 1). \quad (12)$$

Traditional common-source amplifiers often rely on the product of transistor $\mathrm{g_m}$ and load resistance to define the gain, which can vary a lot due to process spread. The amplifier topology presented here defines its gain via the ratio between

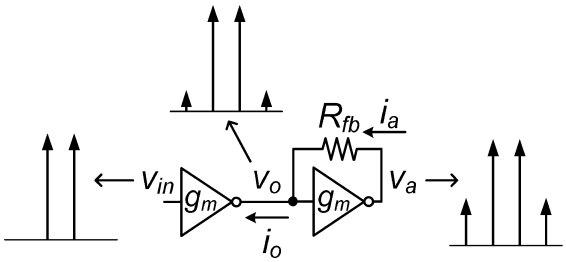


Fig. 8. IM3 compensation mechanism in a unit amplifier with gain $= -1$.

transistors' g_m, which is less sensitive to process spread especially when gain ratios via unit transconductors are used.

The noise performance of such an amplifier is analyzed in [9]. It can be shown that R_{fb} does not contribute to the amplifier's NF.

In Fig. 5, due to the additional stage used for inverting (marked in box) in the V_{o-} path, an extra delay exists therefore the balun performance can degrade at a higher frequency. Any capacitive load at node A (Fig. 5) affects both differential paths, which does not produce imbalance. Loading at node B only affects the V_{o-} path and thus should be minimized. Nevertheless the extra delay on the V_{o-} path can be compensated by adding a capacitor with an appropriate value at the V_{o+} node to better balance the two paths. However, it was not included in this design.

B. Mechanism of Nonlinearity Compensation

The passive pre-gain induced by the *LC* filter improves receiver NF, but it can also degrade linearity. The aim of the feedback resistors in the loading inverters (Figs. 5 to 7) is to mitigate this effect by compensating the third-order distortion.

To understand the compensation principle, consider first the simple case with two equally sized inverters for a voltage gain of -1 (Fig. 8), and only include the linear term and the third-order term in the *V–I* conversion.

If one models the transconductor as a nonlinear *V–I* converter with no v_{ds} dependence, then only g_{m1} and g_{m3} terms need to be considered:

$$\begin{cases} i_o = g_{m1}v_{in} + g_{m3}v_{in}^3 = f(v_{in}) \\ -i_a = g_{m1}v_o + g_{m3}v_o^3 = f(v_o) \end{cases}. \tag{13}$$

Assuming negligible gate current, i_o and i_a are equal due to Kirchhoff's Current Law (KCL), and the solution for (13) is $v_o = (-1)\cdot v_{in}$ which is a perfectly linear *V–V* transfer function. This is because we assume the $i(v)$ functions of the driving and loading inverters are equal, i.e., $v_o(i_a)$ is an *inverse function* of $i_o(v_{in})$. According to (13), $i_o = f(v_{in})$ and $i_a = -f(v_o)$, then we have

$$\begin{aligned} v_o &= -f^{-1}(i_a) = -f^{-1}(i_o) = -f^{-1}[f(v_{in})] \\ &= -v_{in}. \end{aligned} \tag{14}$$

Although the V–I conversion does contain third-order distortion, the V–V conversion can be linear, because the nonlinearity in the *V–I* conversion and the *I–V* conversion cancel each other (inverse functions). This operation with distortion compensation is sometimes referred as voltage mirror [17], [18], a counterpart to current mirror which also relies on inverse functions but with current input and output. If without v_{ds} dependence as (13), the *V–V* conversion can be linear whatever the value of the feedback resistor R_{fb} (can be a short).

However, in modern CMOS technology the output current does depend on v_{ds}, since the output impedance and the $v_{gs}\cdot v_{ds}$ cross-term cannot be neglected anymore [19]–[21]. If we model these effects in Fig. 8 via (15) (shown at the bottom of the page) it still appears possible to achieve third-order distortion compensation.

Traditional amplifier distortion compensation techniques such as derivative superposition [22], [23] mostly focus on the v_{gs}-related term g_{m3}, while this technique, referred as *enhanced voltage mirror*, can also take care of v_{ds}-related terms, e.g., g_{ds3}, x_{12}, and x_{21}, as explained below.

There are two equations in (15) but there are four unknown variables: i_o, i_a, v_o, and v_a, while v_{in} is the given input voltage. Since $i_o = i_a$ based on KCL, the number of unknown variables is reduced to three: i_o, v_o, and v_a. Therefore, the value of v_a will affect the value of v_o now, i.e., the choice of R_{fb} does matter now as it directly affects v_a and therefore affects v_o.

For a linear amplifier, we want $v_o = (-1)\cdot v_{in}$, without any third-order terms. Putting this condition into (15) and equating the two equations shows that $v_a \approx -v_o$ renders a solution. This can be realized by choosing $R_{fb} \approx 2/g_m$, so that $g_m \cdot R_{fb} \approx 2$. Again, although the output current i_o contains third-order distortion, the output voltage v_o can be quite linear.

The above analysis is only valid to the first order. Since i_a is nonlinear with v_o and v_o is linear with v_{in}, $v_a = v_o + i_a \cdot R_{fb}$ cannot be linear with v_{in}. Therefore, v_a is only equal to $-v_o$ to the first order. Then to satisfy $i_o = i_a$ in (15), v_o must also be polluted by some distortion, but to a much lower degree than v_a, as illustrated by the two-tone-test spectra in Fig. 8. This is why in Fig. 5 all the nodes corresponding to v_a are not used. Please note that, for $v_a \approx -v_o$, the feedback resistor for g_m should be 2R and for $2g_m$ it should be $R\,(g_m \cdot R = 1)$, as shown in Fig. 5.

This technique also works for non-equal inverters but the linearity improvement will be less. Here we also use it for the stages with a gain of -2. The simulation results presented in Fig. 9 shows that a peak IIP3 exists at $R \approx 1/g_m$ for both gain of -1 and -2 cases. A 25% change of $g_m \cdot R$ from 1 can still give about 5 dB better IIP3 compared to $g_m \cdot R = 0$ (a short as feedback).

This principle is useful for the odd-order distortion but not very effective for the even-order distortion. Nevertheless, by using an inverter, the even-order distortion of the nMOS and pMOS can compensate each other nominally [24], although

$$\begin{cases} i_o = g_{m1}v_{in} + g_{ds1}v_o + g_{m3}v_{in}^3 + x_{21}v_{in}^2v_o + x_{12}v_{in}v_o^2 + g_{ds3}v_o^3 \\ -i_a = g_{m1}v_o + g_{ds1}v_a + g_{m3}v_o^3 + x_{21}v_o^2v_a + x_{12}v_ov_a^2 + g_{ds3}v_a^3 \end{cases} \tag{15}$$

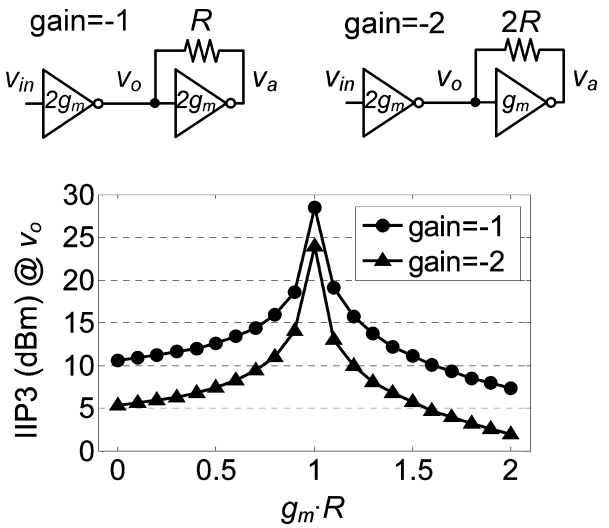


Fig. 9. Simulated IIP3 versus $g_m \cdot R$ of two unit amplifiers (gain $= -1$, gain $= -2$) with two tones around 500 MHz.

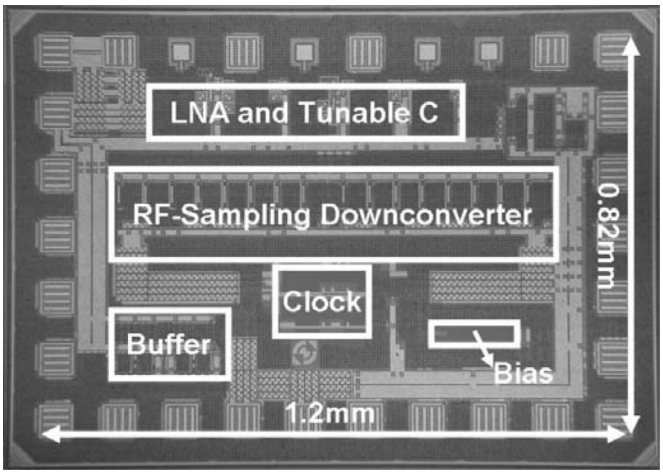


Fig. 10. Micrograph of the chip implemented in 65 nm CMOS.

process spread may lead to residual distortion. A differential configuration can also help with even-order distortion after the balun. Moreover, the AC coupling capacitor used between the LNA and the RFSD can reduce the low-frequency IM2 components generated by the LNA and the DT mixer can also upconvert these input IM2 products.

V. Experimental Results

A proof-of-concept receiver was implemented in 65 nm CMOS and the chip micrograph is shown in Fig. 10, taking an active area $= 0.5$ mm^2. The chip is packaged in a 32-pin Heat-sink Very-thin Quad Flat-pack No-leads (HVQFN) package and measured on PCB and the input port has $R_{\rm src} = 50\Omega$ for all tests. Two inductors of value 100 nH and 36 nH with tolerance of 5% are mounted on board, close to the chip package (Fig. 11). With a 1.2 V supply, the current consumption is 5 mA for the LNA, 10 mA for the clock at 800 MHz LO, and 2.4 mA for the output buffer, while the RFSD consumes no power since it only contains switches and capacitors.

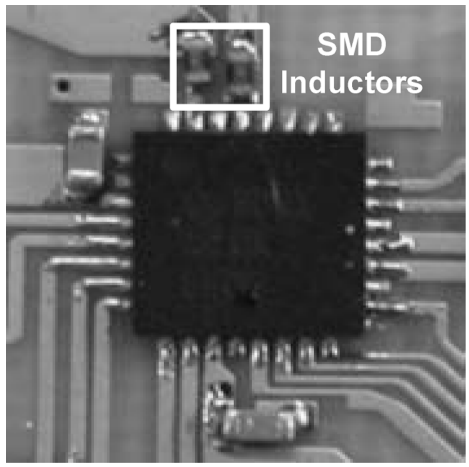


Fig. 11. SMD inductors (36 nH and 100 nH) on PCB.

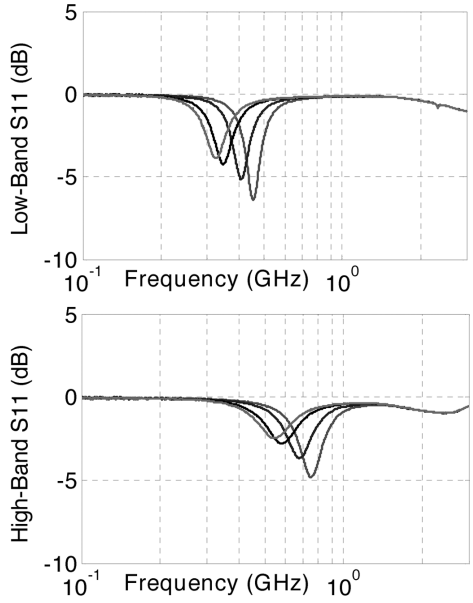


Fig. 12. Measured S11 at low band and high band.

A. S_{11}, Filter Response, Gain, NF, and HR

Fig. 12 shows the measured $\rm S_{11}$ at low band and high band, which basically matches with simulation. The plots show that around resonance frequencies the $\rm S_{11}$ presents dip values which means the series *LC* does not show a perfect short (otherwise $\rm S_{11}$ should be 0 dB). This is due to a resistive part which comes from the inductor parasitics and the LNA, e.g., the LNA output/load resistance in series with $C_{\rm gd}$ and the LNA equivalent gate resistance in series with $C_{\rm gs}$. By simulation, we have found out the resistive part is in the order of 5 to 20Ω.

To verify the tunability of the digitally controlled *LC* filter, we measured the voltage transfer function of the *LC* filter together with the first stage of the LNA via the VXF nodes (Figs. 1 and 5). The input of the *LC* filter is connected to a Vector Network Analyzer via PCB traces and co-axial cables. At the output of the LNA first stage, an active probe (up to 3 GHz) is used to connect

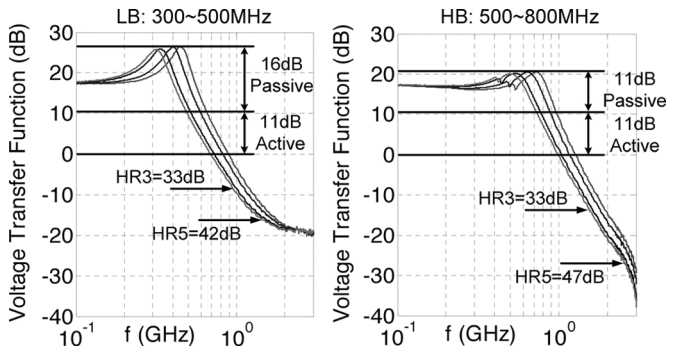


Fig. 13. Measured voltage transfer function: *LC* filter plus LNA first stage (Passive: *LC* pre-gain; Active: LNA first-stage gain).

the VXF nodes (see Fig. 1) to the Vector Network Analyzer.[3] The active probe performs the differential to single-ended conversion with 1× voltage gain as well as the impedance transformation to 50Ω desired for measurements.

Fig. 13 shows the measured voltage transfer function for LB and HB, respectively, which can continuously cover 300–500 MHz and 500–800 MHz with less than 3 dB gain variation in each band. Please note that the gain indicated here is a voltage gain referred to $V_{\rm match}$ in (5). Due to different inductor values (100 nH and 36 nH) used, the Q and therefore the peak gain and bandwidth are different for LB and HB. Considering the 11 dB gain from LNA first stage (verified by measurement), the "passive" *LC* pre-gain is about 16 dB for LB and 11 dB for HB.

Comparing Fig. 13 and Table I, we can see that the measured resonance frequencies basically fit the calculated ones, via a 0.25 pF excess capacitance from PCB ($C_{\rm PCB}$ in Fig. 4), e.g., due to the leadframe and the soldering pad. This excess capacitance may also count the process spread of C_1, C_2, and $C_{\rm LNA}$ in Fig. 4. However, the measured gains (passive) are about 5 dB lower than the calculated gains listed in Table I and about 3 dB lower than the simulated gains. A plausible reason is the deviation from 50Ω of the characteristic impedance of the connection cables and the PCB traces. Therefore, the 50Ω source impedance is transformed to a higher value. Also the resistive part that contributes to the dip values in S_{11} (Fig. 12) can degrade the voltage gain as well.

Both bands show an effective suppression of LO harmonics. The measured LB HR ratios from *LC* filter fit what calculated in Table I, but the measured HB HR ratios are at least 7 dB higher than the calculated values. We attribute this difference to the gain roll off at relatively high frequencies due to circuit parasitics of the LNA first stage and the sharp notch in the HB transfer function due to the inductor self-resonance. The measured third and fifth HR of the complete receiver (4 chips) is shown in Fig. 14, where the HR ratios for the whole band are above 60 dB, with roughly 30 dB contribution from the *LC* filter and the other 30 dB from the RFSD.

[3]The voltage transfer function is obtained via measuring the S21 parameter after using an active probe as the interface between the VXF nodes and the Vector Network Analyzer.

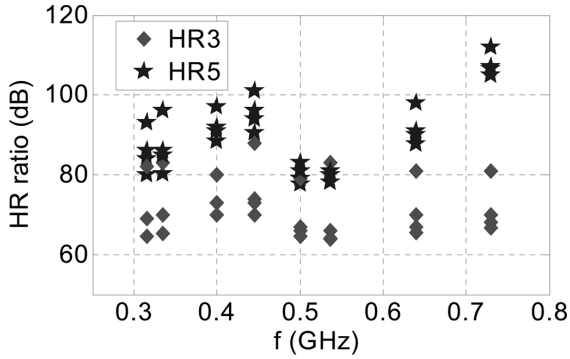


Fig. 14. Measured third and fifth order HR ratios over the RF band (4 chips).

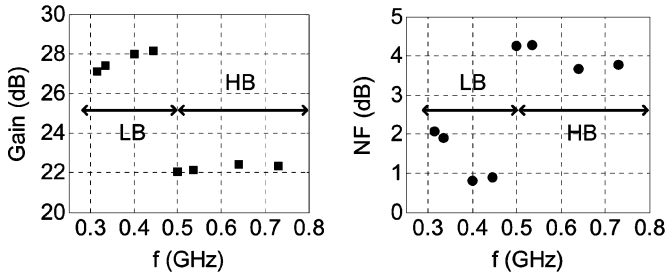


Fig. 15. Measured voltage gain and NF of the complete receiver over the RF band.

Theoretically, a balanced LO with 50% duty cycle can reject all even-order harmonics. However, experiments show the second -order HR can become the bottleneck, since the *LC* filter suppresses the third and higher order harmonics more. This requires balanced LO being more accurate.

Fig. 15 plots the measured voltage gain and NF of the complete receiver, at the peak frequencies of both bands. The gain difference from LB to HB matches the measured voltage transfer function in Fig. 13. The NF is measured via the Y-factor method to read the noise voltage at the output. Fig. 15 shows a clear link between gain and NF, i.e., the high "passive" gain at LB also gives a better NF. The measured minimum NF is 0.8 dB for the complete receiver, which shows a very low NF can be achieved with low power consumption (6 mW for the LNA and downconverter), even for the voltage sampling receiver that suffers from severe noise folding. Such a low NF is achieved via a combination of sufficient "passive" pre-gain to boost the desired signal, second-order *LC* filter to prevent the source noise folding, and HR downconverter to prevent the source and the LNA noise folding.

From Fig. 15, we observe that the variation of the gain and NF is relatively large between LB and HB, which is often undesired. The main cause is the large variation of the *LC* pre-gain (Fig. 13) since the *LC* filter switches band by switching the inductor values (Figs. 1 and 5) so the output voltage of the *LC* filter varies according to (5). *In another implementation,* the variation can be reduced if band switching is done by changing *L* and *C* values at the same time so the *L/C* ratio can be more or less constant. As a result, the variation of the *LC* pre-gain as well as the variation of the total receiver gain and the NF can be made small.

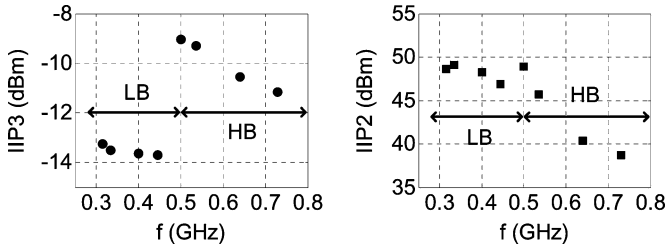


Fig. 16. Measured IIP3 and IIP2 of the complete receiver over the RF band.

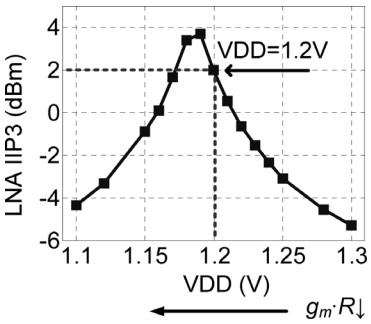


Fig. 17. Measured LNA IIP3 at different VDD levels with two tones around 445 MHz.

B. Linearity

The measured in-band IIP3 and IIP2 via two-tone test are shown in Fig. 16.

Since the LNA is AC coupled to the RFSD (Fig. 1) and the DT mixer upconverts input IM2 products, the IIP2 is dominated by RFSD and degrades with higher frequency (worst case: +38 dBm), rather independent of the gain. Most likely it is due to the degraded balun performance at the high band, since IIP2 directly relates to the matching of differential signal.

From the IIP3 plot, we see the direct effect of the "passive" pre-gain, sharing almost the same trend as NF. The worst-case IIP3 of −14 dBm is moderate for a complete receiver, especially considering that this IIP3 corresponds to a very low NF of 0.8 dB.

Considering the *LC* pre-gain, the LNA plus RFSD combination should present an IIP3 around +2 dBm. Simulation shows the LNA dominates IIP3, which means the two-stage LNA has an IIP3 around +2 dBm. To verify the effect of $\mathrm{g_m} \cdot R$ to the IIP3, we measured and derived the IIP3 of the two-stage LNA (Fig. 17) at different $\mathrm{V_{DD}}$ levels, which affects the $\mathrm{g_m}$ value. Clearly we can see the trend of IM3 compensation which verifies the theory.

Considering $\mathrm{V_{DD}} = 1.2$ V, however, referred to the input of the LNA second stage (VXF nodes in Fig. 5), the IIP3 should be about +7 dBm, since the LNA first stage has a single-ended gain of 5 dB. This IIP3 is far from optimum as simulated in Fig. 9, for the gain = −2 curve, corresponding to a 50% variation of $\mathrm{g_m} \cdot R$ from 1. One reason is the process spread of both $\mathrm{g_m}$ and R which makes the $\mathrm{g_m} \cdot R$ value different from the designed 1. On the other hand, the measured DC linearity via a three-point method [25] is at least 4 dB better than the two-tone test result. This gap of 4 dB could mainly be due to the supply bondwire inductance which is not considered in the simulation of Fig. 9. Measurement via wafer probing (instead of packaged chips on PCB) can exclude the bondwire effect and indeed shows 4 dB better IIP3 [9, Sec. 3.4.3]. The bondwire inductance introduces feedback of the distortion currents and therefore makes the compensation effect more complicated [22].

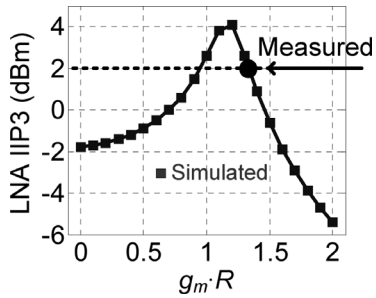


Fig. 18. LNA IIP3: measurement versus simulation.

Simulation has been carried out to include non-ideal effects from both process spread (slow-NMOS and slow-PMOS indicated by measured DC operating point) and supply bondwire inductance ($\mathrm{V_{DD}}$: 2 nH, GND: 0.5 nH, as estimated from the chip size and the specific package used). Fig. 18 compares the measured IIP3 and the simulated IIP3 (by varying the value of R) around 500 MHz RF. The simulation agrees with the measured trend of Fig. 17 and it also indicates that the IIP3 improvement is about 4 dB via the enhanced voltage mirror by applying R_{fb} (instead of a short) in the loading inverter (Fig. 6). Both Fig. 17 and Fig. 18 indicate that the distortion compensation is still effective, although additional techniques are desired to improve its robustness against process spread and bondwire inductance. For instance, techniques to change $\mathrm{g_m}$ to track an *R* or *C* value are well known for filters and a well-designed on-chip decoupling capacitance can reduce the bondwire effect.

Please note that the IIP3 and IIP2 shown in Fig. 16 are in-band IIP3 and IIP2. If needed, it is possible to apply an extra pre-filter between the antenna and the presented *LC* filter to further attenuate out-of-band interference. By using the presented *LC* filter and the HR downconverter, we can relax the requirement on the extra pre-filter which may allow more flexibility. The pre-gain of the *LC* filter can also compensate the losses possibly induced by the extra pre-filter.

VI. Conclusion

A 300–800 MHz multi-band RF-sampling receiver is presented, with 0.8 dB minimum NF and more than 60 dB HR. It is based on a discrete-time mixing harmonic-rejection downconverter in 65 nm CMOS, preceded by a voltage sensing LNA which exploits a simple second-order *LC* filter with one external inductor per sub-band. This *LC* filter does not provide impedance matching but does provide voltage pre-gain and also acts as a harmonic filter tunable via on-chip switchable capacitor banks. The filtering significantly improves the sampling downconverter's HR ratio from 25 dB to more than 60 dB for third and fifth harmonics, resulting in less interference aliasing. The voltage-sensing balun-LNA is built via a simple amplifier topology consisting of inverters and resistors. It reduces the third-order nonlinearity due to both v_{gs} and v_{ds} related terms, via an enhanced voltage mirror technique. The compensation effect is demonstrated via measurements, although an improved robustness against process spread and supply bondwire inductance is desired.

A low NF (0.8 dB) at a low power consumption (6 mW for the LNA and downconverter) for a voltage sampling receiver can be achieved by a sufficient "passive" pre-gain from the *LC* filter, together with the reduced noise aliasing thanks to both the *LC* filter and the harmonic-rejection downconverter.

ACKNOWLEDGMENT

The authors would like to thank Freeband Communications for research funding, and NXP Semiconductors for chip fabrication, especially Domine Leenaerts, and Gerard Wienk and Henk de Vries from University of Twente for their valuable assistance.

REFERENCES

[1] D. Jakonis *et al.*, "A 2.4-GHz RF sampling receiver front-end in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1265–1277, Jun. 2005.

[2] H. Pekau and J. W. Haslett, "A 2.4 GHz CMOS sub-sampling mixer with integrated filtering," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2159–2166, Nov. 2005.

[3] R. B. Staszewski *et al.*, "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, Dec. 2004.

[4] K. Muhammad *et al.*, "The first fully integrated quad-band GSM/GPRS receiver in a 90-nm digital CMOS process," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1772–1783, Aug. 2006.

[5] F. Montaudon *et al.*, "A scalable 2.4 to 2.7 GHz Wi-Fi/WiMAX discrete-time receiver in 65 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 362–619.

[6] R. B. Staszewski *et al.*, "A 24 mm^2 quad-band single-chip GSM radio with transmitter calibration in 90 nm digital CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 208–607.

[7] Z. Ru, E. A. M. Klumperink, and B. Nauta, "On the suitability of discrete-time receivers for software-defined radio," in *Proc. IEEE ISCAS*, May 2007, pp. 2522–2525.

[8] Z. Ru, E. A. M. Klumperink, and B. Nauta, "A discrete-time mixing receiver architecture with wideband harmonic rejection," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 322–323.

[9] Z. Ru, "Frequency translation techniques for interference-robust software-defined radio receivers,," Ph.D. dissertation, Univ. of Twente, Enschede, The Netherlands, 2009.

[10] F. Gatta *et al.*, "An embedded 65 nm CMOS low-IF 48 MHz to 1 GHz dual tuner for DOCSIS 3.0," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 122–123.

[11] "Notice for Proposed Rulemaking (NPRM 03 322): Facilitating Opportunities for Flexible, Efficient, and Reliable Spectrum Use Employing Spectrum Agile Radio Technologies," Federal Communications Commission (FCC), ET Docket No. 03 108, Dec. 2003.

[12] Z. Ru, E. A. M. Klumperink, C. E. Saavedra, and B. Nauta, "A tunable 300–800 MHz RF-sampling receiver achieving 60 dB harmonic rejection and 0.8 dB minimum NF in 65 nm CMOS," in *IEEE RFIC Symp. Dig.*, Jun. 2009, pp. 21–24.

[13] W. Sansen, *Analog Design Essentials*. New York: Springer, 2006.

[14] M. Steyaert *et al.*, "A single-chip CMOS transceiver for DCS-1800 wireless communications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 1998.

[15] M. Camus *et al.*, "A 5.4 mW 0.07 mm^2 2.4 GHz front-end receiver in 90 nm CMOS for IEEE 802.15.4 WPAN Standard," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1372–1383, Jun. 2008.

[16] M. Soer, E. A. M. Klumperink, Z. Ru, F. E. van Vliet, and B. Nauta, "A 0.2 to 2.0 GHz 65 nm CMOS receiver without LNA achieving $>$11 dBm IIP3 and $<$6.5 dB NF," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 222–223.

[17] J. C. Platt, M. F. Wall, G. E. Gribble, and C. A. Mead, "Circuits for linear conversion between voltages and currents," U.S. Patent 5,126,685, Jun. 30, 1992.

[18] H. Song, "Buffer/voltage-mirror arrangements for sensitive node voltage connections," U.S. Patent 6,847,236, Jan. 25, 2005.

[19] S. Kang, B. Choi, and B. Kim, "Linearity analysis of CMOS for RF application," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 3, pp. 972–977, Mar. 2003.

[20] B. Toole, C. Plett, and M. Cloutier, "RF circuit implications of moderate inversion enhanced linear region in MOSFETs," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 51, no. 2, pp. 319–328, Feb. 2004.

[21] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, Jun. 2008.

[22] V. Aparin and L. E. Larson, "Modified derivative superposition method for linearizing FET low-noise amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 2, pp. 571–581, Feb. 2005.

[23] W.-H. Chen, G. Liu, B. Zdravko, and A. M. Niknejad, "A highly linear broadband CMOS LNA employing noise and distortion cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1164–1176, May 2008.

[24] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies," *IEEE J. Solid-State Circuits*, vol. 27, no. 2, pp. 142–153, Feb. 1992.

[25] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2004.

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