# Fabrication and Characterization of the Charge-Plasma Diode

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***Abstract*—We present a new lateral Schottky-based rectifier called the charge-plasma diode realized on ultrathin silicon-on-insulator. The device utilizes the workfunction difference between two metal contacts, palladium and erbium, and the silicon body. We demonstrate that the proposed device provides a low and constant reverse leakage-current density of about 1 fA/$\mu$m with ON/OFF current ratios of around $10^7$ at 1-V forward bias and room temperature. In the forward mode, a current swing of 88 mV/dec is obtained, which is reduced to 68 mV/dec by back-gate biasing.**

***Index Terms*—Buried oxide (BOX), charge-plasma (CP) diode, diode, p-i-n diode, Schottky barrier, silicon-on-insulator (SOI).**

## I. Introduction

SILICON-ON-INSULATOR (SOI)-based devices with ultrathin body are considered for future very large scale integrated circuit (IC) applications [1]–[3]. A silicon p-i-n diode acting as a rectifier is one such component. It plays an important role in diverse research domains, like power ICs and light-emitting devices [4], [5]. Desirable diode properties are a very low forward voltage drop and small reverse leakage current to reduce the power dissipated by the rectifier. For conventional p-n junctions with nanoscale dimensions, the key issue is doping control: doping fluctuation [6], [7], doping activation [8], and obtaining steep doping profiles demanding a low temperature budget.

Schottky-based devices with metal or metal silicided source–drain contacts are reported to circumvent these fabrication-related issues and produce performance specifications comparable with conventional diodes [9], [10]. Fig. 1(a) shows a schematic cross section of our realized device called the charge-plasma (CP) diode. Here, two separate metallic gates are placed on top of a thin silicon body. The gates are isolated from the top of the body by a dielectric layer, and each forms a contact at one side of the silicon body. In the devices presented in this letter, the metallic contacts are extended to

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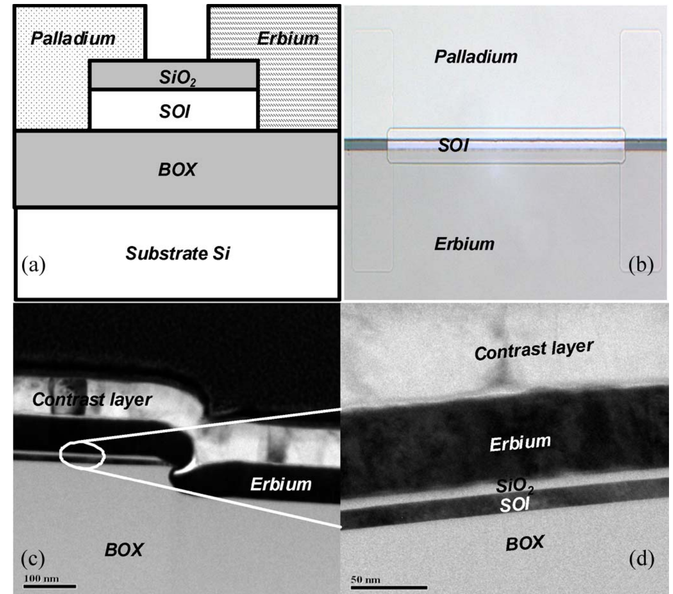


Fig. 1. (a) Schematic cross section of a CP diode. Pd used as an anode and Er used as a cathode contacted the top and sidewall of the SOI. In the region above the $Si/SiO_2$ stack, the metals act as a gate. (b) Top-view image of the fabricated device. (c) TEM cross section of the device with different layer stack. (d) Enlarged image showing the thin $Si/SiO_2$ layer stack.

the top of the thin silicon body in order to reduce the contact resistance. As stated earlier [10], [11], there are two essential features in this concept. First, the workfunctions of the cathode and the anode metals should fulfill $\varphi_{m,C} < \chi\text{Si} + (E_G/2)$ and $\varphi_{m,A} > \chi\text{Si} + (E_G/2)$ in terms of the electron affinity of bulk silicon ($\chi\text{Si} = 4.17$ eV), and the bandgap of bulk silicon ($E_G$). For optimal rectifying behavior, the difference between both workfunctions should be at least $\sim$0.5 eV. Second, the thickness of the silicon body should be around or less than the Debye length [12]. For this situation, the charge underneath both gates in the silicon is primarily determined by charge carriers, and the depletion charge can be neglected irrespective of the doping concentration in the silicon layer.

This letter deals with the fabrication and electrical characterization of the CP diodes. We will show that the CP diodes can perform comparably with conventional p-n diodes or junctions with doped regions by making a wise choice of metal combination and device dimensions.

## II. Experimental Procedure

The devices were fabricated using 4-in SOI wafers with a 1-$\mu$m buried oxide (BOX) and almost intrinsic ($6 \cdot 10^{14}$ cm$^{-3}$)

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n-Si layer of 340-nm thick on top. The top Si layer was then thinned down to 25 nm by thermal oxidation at 950 °C in a quartz furnace under oxygen ambient. The thinned-down Si layer is patterned in a 30% tetramethylammonium hydroxide solution using a silicon-oxide mask. After cleaning and removal of the oxide mask, a 10-nm-thick gate oxide was grown by thermal oxidation at 950 °C on clean silicon surface resulting in a final Si thickness of around 20 nm. The metal contacts are then made to form the anode and cathode. The choice of contact metals is based on their availability in our cleanroom facility, ease of process integration, and extracted Schottky barrier height to lowly doped bulk Si ($10^{15}$ cm$^{-3}$). For the devices described here, we chose palladium (Pd), a metal with high workfunction (4.9 eV), as the anode and erbium (Er), with low workfunction (4.4 eV), as the cathode.

Both metals were sputtered immediately after an HF dip, to minimize residual oxide. No thermal treatment was applied after sputtering. Care should be taken that measurements do not exceed 400 K due to the onset of Pd silicidation at temperatures of as low as 330 K [13]. Increasing the measurement temperature or time results in $Pd_2Si$ formation observable as a slight increase in the reverse current due to the lower workfunction of the $Pd_2Si$ (4.8 eV). Er silicidation is reported to significantly reduce the Schottky barrier height [14]. We have not observed instabilities in the Er contacts, but material analysis could not exclude the possibility of Er silicidation. In Fig. 1(b), the top-view image of a device on wafer is shown as seen through a microscope. Fig. 1(c) and (d) shows a cross section of a fabricated device obtained using transmission electron microscopy (TEM). Electrical characterization was carried out on a Suss MicroTec PM300 Manual Probe Station equipped with a Keithley 4200 semiconductor characterization system.

## III. Results and Discussion

The electrical characteristics discussed here are for an intrinsic silicon area of $100 \times 10$ $\mu$m$^2$ and a metal spacing of 3 $\mu$m unless specified otherwise. We began by investigating the symmetric device structures in which the same metal was employed for the anode and the cathode (either Pd or Er). From these structures, we investigated the MOSFET behavior by using the substrate as back gate. The cathode was kept at 0 V, the anode voltage $V_{\rm ac}$ was swept from 0 to 1 V, and the gate voltage $V_{\rm gc}$ was stepped from 0 to $-30$ V. The resulting output characteristics are shown in Fig. 2. High gate voltages had to be applied because of the thick (~1 $\mu$m) BOX layer between the substrate and the SOI layer. The $I_a - V_{\rm ac}$ output characteristics of the Er–Er devices show a linear behavior in the linear region, indicating good ohmic contacts. On the other hand, the Pd–Pd devices show diode behavior in the "linear" region confirming the Schottky behavior of these contacts to lowly doped n-type Si [15].

Next, we examine the CP diode. The cathode (Er side) and the back gate are kept at 0 V. The anode is biased from $V_{\rm ac} = -1$ to 1 V. Fig. 3 shows the temperature-dependent $I_a - V_{\rm ac}$ characteristics of a diode under the aforementioned biasing condition. The diode shows rectification in the whole range from 288 to 398 K. In contrast to a conventional p-n diode,

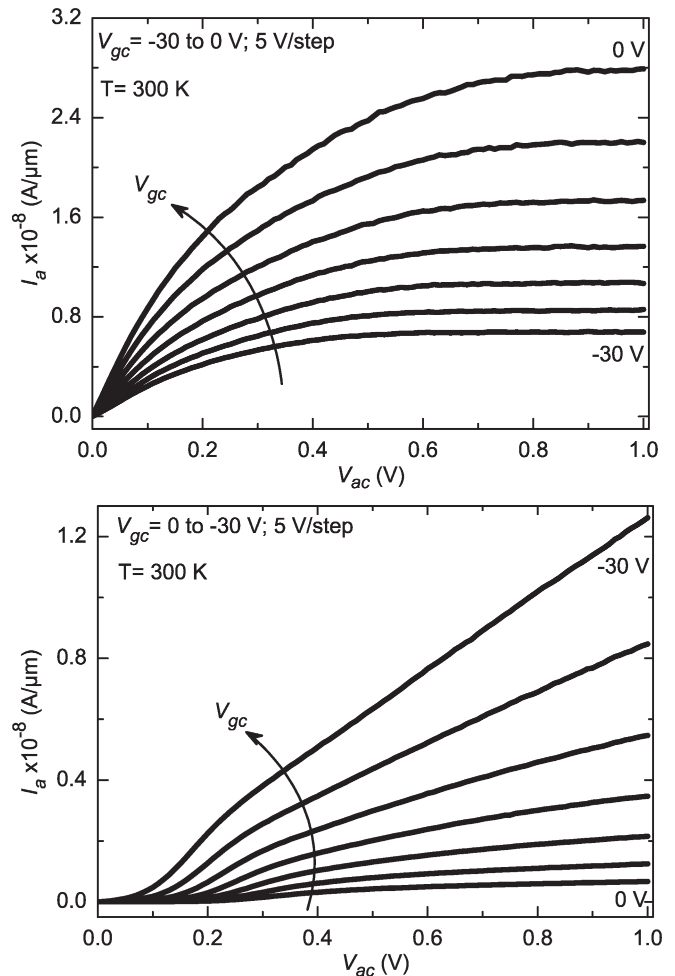


Fig. 2. Anode current $I_a$ as a function of the anode-to-cathode voltage $V_{\rm ac}$ for (top) symmetric Er–Er electrode and (bottom) symmetric Pd–Pd electrode transistor at RT (300 K). The anode is kept at 0 V, the substrate is used as back gate, and its voltage is varied from $-30$ to 0 V for Er and 0 to $-30$ V for the Pd devices, as indicated.

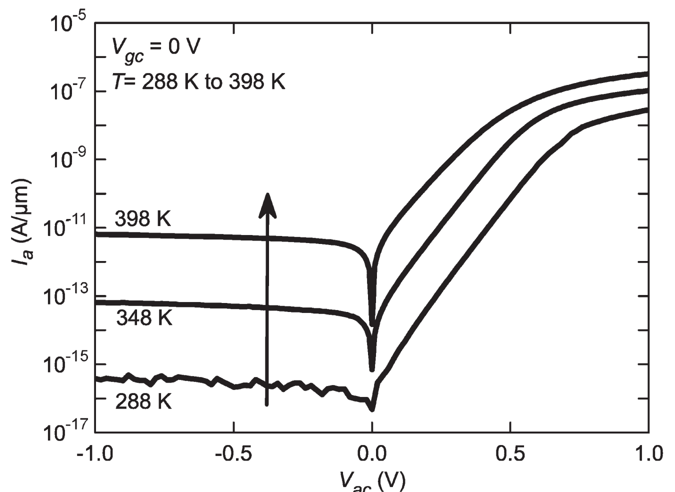


Fig. 3. Measured temperature dependence of the anode current $I_a$ to anode-to-cathode voltage $V_{\rm ac}$ for the CP diode. The anode voltage was swept, while the cathode voltage was kept at 0 V. The diode shows rectification in the whole range from 288 to 398 K.

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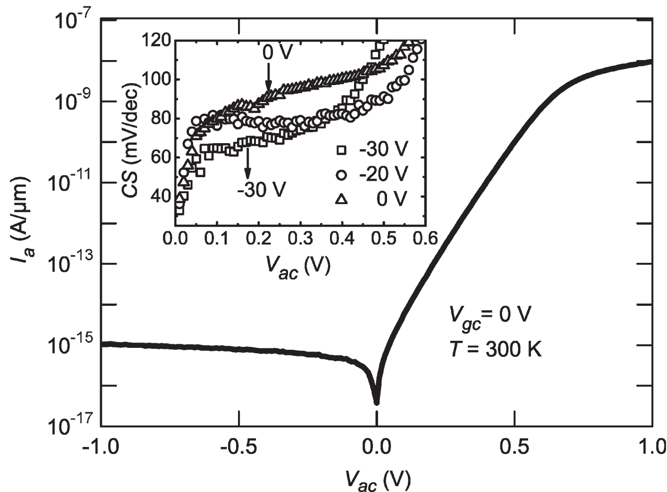


Fig. 4. Current–voltage relation of our CP diode at RT (300 K). The anode current $I_a$ is measured while sweeping the anode voltage $V_{\mathrm{ac}}$ from $-1$ to 1 V. The cathode and substrate are kept at 0 V. The inset shows reduction in CS by increasing the substrate biases from 0 to $-30$ V. Further increase does not show additional improvement in the CS.

the ON current increases (exponentially) with the temperature, resulting in an $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio of $10^5$ at 398 K, only two orders of magnitude of reduction with respect to the $10^7$ at room temperature (RT). This increase in $I_{\mathrm{on}}$ is attributed to the ON current being limited by diffusion since the gates are in weak inversion mode at high forward bias. At RT (Fig. 4), a small and almost constant leakage current of around 1 fA$/\mu$m is obtained which indicates a low density of active generation centers in the "bulk" silicon body. This also gives a confirmation that the region under the Pd metal gate acts as a p/p+ region and under the Er metal gate as the n/n+ region and hence, forming a p-i-n diode. A high ON/OFF current ratio of around $10^7$ and a current swing (CS) of around 88 mV/dec at zero substrate bias is obtained. The CS depends on the quality of the $\mathrm{Si}/\mathrm{SiO_2}$ interface [12]. The presence of interface traps tends to degrade the fast switching of the diode from OFF to ON state and hence, results in poor CS. By applying a suitable substrate bias, it is possible to determine whether the interface traps at the BOX/Si interface play a role in weakening the CS from the ideal value of 60 mV/dec. On varying the substrate bias from 0 to $-30$ V, it can be seen that the CS changes from 88 to 68 mV/dec (Fig. 4 inset). No hysteresis was observed in the device characteristics. Interchanging the anode and cathode was reported to give a shift in the characteristics for CNTs [16]. We do not see this in our devices.

## IV. Conclusion

We have fabricated a new rectifier called the CP diode that makes use of the workfunction difference between the metal contact and the intrinsic silicon body. This novel device requires no doping, avoiding statistical doping fluctuations and doping-control issues, and it can be processed at low temperatures. Our experimental results show that high ON–OFF current ratios, both at RT $(10^7)$ and at elevated temperature $(10^5)$, combined with very low leakage currents (1 fA$/\mu$m at RT) are possible to achieve using this technique. It is expected that compared with conventional diodes, the ON–OFF ratio at elevated temperatures is orders of magnitude better due to the exponential increase in the ON current. Better CSs can be achieved by reducing interface traps between $\mathrm{SiO_2}/\mathrm{Si}$ interfaces. By using the symmetrical metal contacts and the substrate as back gate, MOSFET-like characteristics can be obtained. Thus, a new way of making rectifiers and MOSFETs in a CMOS-compatible manner is introduced.

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