A BREAKDOWN VOLTAGE MODEL FOR IMPLANTED RESURF p -LDMOS DEVICE ON n^+ BURIED LAYER

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(Received 21 April 1993; in revised form 11 October 1993)

Abstract—This paper presents an analytical expression of the breakdown voltage of a high voltage implanted RESURF p -LDMOS device which uses the n^+ buried layer as an effective device substrate. In this model, the doping profile of the buried layer is considered and discussed. The implant dose for the drift region to implement the RESURF principle is also described by this model. Results calculated from this model are verified by experimental values.

1. INTRODUCTION

The integration of the high voltage double-diffused MOS (DMOS) devices with bipolar, CMOS devices using BICMOS technology leads to wide applications like display drive, motor control and telecommunication[1]. One of these DMOS devices is the lateral DMOS (LDMOS) on thin epitaxial layer. However, such devices have lower breakdown voltages due to the high electric fields at the surface, near the drain diffusion. The breakdown performance can be improved by introducing the RESURF principle[2] to reduce the surface fields, causing the breakdown to move into the drift-substrate junction under the drain. To implement the principle the drift region should be a pn junction with the substrate and the charge in the drift region should be accurately controlled by methods like ion implantation.

In [3, 4], a complementary p -LDMOS device is proposed using BICMOS technology as shown in Fig. 1. The starting material is a p -type silicon wafer above which lies a lightly doped thin epitaxial layer of the same type. Such a p - p^+ substrate has the advantages of low latchup susceptibility and ease of isolation. To form a pn junction between the drift region and the substrate, the n^+ buried layer, necessary for the bipolar devices and the latch-up immunity, is at the meantime used as an effective substrate of the LDMOS device. Because of the buried layer up-diffusion, the drift region depth t_d becomes much smaller. The lightly doped drift region of the device is then implanted by borons to adjust its charge according to the RESURF principle. Obviously, the influence of the buried layer has to be considered. In this paper, a closed form of the breakdown voltage calculation for the RESURF device will be presented. Consequently, the dose condition of the p^+ ion implantation for the drift

charge adjustment will be obtained. Results from this model will be compared with the experimental values.

2. MODEL DESCRIPTION

It is known that when the RESURF principle is observed in the p -LDMOS device as shown in Fig. 1, the surface electric field in the drift region is significantly reduced and as a result, the device breakdown is dominated by the drift-substrate junction under the drain. The limiting value of the composite p^+pn^+ junction breakdown voltage can be derived by considering it as a punched-through (PT) diode breakdown[4]. The concerned PT diode structure and the impurity profile used to derive the expression of the breakdown voltage are shown in Fig. 2. The doping concentration in the drain diffusion region is assumed infinite and the doping profile of the n^+ buried layer is exponential: $N_D = N_A e^{x/\alpha}$ (where x is in μm , and α is the impurity gradient parameter of the buried layer). Here, in order to simplify the

Fig. 1. Cross-section of the implanted RESURF p -LDMOS device structure. ($N_A = 5 \times 10^{14} \text{ cm}^{-3}$, $t_{p+} = 0.5 \mu\text{m}$.)

Fig. 2. p^+ -drain/ p -drift/ n^+ -buried layer punched-through diode model and its impurity profile used for breakdown voltage calculation.

problem, we assume that the doping concentration at $x = 0$ for n^+ side is equal to the doping value of the p -drift N_A .

Let us first consider the breakdown case of a parallel p - n^+ plane junction (without the p^+ drain), defined as a free junction. The Poisson's equation to be solved is one-dimensional:

$$\frac{d^2 V}{dx^2} = -\frac{\rho(x)}{\epsilon_s}, \quad (1)$$

where

$$\begin{cases} \rho(x) = -qN_A & -x_p < x < 0 \\ \rho(x) = qN_D = qN_A e^{\alpha x} & 0 < x < x_n \end{cases} \quad (2)$$

where ϵ_s is the permittivity of silicon, q is the electron charge, x_n and x_p are the widths of the n -side and p -side depletion regions, respectively, when the junction is biased at its breakdown conditions.

After solving eqn (1) with boundary conditions $E(-x_p) = 0$ and $E(x_n) = 0$, the electric field and potential distribution [defining $V(0) = 0$] become:

$$\begin{cases} E(x) = -(qN_A/\epsilon_s)(x + x_p) & -x_p < x < 0 \\ E(x) = (qN_A/\alpha\epsilon_s)(e^{\alpha x} - e^{\alpha x_n}) & 0 < x < x_n \end{cases} \quad (3)$$

and

$$\begin{cases} V(x) = (qN_A/2\epsilon_s)(x^2 + 2x_p x) & -x_p < x < 0 \\ V(x) = (qN_A/\alpha\epsilon_s)(xe^{\alpha x} - e^{\alpha x_n}/\alpha + 1/\alpha) & 0 < x < x_n \end{cases} \quad (4)$$

Using Fulop's formula for the effective ionization coefficient, the junction breakdown condition is given by the following ionization integral[5]:

$$\int_{-x_p}^{x_n} A_F E^7(x) dx = 1, \quad (5)$$

where $A_F = 1.8 \times 10^{-35}$ and $E(x)$ is the field distribution in the depletion region of the junction.

By solving eqns (1)–(5), the depletion widths x_n and x_p of the free junction can be obtained.

If we now take the p^+ drain into account, we can see that the reverse biased depletion region at p -side will reach the highly doped drain region and result in the vertical punchthrough condition. In this situation, we assume that the maximum electric field,

in the case of breakdown occurring at the metallurgical junction $x = 0$, equals the so-called critical value E_{crit} . To simplify the problem and consider in an idealized manner, we take E_{crit} approximately equal to the maximum electric field of the former free p - n^+ plane junction, as discussed above, under breakdown conditions. Therefore, E_{crit} can be simply expressed as:

$$E_{crit} = -\frac{qN_A x_p}{\epsilon_s}, \quad (6)$$

where x_p is still the depletion width from a solution of eqns (1)–(5).

For the PT diode, we re-solve eqn (1) with the boundary conditions $E(0) = E_{crit}$ and $E(x_n) = 0$. In this case the expression of the potential for the n -side is the same as that in eqn (4). This leads to the final expression for the diode punchthrough breakdown voltage V_{BR} :

$$\begin{aligned} V_{BR} &= V(x_n) - V(-x_p) \\ &= \frac{qN_A}{\epsilon_s} \left(x_p w_p + w_p^2 + \frac{x_n e^{\alpha x_n}}{\alpha} - \frac{e^{\alpha x_n}}{\alpha^2} + \frac{1}{\alpha^2} \right), \end{aligned} \quad (7)$$

where $w_p = t_d - t_{p+} t_d$ and t_{p+} are the drift and the drain diffusion depths, respectively.

It should be emphasized that eqn (7) gives the maximum breakdown voltage that the device can achieve. It is only possible when the RESURF principle is implemented which requires the net of the charge in the drift region equal to those in the depleted region of the substrate when V_{BR} is applied. Such a condition is not satisfied in our device due to its thin and lightly doped drift region. The charges in the drift region can be modified by a p^+ ion implantation and the implant dose can be obtained by:

$$N_{dose} = N_A(x_p - t_d + t_{p+}). \quad (8)$$

Fig. 3. Breakdown voltages of the composite PT junctions as a function of impurity gradient parameter of the buried layer α for the two different drift depths t_d . N_{dose} is the corresponding p^+ implant dose for the drift charge modification.

Table 1. Breakdown voltages of the implanted RESURF LDMOS devices with different drift depth and impurity gradient parameter of the buried layer

Parameters				
t_d (μm)	3.2	4.2	3.3	4.1
α ($1/\mu\text{m}$)	1.81	1.81	1.01	1.01
V_{BR} (V) exp.	115.7 ± 1.3	146.3 ± 2.0	148.4 ± 0.6	159.3 ± 2.3
V_{BR} (V) cal.	117.5	142.0	142.0	159.8

3. RESULTS AND DISCUSSIONS

In Fig. 3, the breakdown voltages V_{BR} calculated by (7) of this PT composite junction are plotted as a function of the impurity gradient of the buried layer α with the depth of the drift region t_d as a parameter. This figure shows that V_{BR} increases with the increase of t_d and the decrease of α . It implies and will be further verified that the above model is more accurate than that assuming an abruptly buried layer-drift region junction where α becomes infinite.

Figure 3 also gives the values of the implant dose N_{dose} , derived by (8). We find that N_{dose} is almost independent of t_d , but increases with α . We also find that, as α changes from 1 to $2 \mu\text{m}^{-1}$, typical values in our investigation, the variation of N_{dose} is small. We should point out that the calculated N_{dose} represents a minimum rather than a definite dose, however, N_{dose} cannot be too high. Otherwise, the p^+ implanted layer would become part of the drain, resulting in a lateral breakdown between the channel and the drain. To accurately deal with this problem, a two-dimensional analysis is necessary.

It should be mentioned that the assumption of the exponential doping profile of the buried layer in the above discussion is obtained approximately

from the measurement of spreading resistance. We find that this assumption is quite effective at a first order within a range of x ($x < 5 \mu\text{m}$) from the junction.

In this experiment, the p^+ implant dose is chosen about $1.6 \times 10^{12} \text{ cm}^{-2}$. The implant energy is 50 keV and the depth following the drive-in is about $0.3 \mu\text{m}$ thereby forming a very abrupt profile at the surface. To avoid the horizontal breakdown between the channel and the drain, the drift length is chosen much larger than its depth. Table 1 shows the calculated and the experimental breakdown voltages in the implanted RESURF LDMOS devices with different values of t_d and α . The comparison shows a very good agreement.

To demonstrate the effect of the application of the RESURF principle to our devices, we calculate the equipotential lines in the drift region with and without the p^+ ion implantation. The calculation is made numerically using boundary element method[6]. It is obvious that when using the p^+ implant, the surface electric field is reduced due to the spreading of the equipotential lines between the channel and the drain.

4. CONCLUSION

An analytical calculation model of the breakdown voltage of a high voltage implanted RESURF *p*-LDMOS device on the n^+ buried layer substrate is presented. With this model, the implant dose for the drift region can be predicted. Results from this model agree well with the experimental values. The presented model can provide a first-order insight into the factors affecting the device breakdown performance and is very useful for the design of the *p*-LDMOS using BICMOS technology.

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Fig. 4. Map of equipotential lines in the drift region of the *p*-LDMOS devices in off-state when the drain voltages is -150 V (a) without and (b) with the p^+ ion implantation.