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# On Device Architectures, Subthreshold Swing, and Power Consumption of the Piezoelectric Field-Effect Transistor ($\pi$-FET)

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**ABSTRACT** This paper describes the potential of tunable strain in field-effect transistors to boost performance of digital logic. Voltage-controlled strain can be imposed on a semiconductor body by the integration of a piezoelectric material improving transistor performance. In this paper, we derive the relations governing the subthreshold swing in such devices to improve the understanding. Using these relations and considering the mechanical and technological boundary conditions, we discuss possible device architectures that employ this principle. Further, we review the recently published experimental and modeling results of this device, and give analytical estimates of the power consumption.

**INDEX TERMS** Piezoelectric effect, MOSFET, CMOS, subthermal device, steep-subthreshold device.

## I. INTRODUCTION

In recent years, the performance improvement of transistors from generation to generation has slowed down, as a result of lagging gate length scaling. So-called performance boosters have been introduced in Complementary Metal-Oxide-Semiconductor (CMOS) technology to further improve the circuit performance in new process generations [1]. These performance boosters include metal-gate-high-k stacks [2], [3], channel strain [4]–[6], and ultra-thin body configurations (e.g., ultra-thin body silicon-on-insulator substrates [7] and FinFETs [8], [9]). Both higher on-currents and lower off-currents are achieved through these measures.

For the further advancement of CMOS, devices must exhibit a high on/off ratio at low power supply voltage. The key limiting factor in conventional MOS transistors is the subthreshold swing (*SS*), see also Fig. 1, defined as [10]:

$$SS \equiv \frac{dV_{GS}}{d\log(I_D)} = \frac{dV_{GS}}{d\ln(I_D)} \cdot \ln(10) = m \cdot u_T \cdot \ln(10), \quad (1)$$

where $V_{GS}$ is the gate-source voltage, $I_D$ is the drain current, $u_T$ is the thermal voltage, and $m$ is the ideality factor.

In a classical FET the subthreshold swing is limited by diffusion of charge carriers and is ≥60 mV/dec at room temperature whereas for future CMOS a lower, i.e., subthermal, *SS*, is required. Several device concepts aiming at a subthermal *SS* have been proposed and are currently under investigation; see [11]–[19] and the other articles of this Special Issue.

In recent articles we proposed the addition of piezoelectric material to the FinFET as a further performance booster [20], [21]. In this device, dubbed $\pi$-FET, the converse piezoelectric effect is employed to achieve active modulation of the channel strain. Instead of permanent strain, we can now turn on the strain only in the on-state, leading to an advantageous on/off ratio, as visualized in Fig. 1. We earlier reported on experimental realizations of prototype devices following this principle [22].

In this work we further analyze the potential of the $\pi$-FET by technological and performance considerations. This article

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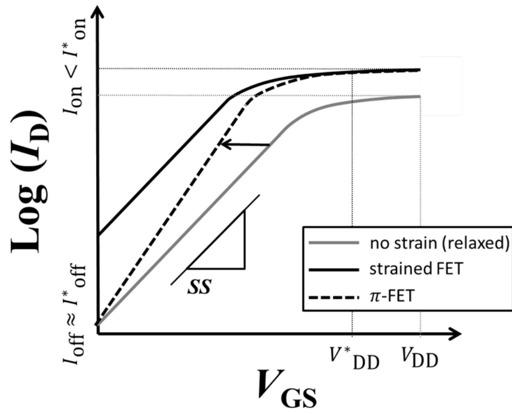


**FIGURE 1. Illustration of the $I_D$-$V_{GS}$ characteristics of a FET on semi-logarithmic scale. The characteristics are shown for a device with no strain (i.e., relaxed condition), constant strain, and strain formed by the converse piezoelectric effect (i.e., the $\pi$-FET). The subthreshold swing (SS) is also indicated.**

describes the envisaged $\pi$-FET configurations, presents analytical relations of the *SS*, and estimates the power consumption based on analytical relations and roadmap projections [1].

This work is outlined as follows. In Section II we detail the principle of operation and derive the equations for the *SS*. In Section III we explain several device configurations. In Section IV we address the power consumption of the $\pi$-FET. Finally, in Section V the conclusions of this work are drawn.

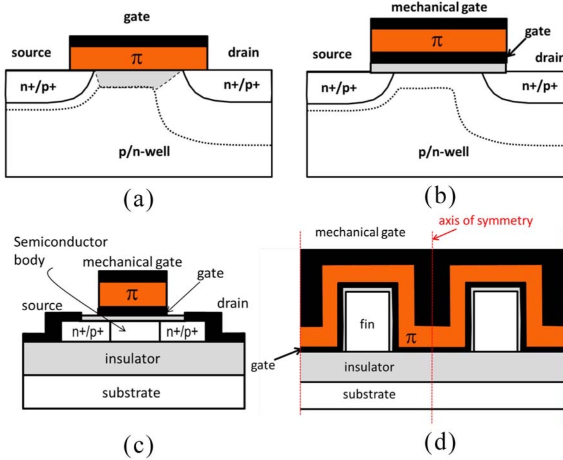


**FIGURE 2. Schematic cross section of several envisaged $\pi$-FET configurations. (a) Bulk $\pi$-FET in which the $\pi$-layer has been directly placed on the silicon (the gray region indicates the depletion region), and devices in which there is only a mechanical contact between the $\pi$-layer and the channel such as (b) bulk $\pi$-FET and ultrathin body (UTB) devices in (c) planar/double-gate $\pi$-FET configuration, and (d) $\pi$-FinFET configuration (perpendicular to the current flow direction). For the $\pi$-FinFET, the vertical dotted line indicates the axis of symmetry. The dimensions are not to scale. Note for maximum strain effect the mechanical gate should be preferably made out of a stiff metal and fixed e.g., in the third dimension.**

## II. BASIC PRINCIPLE

Before treating the possible device configurations we first discuss the basic principle and for the first time derive relations for the *SS* applicable to most types of $\pi$-FETs for improving the basic understanding. For a classical Si transistor, when there is good electrostatic gate control over $I_D$, *SS* equals 60 mV/dec at room temperature as illustrated in Fig. 1 (no strain). In CMOS technology so-called strain, i.e., mechanical deformation, is employed in Si to increase the mobility hence the performance. This type of strain is typically constant depending on the surrounding materials and leads to a relatively high $I_{off}$ and $I_{on}$ provided all other process parameters are kept the same [5], [23], as illustrated in Fig. 1 (strained FET). Recently, we have proposed a new device called the PiezoFET ($\pi$-FET) [20], [21] in which a piezoelectric ($\pi$-) layer is incorporated in the device, see e.g., Fig. 2. The basic idea is that the strain in the semiconductor body can be tuned by the *converse* piezoelectric effect [24]. As a result, during device operation the body is relaxed in the off-state, resulting in a low $I_{off}$, and it is strained in the on-state. As mentioned before the strain has an effect on the mobility, however, also on the band alignment. In particular the change in band alignment reduces the *SS* as predicted by [21], schematically illustrated in Fig. 1. However, [21] presented numerical calculations with a focus on ultrathin body (UTB) configurations. To grasp the basic principle it is important to derive closed form relations for the *SS* of the $\pi$-FET in bulk and UTB configurations.

For determining the *SS* we need to study the electrostatics of a FET starting from:

$$V_{GS} = V_{ins} + V_s, \tag{2}$$

with $V_{ins}$ and $V_s$ being the voltage drop across the gate insulator and semiconductor, respectively.

Neglecting the mobile charge and nonidealities such as fixed charge in the gate dielectric, the following holds in subthreshold [10], [25]:

$$V_{GS} = -\frac{Q_{dep} + Q_{it}}{C_{ins}} + \psi_s + \varphi_m - \varphi_s, \tag{3}$$

where $Q_{dep}$ is the depletion charge per unit area, $Q_{it}$ is the interface trap charge per unit area, $C_{ins}$ is the gate insulator capacitance per unit area, $\psi_s$ is the surface potential and $\varphi_m$, $\varphi_s$ are the workfunctions of the metal gate and semiconductor, respectively.

In particular $\varphi_s$ is important for the $\pi$-FET, since it depends on the semiconductor electron affinity $\chi_s$ and the bandgap $E_g$. Both these parameters are affected by the strain, and therefore by the converse piezoelectric effect [21], see also Section III.

For an n-type bulk MOSFET holds that

$$\varphi_s = \chi_s + \frac{E_g}{q} + \frac{kT}{q}\ln\left(\frac{N_V}{N_A}\right), \tag{4}$$

and for a p-type bulk MOSFET

$$\varphi_s = \chi_s + \frac{kT}{q}\ln\left(\frac{N_C}{N_D}\right). \tag{5}$$

Finally for an ultrathin body (UTB) device, e.g., double-gate FET or FinFET, holds

$$\varphi_s = \chi_s + \frac{E_g}{2q} + \frac{kT}{2q} \cdot \ln\left(\frac{N_C}{N_V}\right), \tag{6}$$

for both n- and p-type FETs. $N_{A,D}$ is the acceptor and donor concentration, $N_{C,V}$ is the effective density-of-states in the conduction and valence band, $k$ is Boltzmann's constant, and $T$ is the temperature. Further,

$$Q_{dep} \approx \mp\sqrt{\pm 2 \cdot q \cdot \varepsilon_s N_{A,D} \psi_s}, \tag{7}$$

with $\varepsilon_s$ the semiconductor permittivity. The upper (lower) sign corresponds to an n-type (p-type) FET. The depletion charge in long channel UTB devices can generally be neglected.

Since the potential barrier hence band alignment exponentially determines the subthreshold current (see also Eq. (11)), while transport parameters such as mobility $\mu_{n,p}$ and $N_{C,V}$ will have a less pronounced effect, in this work for simplicity we consider $\mu_{n,p}$ and $N_{C,V}$ to be independent of the strain hence the bias over the $\pi$-layer.

From Eqs. (3)–(6) it can then be derived for the n-type bulk MOSFET that

$$\frac{dV_{GS}}{d\psi_s} = \frac{C_{ins} + C_{dep} + C_{it}}{C_{ins} \cdot \left(1 + \frac{d\chi_s}{dV_{GS}} + \frac{1}{q} \cdot \frac{dE_g}{dV_{GS}}\right)}, \tag{8}$$

and for the p-type bulk MOSFET

$$\frac{dV_{GS}}{d\psi_s} = \frac{C_{ins} + C_{dep} + C_{it}}{C_{ins} \cdot \left(1 + \frac{d\chi_s}{dV_{GS}}\right)}, \tag{9}$$

while for the UTB FET

$$\frac{dV_{GS}}{d\psi_s} = \frac{C_{ins} + C_{it}}{C_{ins} \cdot \left(1 + \frac{d\chi_s}{dV_{GS}} + \frac{1}{2q} \cdot \frac{dE_g}{dV_{GS}}\right)}. \tag{10}$$

Here, $C_{dep}$ and $C_{it}$ are the depletion respectively interface trap capacitance per unit area ($C_{dep} = -\frac{dQ_{dep}}{d\psi_s}$, see Eq. (7)).

The terms depending on $\chi_s$, and $E_g$ in the denominators of Eqs. (8)–(10) form the tunable strain parameters caused by the converse $\pi$-effect. These parameters strongly depend on the device configuration as is discussed in Section III.

Generally the following relation holds for the subthreshold current:

$$I_D = \pm I_0 \cdot \exp\left(\pm\frac{\psi_s}{u_T}\right) \cdot \left(1 - \exp\left(\mp\frac{V_{DS}}{u_T}\right)\right), \tag{11}$$

with $u_T = kT/q$ the thermal voltage. The upper (lower) sign holds for n-type (p-type) FETs.

The prefactor $I_0$ depends on the type of FET. So holds for the long channel bulk FET [10]:

$$I_0 = \mu_{n,p}\frac{n_i^2}{N_{A,D}} u_T^2 \cdot C_{dep}\frac{W}{L}, \tag{12}$$

with $\mu_{n,p}$, $W$, $L$ is the charge carrier mobility, gate width, and channel length, respectively.

For long channel UTB devices holds:

$$I_0 = q\mu_{n,p} n_i u_T \cdot \frac{A_{body}}{L} \tag{13}$$

with $A_{body} = W \cdot t_s$ for the double-gate FET [26], $A_{body} = W_{FIN} \cdot H_{FIN} \cdot N_{FIN}$ for the FinFET, and $A_{body} = \pi \cdot R^2 \cdot N_{FIN}$ for the gate-all-around (GAA) FET [27]. $N_{FIN}$, $W_{FIN}$, $H_{FIN}$, $t_s$, $R$ are the amount of wires or fins, fin width, fin height, semiconductor thickness, and nanowire radius, respectively.

So far there have been no reports in case of an aggressively scaled UTB $\pi$-FET below the ballistic limit, i.e., for a channel length that is near or less than the mean free path $\lambda$. For deriving a closed form relation for the subthreshold current below the ballistic limit the so-called flux method [29]–[31] or scattering matrix approach (SMA) [28], [32] can be used. For the nanoscale FET the electrostatics are not fundamentally different [33]. Neglecting short-channel effects and considering three scattering matrices through the source, channel and drain region it can be derived that basically Eq. (11) holds with

$$I_0 = q \cdot (v_R B_Q) \cdot n_i \cdot A_{body}, \tag{14}$$

where $v_R$ is the Richardson velocity and

$$B_Q = \frac{T_0 \cdot (1-r)^2}{1 - 2(1-T_0)\,r + (1-2T_0)} = \frac{1-r}{1+r}. \tag{15}$$

Here the transmission coefficient $T_0 = \lambda/(\lambda + L)$ is assumed to be unity in the ballistic regime ($L \to 0$) and the source/drain backscattering coefficients to be the same $r_S = r_D = r$. An important difference between Eq. (13) and Eqs. (14), (15) is that for the former in principle the integral of the potential barrier is important, while for the latter the peak potential barrier matters most. For a long channel device $B_Q \approx \lambda/L$ and Eq. (13) is re-obtained. Note that for narrow UTB devices the channel quantum well in the subthreshold condition results in a constant offset of the band edges; this has no effect on the *SS* and therefore is not taken into account.

In Eqs. (4)–(6) and Eqs. (12)–(14) both $I_0$ and $\psi_s$ depend on $V_{GS}$. The former through $n_i$, hence $E_g$, the latter because of $\chi_s$, $E_g$ and the electrostatics.

Hence from Eqs. (11)–(14) we obtain

$$\frac{d\ln(I_D)}{dV_{GS}} = \mp\frac{1}{a \cdot kT} \cdot \frac{dE_g}{dV_{GS}} + \frac{1}{u_T} \cdot \frac{d\psi_s}{dV_{GS}}, \tag{16}$$

with a = 1, 2 for the bulk FET and UTB FET respectively. Again the upper (lower) sign holds for n-type (p-type) FETs.

Substituting Eqs. (8)–(10) in Eqs. (1) and (16) and after some manipulation we obtain for the n-type bulk FET:

$$m = \frac{C_{ins} + C_{dep} + C_{it}}{C_{ins} \cdot \left(1 + \frac{d\chi_s}{dV_{GS}}\right) - \frac{(C_{dep}+C_{it})}{q} \cdot \frac{dE_g}{dV_{GS}}}, \tag{17}$$

and for the p-type bulk FET:

$$m = \frac{C_{ins} + C_{dep} + C_{it}}{C_{ins} \cdot \left(1 + \frac{d\chi_s}{dV_{GS}}\right) + \frac{(C_{ins}+C_{dep}+C_{it})}{q} \cdot \frac{dE_g}{dV_{GS}}}. \tag{18}$$

For the n-type UTB FET we obtain:

$$m = \frac{C_{ins} + C_{it}}{C_{ins} \cdot \left(1 + \frac{d\chi_s}{dV_{GS}}\right) - \frac{C_{it}}{2q} \cdot \frac{dE_g}{dV_{GS}}}, \tag{19}$$

and finally for the p-type UTB FET we arrive at:

$$m = \frac{C_{\text{ins}} + C_{\text{it}}}{C_{\text{ins}} \cdot \left(1 + \frac{d\chi_s}{dV_{\text{GS}}}\right) + \frac{2C_{\text{ins}}+C_{\text{it}}}{2q} \cdot \frac{dE_g}{dV_{\text{GS}}}}. \tag{20}$$

In case of a negligible amount of strain we obtain the traditional text book equations [10], [25]: all terms in the denominators are zero except for $C_{\text{ins}}$.

For the $\pi$-FET, on the other hand, the parameters $\chi_s$ and $E_g$ depend on the strain hence applied bias $V_{\text{GS}}$ across the $\pi$-layer. $\chi_s$ needs to increase, hence the minimum conduction band $E_C$ needs to drop, with increasing strain values for the n-type $\pi$-FET while for the p-type $\pi$-FET the maximum valence band $E_V$ needs to increase as confirmed by numerical calculations [21]. Therefore the following conditions for the $\pi$-FET should hold:

$$\begin{array}{ll} \frac{d\chi_s}{dV_{\text{GS}}} = -\frac{1}{q}\frac{dE_C}{dV_{\text{GS}}} > 0 & (\text{n}-\text{type}) \\ \frac{dE_V}{dV_{\text{GS}}} = q\frac{d\chi_s}{dV_{\text{GS}}} - \frac{dE_g}{dV_{\text{GS}}} < 0 & (\text{p}-\text{type}) \end{array} \tag{21}$$

From Eqs. (1), (17), and (19) and the given conditions it can be concluded that the *SS* drops in the n-type $\pi$-FET compared to the same device without the $\pi$-layer. For the p-type FET this is more difficult to see. By checking the denominators of Eqs. (18) and (20) more carefully the terms $C_{\text{ins}} \cdot (1 + d\chi_s/dV_{\text{GS}})$ and $(C_{\text{ins}}/2q) \cdot dE_g/dV_{\text{GS}}$ add up to $(C_{\text{ins}}/q)(1 - dE_V/dV_{\text{GS}})$. Hence, we can also conclude that for p-type $\pi$-FET *SS* drops. However it will be less pronounced compared to an n-type $\pi$-FET [21] because $|(1/q)\,dE_V/dV_{\text{GS}}| < |d\chi_s/dV_{\text{GS}}|$, as addressed in Section III.

Further, it indeed appears that a subthermal *SS* value ($< \ln(10) \cdot u_T \approx 60$ mV/dec) can be obtained in UTB devices provided that $C_{\text{it}}$ is sufficiently low. However for the bulk FETs the *SS* strongly depends on the $C_{\text{dep}}$ (and of course $C_{\text{it}}$), though for the p-type bulk FET this is more important because of the additional positive right term in the denominator of Eq. (18). We will use Eqs. (17)–(20) for the discussion in the next section.

## III. DEVICE CONFIGURATIONS

To achieve subthermal switching performance as described in the previous paragraph, the transistor channel strain must be modulated by a control voltage. In recent work we have proposed to implement this by the integration of a piezoelectric material such as PZT or AlN [21], [22]. Fig. 2 shows the envisaged configurations of field effect transistors with a piezoelectric strain modulation layer.

The most straightforward and compact arrangement is obtained by replacing the gate dielectric by a piezoelectric insulator and hence by placing it directly on the silicon, as depicted in Fig. 2(a). This arrangement benefits from the fact that piezoelectric materials exhibit a relatively high dielectric constant, but it is expected that a subthermal *SS* is not reached for this case. The reason for this is that the dielectric should be surrounded by charge, preferably a lot. In case of a long channel FET in subthreshold condition this basically should be the depletion charge (or $C_{\text{dep}}$) in the grey area: the higher the amount of charge the higher the field, hence $\pi$-effect. However, when we check Eqs. (17)–(18) we see that $C_{\text{dep}}$ counteracts with the $\pi$-effect. Therefore the *SS* will be reduced by the $\pi$-effect but won't reach a subthermal value.

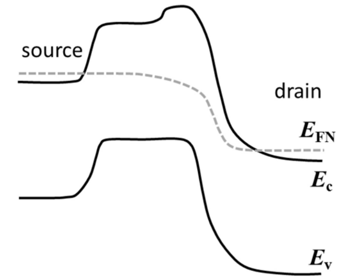


**FIGURE 3. Schematic band diagram of the $\pi$-FET (Fig. 1) in the current flow direction just underneath the gate-dielectric. A potential barrier is formed at the drain side because of the high gate and drain potential. It is expected that this reduces the DIBL effect.**

Related to this, simply replacing the gate dielectric by a piezoelectric insulator in a long channel UTB FET configuration will change the strain only slowly in the subthreshold regime as not all of the voltage drops over the dielectric ($C_{\text{dep}}$ can be neglected). Hence the strain will indeed be modulated in this arrangement, but only strongly in accumulation and inversion. Further, the carrier mobility may deteriorate in the presence of a polar material such as a piezoelectric layer.

There is one more topic to consider and that is the short-channel effect (SCE). When we reduce the device dimensions of course the high amount of charge present in the source and drain regions will become dominant that increases the $\pi$-effect. As a result, there might be a reduced *SS* but again no subthermal values, both for bulk and UTB FETs. Also, depending on the shape of the source/drain doping profiles band-to-band tunneling will become more important because of the strain-induced $E_g$ narrowing. Related to this, when using short channel $\pi$-FETs the drain-induced barrier lowering (DIBL) effect will be less compared to the classical counterpart. Since the gate-drain voltage at maximum current is near zero the field through the $\pi$-layer at the drain side will be low, and as a result the band alignment in the semiconductor is not affected. We basically obtain a change in the band alignment along the current flow direction, where a potential barrier is formed at the drain side, see Fig. 3. This makes the subthreshold current less sensitive to the drain bias. Of course this should be verified experimentally.

From the technology point of view there is another issue. A $\pi$-material with a high piezoelectric response such as lead zirconate titanate (PZT) [34], [35] and Si (or perhaps any other semiconductor) technology are mutually not compatible. To combine these materials, and to avoid ferroelectric performance degradation and atom interdiffusion through interfaces, a so-called buffer or seed layer is required [36]–[38] to avoid direct contacting on a semiconductor.

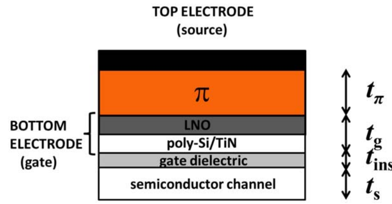


**FIGURE 4. Schematic cross section of a metal-ferroelectric-metal (MFM) capacitor on top of a semiconductor substrate. In our experiments [39], we used for the top electrode (source) Pt/Ti, for the bottom electrode (gate) an LNO/poly-Si/TiN stack, and for the gate dielectric $SiO_2$ was used. For the discussion in the layer thicknesses are indicated. The dimensions are not to scale.**

Earlier we did some experiments on metal-ferroelectric-metal (MFM) capacitors on top of a gated Si channel, see Fig. 4. For these capacitors a lanthanum nickelate, $LaNiO_3$ (LNO), layer was used as a buffer layer for the PZT layer on top of a traditional poly-Si/TiN/$SiO_2$ gate stack [39]. X-ray photoelectron spectroscopy (XPS) was used here to obtain the compositional depth profile of the fabricated multi-film stack. XPS analysis is generally used to get information on the material distribution in different layers and on interfaces. It can detect diffusion of impurity atoms (e.g., Pb) into the silicon channel below the PZT/LNO/poly-Si/TiN/$SiO_2$ stack. This is important to know since the impurity diffusion can degrade the performance of the underlying transistor.

Fig. 5 shows the XPS depth profile in such a capacitor. Starting from the surface the PZT layer is recognized. Below that layer the LNO buffer, poly-Si and TiN layers can be observed. Further down is the $SiO_2$ gate dielectric. No diffusion of Pb in the Si layer is observed within the resolution limit of XPS ($\sim$ 0.5 at. %). This gives an indication that, when deposited on devices, there will be no degradation on the transistor properties as confirmed in our Si $\pi$-FinFET data [22].

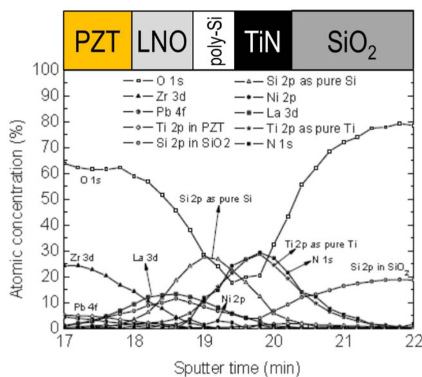


**FIGURE 5. XPS depth profile of the MFM capacitor from top to $SiO_2$ layer. In this experiment, LNO is used as buffer layer, the poly-Si and TiN layers are used as a gate, and the $SiO_2$ layer is used as a gate dielectric. The layer stack is schematically drawn on top of the graph to guide the eye.**

Given these considerations we chose to study the configurations in Fig. 2(b)–(d) in more detail. Here, the piezoelectric film is positioned *outside* the gate stack. The gate metal both shields the horizontal (source-drain) field and may act as a diffusion barrier. Depending on the $\pi$-material additional buffer layers may be required. So basically there is no electrical contact between the $\pi$-layer and semiconductor body, rather an indirect mechanical contact. Of course, tunnel FETs [13], [20] or Junction-less transistors [40] could also be formed in each of these configurations.

One advantage is that $Q_{dep}$ in all devices is no longer important for the $\pi$-effect because the full $V_{GS}$ can be applied over the $\pi$-layer. In case of long channel devices we can omit all $C_{dep}$ terms in Eqs. (17) and (18). This means that irrespective the use of a bulk $\pi$-FET of any UTB $\pi$-FET a subthermal $SS$ can be obtained. Note that in these configurations $C_{ins}$ in Eqs. (17)–(20) no longer depends on the $\pi$-layer properties.

So far we have not discussed the mechanics and the mechanical boundaries. For planar devices, such as those depicted in Fig. 2(a)–(c), when we apply a voltage over the $\pi$-layer depending on the polarity of the voltage and $\pi$-material the $\pi$-layer thickness will deform. In conventional planar FET designs the top (or gate) metal is more or less free, i.e., mechanically floating. This means when we apply a bias over the $\pi$-layer some, perhaps most, of the electromechanical energy is not used to strain the semiconductor body and hence is lost. It is therefore advisory to mechanically fix the top metal in the third dimension using e.g., anchors attached to the either a substrate of (preferably) a stiff dielectric. This problem is more or less solved in the symmetric $\pi$-FinFET configuration as depicted in Fig. 2(d). In this case we have a symmetric mechanical boundary condition. However, in this configuration we need to have a good step coverage of the $\pi$-layer around the device, which is a problem since for this uniform deposition techniques such as atomic-layer deposition may be required [22] which is not straightforward in particular for ternary or quaternary compounds. For this AlN can be used as an alternative piezoelectric material, which can be deposited by ALD [41], [42]. However, as mentioned before AlN has a ten times lower piezoelectric response compared to PZT. In addition, the issue of the mechanical boundary condition can also be elegantly solved by utilizing a GAA device geometry encapsulated in stiff material.

There is an indirect mechanical contact between the $\pi$-layer and semiconductor body in the configurations of Fig. 2(b)–(d), which requires more effort to reduce $SS$ effectively. When the mechanical gate is connected to the source it can be derived for the strain in the (100) oriented semiconductor body [21]:

$$s_s = -\frac{\frac{e_\pi V_{GS}}{c_\pi c_s}}{\left(\frac{t_s}{c_s} + \frac{t_{ins}}{c_{ins}} + \frac{t_g}{c_g} + \frac{t_\pi}{c_\pi}\right)}, \tag{22}$$

where $t_{\pi,ins,g}$ is the thickness of the $\pi$-, insulator and gate metal layer (see also Fig. 4), $c_{\pi,ins,s,g}$ is the stiffness of the $\pi$-, insulator, semiconductor and gate metal layer,

and $e_\pi$ is the piezoelectric (charge) constant. Note that the physical parameters $e_\pi$ and $c_{\pi,\text{ins,s,g}}$ are tensors but in this one-dimensional relation have been assumed to be scalars for simplicity sake. Consequently, shear strain components have been ignored as well. In real life these parameters, in particular $c_\pi$ and $e_\pi$, depend on the crystal (and device) orientation and field direction. From Eq. (22) we can derive the $\chi_s$ and $E_g$ strain dependence via the deformation potentials in the conduction band and valence band. Basically it can be summarized that:

$$\chi_s(s_s) = \chi_{s0} - \Xi_{C,\text{eff}} \cdot s_s, \tag{23}$$

$$E_g(s_s) = E_{g0} + \left(\Xi_{C,\text{eff}} - \Xi_{V,\text{eff}}\right) \cdot s_s, \tag{24}$$

with $E_{g0}$ and $\chi_{s0}$ are the bandgap and workfunction of the relaxed semiconductor, and $\Xi_{C,\text{eff}}$, $\Xi_{V,\text{eff}}$ are the "effective" deformation potential in the conduction band and valence band of the semiconductor, respectively. These "effective" parameters are introduced to avoid numerous details [21], [43]–[47] which are not important for this discussion. More importantly, in case of III-V materials a tensile (compressive) $s_s$ value is required for the n-type (p-type) FET because $\Xi_{C,\text{eff}}$ and $\Xi_{V,\text{eff}}$ are both negative in sign. For germanium (Ge), Si on the other hand a compressive $s_s$ value is required irrespective of the type of FET ($\Xi_{C,\text{eff}}$, $\Xi_{V,\text{eff}}$ is positive respectively negative in sign) [21]. Also $|\Xi_{C,\text{eff}}| > |\Xi_{V,\text{eff}}|$ for all materials and consequently the converse $\pi$-effect is in principle more effective for n-type FETs. From Eqs. (22)–(24) we obtain relations for $d\chi_s/dV_{GS}(= -\Xi_{C,\text{eff}} \cdot s_s/V_{GS})$ and $dE_g/dV_{GS}$ $(= \left(\Xi_{C,\text{eff}} - \Xi_{V,\text{eff}}\right) \cdot s_s/V_{GS})$ needed for the *SS*, see Eq. (21).

From Eqs. (22)–(24) we can also conclude the following. First, for reducing mechanical losses ultrathin and relatively stiff interfacial layers in between the $\pi$- and semiconductor body are required (e.g., hafnium-oxide ($HfO_2$) instead of $SiO_2$). In particular the stiffness is important for the gate metal since the workfunction of the metal could also depend on the amount of strain. This effect has been reported before for titanium-nitride (TiN) [48]–[50]. Because of its high stiffness relatively high stress values are required to change the workfunction. Second, the semiconductor body should preferably have a low stiffness and a high deformation potential (e.g., germanium, III-Vs [44], [47]), and third, the $\pi$-material should preferably have a high piezoelectric response, but also a high breakdown field $E_{cr}$ [21].

Fig. 6 shows simulation data for three types of n-type Ge FinFETs [21]: a device without strain (i.e., relaxed), one with a fixed strain value of 1.6%, and another device with tunable strain (the $\pi$-FinFET) with PZT as a piezoelectric layer. In the latter the maximum strain level is 1.6% at $V_{DS}$ = 1 V. The simulations were performed in mixed-mode: Comsol Multiphysics was used for the mechanical domain and used as input for the TCAD Sentaurus (Synopsys) simulation tool used for the electrical domain. For comparison the analytical model obtained from [26] has been plotted in the same graph in which the conduction band has been adjusted depending on the amount of strain according to Eq. (23) where $\Xi_{C,\text{eff}} \approx 12.4$ eV for Ge [43]. The results show that for an increased fixed strain value the subthreshold current increases exponentially while the *SS* does not change. However, for the $\pi$-FinFET the *SS* has been reduced to 50 mV/dec ($T$ = 300 K), indicating that subthermal *SS* values can be obtained.

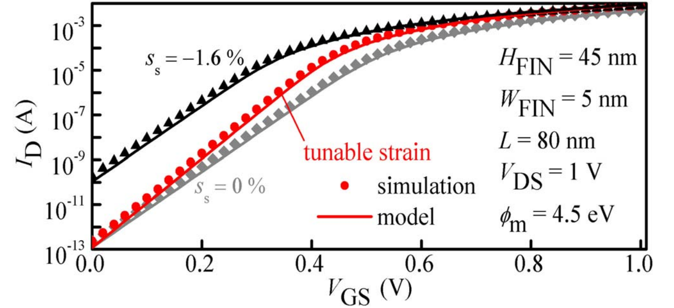


**FIGURE 6. Simulated and modeled $I_D$-$V_{GS}$ characteristics of an n-type Ge FinFET (Fig. 2(d)) with tunable strain ($\pi$-FinFET) and with constant strain [21] ($T$ = 300 K). All devices have a 1.5-nm thick hafnium-dioxide ($HfO_2$) layer for the gate dielectric and a 3-nm thick titanium-nitride (TiN) layer for the gate metal. The $\pi$-FinFET consists of a 10-nm thick PZT layer.**

In summary, depending on the boundary conditions in the processing, mechanics and device physics several device configurations have been proposed and discussed for the $\pi$-FET concept. These configurations could potentially reach subthermal *SS* values.

## IV. POWER CONSUMPTION

The reason to investigate steep subthreshold slope devices is the promise of a lower power consumption. In this section we estimate the effect of strain modulation on the power consumption of a transistor that is used in digital logic circuitry. The total power consumption can be divided into two parts. The first is the dynamic power $P_{dyn}$, which in digital logic is the energy required to switch the transistor state [51] and multiplied by the number of switches per second. The second is the static power $P_{stat}$, given by the leakage current multiplied by the supply voltage.

The strain modulation effect can be employed in different ways. For instance either the supply voltage $V_{DD}$ can be kept the same and consequently the leakage current $I_{off}$ is reduced, resulting in a lower $P_{stat}$, or the $I_{off}$ can be kept constant and the $V_{DD}$ is reduced, resulting mostly in a lower $P_{dyn}$. In the $\pi$-FinFET a piezoelectric capacitance is added parallel to the gate capacitance. For each cycle both must be charged and discharged, and as a result this adds up to $P_{dyn}$. Hence it is unlikely that the $\pi$-FinFET is able to reduce the $P_{dyn}$. However, it can reduce the $P_{stat}$ at the cost of an increased $P_{dyn}$. We follow [51], and note that the $P_{dyn}$ is given by the sum of the charge required to charge both the oxide $P_{ins}$ and the piezoelectric layer $P_\pi$ and find

$$P_{ins} = W \cdot L_g \cdot \alpha \cdot f_{clk}\, f_o \frac{V_{DD}^2}{2} C_{ins} \tag{25}$$

$$P_\pi = W \cdot L_g \cdot \alpha \cdot f_{clk} f_o \frac{V_{DD}^2}{2}\left(\frac{\varepsilon_\pi}{t_\pi} + \frac{s_\pi \cdot e_\pi}{V_{DD}}\right) \quad (26)$$

$$P_{stat} = I_{off} \cdot V_{DD} \cdot \exp\left(\frac{\Xi_{C,eff} \cdot s_s}{u_T}\right) \quad (27)$$

where $\alpha$ is the switching activity factor, $f_{clk}$ is the clock frequency, $f_o$ is the tapering factor (the number of switches each transistor has to drive), $W$ is the gate width, $L_g$ is the gate length, and $I_{off}$ is the off-current of a device without strain (see e.g., Eqs. (11) and (13), with $V_{DS}$=$V_{DD}$, $V_{GS}$=0). Note that the leakage through the piezoelectric layer can be ignored in this discussion since its current density is less than $\sim 10^{-4}$ A/cm$^2$ which is much less than the value reported for the gate leakage [52], [53].

The band deformation due to the induced strain is given by $\Xi_{C,eff} \cdot s_s$, where $\Xi_{C,eff}$ is the effective deformation potential. Further, $t_\pi$, $\varepsilon_\pi$, and $s_\pi$ is the thickness, permittivity, and strain in the $\pi$-layer, respectively. $t_\pi$ is calculated by assuming that the maximum field $E_{cr}$ is over the $\pi$-layer when $V_{DS} = V_{DD}$, i.e., $t_\pi = V_{DD}/E_{cr}$ [21]. The strain values $s_s$, $s_\pi$ can be calculated using Eq. (22).

Hence, the piezoelectric power scales with the sum of the permittivity and the strain in the piezoelectric layer. The equations can be used to estimate whether strain modulation can reduce the power consumption of a transistor. In the general case we can only answer that it strongly depends on all the material parameters, device dimensions, frequency of operation and usage of the devices. However, we can state that strain modulation can reduce the $P_{stat}$ at the cost of an increased $P_{dyn}$, hence it can only be beneficial in circuits where $P_{stat}$ dominates the total power consumption.

An estimation for the device parameters in the future can be found in the ITRS roadmap [1]. We used the device parameters from the 2011 edition for the FEP4 Low Standby Power Devices Technical Requirements, other parameters used are summarized in Table 1. For the $\pi$-layer we considered PZT, for the semiconductor Ge, for the gate metal layer TiN, and gate insulator HfSiO. From this roadmap we estimated the expected $P_{stat}$ and $P_{dyn}$ for an n-type transistor, and these are shown in Fig. 7. The graph shows that $P_{stat}$ exceeds $P_{dyn}$ for technologies with gate lengths below 18 nm. Next, following Eqs. (26) and (27) we estimated the effect piezoelectric strain modulation can have on the power consumption. We tuned the piezoelectric layer thickness, and thus the strain modulation and corresponding power $P_{ins}$, to obtain a minimal total power. To illustrate the numbers at $L$ = 5 nm, the tuned piezoelectric thickness is 48 nm, its dielectric constant is assumed to be 150, while the gate oxide thickness is 0.5 nm. We found that from $\sim$ 8 nm gate length onward the estimated $P_{stat}$ is significantly higher than $P_{dyn}$. There the strain modulation can reduce the total power consumption of a transistor, even at the cost of the additional $P_{dyn}$ of the $\pi$-layer.

**TABLE 1. Device parameters used for estimating the power consumption of the $\pi$-FET (see Fig. 7). $E_{cr}$ is the breakdown field for PZT used to scale $t_\pi$ (= $V_{DD}/E_{cr}$). Other parameters such as $t_{ins}$, $V_{DD}$, $I_{off}$, and gate length have been taken from [1]. Note that for the permittivity of PZT the high field (near $E_{cr}$) value has been used.**

| $\alpha$ | 0.01 [54] | $c_{ins}$ | 70 GPa |
|---|---|---|---|
| $c_g$ | 660 GPa | $c_s$ | 131 GPa |
| $c_\pi$ | 117 GPa | $\varepsilon_{ins}$ | 13 |
| $\varepsilon_\pi$ | 150 | $e_\pi$ | 23.3 C/m$^2$ |
| $E_{cr}$ | 1 MV/cm | $f_o$ | 3 [54] |
| $t_g$ | 5 nm | $t_s$ | 5 nm |
| $T$ | 300 K | $\Xi_{C,eff}$ | 12.4 eV |

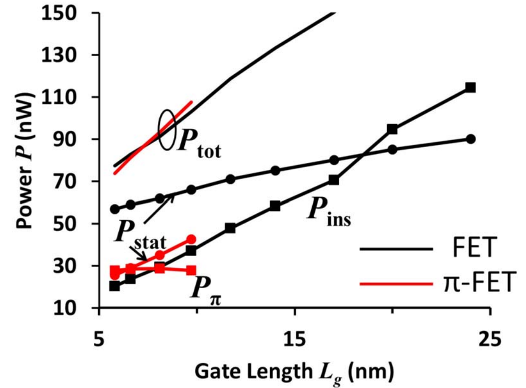


**FIGURE 7. Estimated power of an n-type transistor calculated from the ITRS [1] prognoses for device parameters and performance (black line). An estimate for the strain modulation effect on the power consumption is shown in red. Please note that the strain modulation is used to decrease the static power consumption. Hence, $P_{ins}$ is the same for both transistors.**

## V. CONCLUSION

In this work we have discussed the effect of the envisaged device configurations for the $\pi$-FET based on simple estimations. It is expected that a $\pi$-layer in direct contact with the semiconductor body will not result in subthermal *SS* values. However for the proposed device configurations subthermal *SS* can be reached depending upon the mechanical boundary conditions, such as mechanical material properties, interfacial layer thicknesses and device design. Based on the ITRS roadmap the main benefit in the power consumption is estimated to occur from 8 nm gate length onwards. In case of standby operation the total power consumption is primarily determined by the static power consumption which will then make the $\pi$-FET concept an attractive candidate. However for our experimental work more research is needed to obtain subthermal *SS* values following the guidelines of this work in addition to well controlled interfaces.

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