Tunable N-Path Notch Filters for Blocker Suppression: Modeling and Verification

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Abstract **— N-path switched-RC circuits can realize filters with very high linearity and compression point while they are tunable by a clock frequency. In this paper both differential and single-ended N-path notch filters are modeled and analyzed. Closed-form equations provide design equations for the main filtering characteristics and non-idealities such as: harmonic mixing, switch resistance, mismatch and phase imbalance, clock rise and fall times, noise and insertion loss. Both an 8-path single-ended and differential notch filter are implemented in 65nm CMOS technology. The notch center frequency which is determined by the switching frequency is tunable from 0.1-1.2GHz. In a 50Ω environment the N-path filters provide power matching in the pass-band with an insertion loss of 1.4-2.8dB. The rejection at the notch frequency is 21-24dB, P_{1dB}> +2dBm and IIP3> +17dBm.**

Index Terms — N-path filter, tunable filter, high linearity, linear periodically time variant circuit, LPTV, commutated capacitors, frequency translated filter, high-Q, CMOS, notch filter, band-stop filter inductorless filter, cognitive radio, software-defined radio, coexistence, blocking, blocker suppression.

I. INTRODUCTION

The demand for multi-mode multi-band wireless handheld devices has been pushing the integration of many wireless transceivers on a single RFIC chip, leading to a reduction in cost, size and power consumption. However, close proximity of wireless transceivers, which are also supposed to work concurrently, poses a very challenging coexistence problem: the transmitted signal of one transmitter becomes a "blocker" for co-existing receivers (see Fig. 1a), which can be stronger than 0dBm. A somewhat similar problem occurs in a single standard wireless systems with frequency division duplexing (FDD) where the receiver and the transmitter share the same antenna through a duplexer as shown in Fig. 1b (e.g. W-CDMA). Although the duplexer provides some selectivity still leakage of the transmitted power to the receiver can deteriorate the sensitivity of the receiver. Similar challenges also occur when aiming at Dynamic Spectrum Access, exploiting software defined radio concepts.

In order to provide suppression for blockers, a notch filter can be applied in the receiver. A high-Q filter is needed, e.g. 10MHz bandwidth around 1GHz asks for a Q of 100. Given the desire to support multiple radio bands, a software defined radio solution is preferred, i.e. a filter which is widely tunable in a digitally controlled way.

A well-known way to implement a high-Q notch filter is by applying an LC resonator assisted with a Q-enhancement negative impedance circuit to overcome the limited Q of on-chip inductors (see Fig. 2a) [1] Apart from consuming a large die area, these circuits suffer from limited linearity and poor noise performance due to the application of active components in the negative impedance circuit. Moreover the tunability, usually implemented with varactors, is limited and makes the bandwidth of the notch filter frequency dependent. Finally the center frequency is strongly related to the process variations and parasitics which makes the design even more difficult. Another approach to realize a bandstop filter is applying the frequency translated filtering. As an example in [2] the low input impedance of a transimpedance amplifier with feedback is upconverted to create a notch filter at low frequencies (80MHz) suppressing TX leakage in an FDD system (see Fig. 2b).

Frequency translated filtering recently has gained attention to realize high Q inductorless filters with wide tunability and high linearity and compression points [2-9]. Albeit independently re-invented with innovative contributions, the basic concept can be traced back at least to the 50s [10]. Basically a filter in baseband is frequency-shifted to a high frequency by means of frequency mixers. Thus the mixer LO-frequency defines the center frequency, and the baseband filter defines the filter shape. In [4] a notch filter with a combination of active and passive mixers is applied in a feedforward path realizing a band-pass filter.

Applying the fully passive mixers to implement N-path filters is a key factor in achieving high linearity and compression point. As we presented in [5, 6] a fully differential 4-path band-pass filter with passive mixers, using NMOS switches and capacitors provides a decade of center frequency range with good linearity (IIP3 >14dBm), a high 1dB compression point >0dBm and a few dB noise figure. In [7], these 4-path band-pass filters with passive mixers are embedded in an LNA providing filtering in a SAW-less receiver for GSM/GPRS/EDGE. Moreover, in [8] the N-path concept is utilized to implement a complex impedance to provide image rejection in a superheterodyne receiver. Passive mixers terminated with capacitors can also be modeled as N-path filters considering the RF-node, whereas they also provide down-converted baseband signal output on the capacitors [11-14].

In [15] we presented a differential and a single-ended (SE) 8-path notch filter. These switched-RC 8-path notch filters demonstrate a very high-Q band-stop characteristic with a center frequency determined by the switching frequency which can have a very low sensitivity to the PVT (Process, Voltage, and Temperature) variations.

To exploit N-path filters, we need a clock and the question arises how to realize this clock. If we aim at rejecting a "self-blocking" transmitter signal, this can be relatively straightforward as the synthesized frequency is readily available. However, if we aim at applying N-path notch filters for Dynamic Spectrum Access applications, we need information about the blocker frequency. This information can come from databases that are currently built [16] or from spectrum sensing, see for instance [17, 18]. The clock generation will require extra hardware in the system. Note however that apart from N-path filters there are hardly other integrated filter techniques that can handle 0dBm blockers while also providing tunable filtering. This is especially true at low GHz frequencies, where inductor takes large chip area and have rather poor quality factor. On the other hand new CMOS technologies offer high density linear capacitors and switches with low "on" resistance, low nonlinearity and low parasitic capacitance. This allows for realizing purely passive notch filters with high linearity and large blocker handling capability.

In this paper we provide a thorough analysis of N-path notch filters with closed form equations. The analysis results describe the main characteristics of the notch filters such as bandwidth and maximum rejection at notch frequency. They also provide comprehensive quantitative results for non-ideal properties of the N-path notch filters such as harmonic mixing, the effect of the switch resistance, reduced duty cycle, pass-band insertion loss, noise figure, mismatch and phase imbalance. Similar to the N-path band-pass filters in [6] a simple RLC model is presented for the frequencies close to the switching frequency which describes

the main properties of the N-path filters in a quite simple but rather accurate manner. Moreover, in this paper extra measurement results will also be provided for the 8-path notch filters compared to [15], most notably transfer function and notch depth measurements under strong blocking conditions.

In section II a short intuitive introduction of N-path notch filters is presented, while section III covers mathematical analysis. In Section IV important non-idealities of the N-path notch filters are discussed based on the analysis results of section III. Sections V and VI cover the implementation and measurement results of the 8-path notch filters, while section VII presents conclusions.

II. N-PATH NOTCH FILTER CONCEPT

Fig. 3a illustrates how up-converting a high-pass filter characteristic in the baseband to the LO frequency results in a band-stop or notch behavior. The high-pass filter can be as simple as a C-R network (Fig. 3b) and the mixers in Fig. 3a can be realized by switches driven by multiphase clocks (Fig. 3c). The resistances of the high-pass filters in Fig. 3b are not memory elements and only one path is active at any time, so one shared resistor can be used (Fig. 3c). Moreover, in each path one of the two switches can be removed if we assume the clock phases driving the two involved switches are the same. Thus the simple single-ended (SE) notch filter shown in Fig. 3d results.

Considering the single-ended N-path notch filter in Fig. 3d for N=8, a typical set of node voltages for a sinusoidal signal with the frequency of the switching frequency as an input is illustrated in Fig. 4. Here we assume that the RC time constant is very much larger than the closing time of the switches. This allows us to assume that the voltages on the capacitors contains approximately a constant value which is the integration of the part of the input signal seen periodically by each capacitor. The passive mixers which are realized by the switches, up-convert the DC voltages on the capacitors and create a stair case approximation of the input signal on the switched-capacitor part in Fig. 3d as V_{SC}. The output voltage $V_{out} = (R_L /(R_L + R_S))(V_S - V_{SC})$ in Fig. 4 illustrates a strong suppression of the input signal. As a result the switched-capacitor part in combination with the source and load resistors act as a high impedance element for the switching frequency while it presents a low impedance for the frequencies far away from the switching frequency. However, note that this circuit not only will present a notch characteristic at the switching frequency but also at the harmonics of the switching frequency. At first sight this may seem similar to some comb filters or microwave filters, but here it results from mixing effects and the clock periodicity defines the

frequency spacing. Note also that apart from repeated filter responses, the mixing nature of the circuit also introduces unwanted mixing products. These will be analyzed later in this paper.

A fully differential N-path notch filter architecture is shown in Fig. 3e. A second set of switches is required to generate the differential signal at the output. As a result of the fully differential structure, the notch behavior at the even harmonics of the switching frequency is cancelled, so the pass-band is widened compared to the single-ended version.

Despite the unwanted responses, the N-path filters can achieve very high Q, whereas they are digitally tunable in the center frequency by simply changing the mixer clock frequency. However, insight in several second order effects is needed to successfully apply N-path circuits, and we hope to provide such insight and quantitative estimates for filter properties in this paper.

III. MATHEMATICAL ANALYSIS

A. State Space Analysis

In [6] we provided the detailed analysis results for a differential N-path bandpass filter. Here we will follow the same analysis approach to derive the transfer functions for the SE and the differential notch filters. The circuits shown in Fig. 3 are linear periodically time variant (LPTV) systems. If we define the voltage on the switched-capacitor part as: $V_{SC}(j\omega) = V_X - V_{out}$, it can be shown that the relation between $V_{SC}(j\omega)$ and the input in such an LPTV circuit will comply with the following equation [19, 20]:

$$V_{SC}(j\omega) = \sum_{-\infty}^{\infty} H_n(j\omega) V_S(j(\omega - n\omega_S)) \tag{1}$$

where $\omega_S = 2\pi f_S$ is the switching frequency, "n" indicates a harmonic of f_S and $H_n(j\omega)$ is the "nth harmonic transfer function" associated with the frequency shift of nf_S. Equation (1) models the frequency spectrum for $V_{SC}(j\omega)$ as a summation of shifted versions of the input spectrum multiplied by a weighting factor $H_n(j\omega)$. Please note that if, for the purpose of analysis, R_L in Fig. 3d/e is shifted before the switched-capacitor section, then the architecture becomes similar to a bandpass N-path filter. As a result $H_n(j\omega)$ can be found similar to the bandpass N-path filters as in [6, 21]. Here we will apply the approach discussed in [6] which provides exact equations in the passband and also stopband of the filters including all side-

band transfers. Consiquently by finding $V_{SC}(j\omega)$ in (1) the output spectrum relates to the input as following:

$$V_{out}(j\omega)=\frac{R_L}{R_L+R_S}\left(V_S(j\omega)-V_{SC}(j\omega)\right)= \\ \frac{R_L}{R_L+R_S}\left(\left(1-H_0(j\omega)\right)V_S(j\omega)-\sum_{n=-\infty,n\neq 0}^{\infty}H_n(j\omega)V_S(j(\omega-n\omega_s)\right) \tag{2}$$

According to (2) the output voltage on R_L consists of two parts: 1) the desired part " $V_{de}(j\omega)$ " which provides filtering without frequency shifting, and 2) " $V_{un}(j\omega)$ " which entails possible folding back components that might fall in the desired band. Then $V_{out}(j\omega)=V_{de}(j\omega)+V_{un}(j\omega)$.

$$V_{de}(j\omega)=\frac{R_L}{R_L+R_S}\left(1-H_0(j\omega)\right)V_S(j\omega) \tag{3}$$

$$V_{un}(j\omega)=\frac{-R_L}{R_L+R_S}\left(\sum_{n=-\infty,n\neq 0}^{\infty}H_n(j\omega)V_S(j(\omega-n\omega_s))\right) \tag{4}$$

As shown in [6, 22] a state space analysis can be carried out on a single path of an N-path system and by considering the fact that the output spectrum for an N-path system is the superposition of the responses of "N" similar paths after appropriate phase shifting, the frequency response for $V_{SC}(f)$ can be determined. This is possible because we assume that the state variables do not have any interaction with each other and are determined independently from each other.

The timing diagram for the analysis is shown in Fig. 5. The time interval $nT_S<t<nT_S+T_S$. $T_S=1/f_S$ is divided into M portions (M is the number of the states) and each portion identified by k can be represented as $nT_S+\sigma_k<t<nT_S+\sigma_{k+1}$, k=0,…, M-1 and $\sigma_0=0$ (see Fig. 5). During each interval there is no change in the state of the switches and the network behaves as an LTI system. Suppose $\tau_0, \tau_1, \ldots, \tau_{N-1}$ are the time intervals in which each switch is closed. Here we have assumed that there is no overlap in the multiphase clocks and also that $\tau_0+\tau_1+\ldots+\tau_{N-1}=T_S$ (later this assumption will be modified to cover the case of a duty cycle lower than 1/N).

B. Single-Ended Notch Filter Harmonic Transfers

By applying the state space analysis for the SE N-path notch filter we find the harmonic transfer function of $H_n(j\omega)$ in (1) as :

$$H_{n,SE}(j\omega)=\sum_{m=0}^{N-1}e^{-jn\omega_s\sigma_m}H_{n,m,SE}(j\omega)$$

$$H_{n,m,SE}(j\omega)=\frac{1}{1+j\omega/\omega_{rc,SE}}\times\left(\frac{1-e^{-jn\omega_s\tau_m}}{j2\pi n}+\frac{1-e^{j(\omega-n\omega_s)(T_s-\tau_m)-jn\omega_s\tau_m}}{2\pi\dfrac{\omega_{rc,SE}}{\omega_s}}G_{SE}(j\omega)\right)$$

$$G_{SE}(j\omega)=\frac{e^{j(\omega-n\omega_s)\tau_m}-e^{-\omega_{rc,SE}.\tau_m}}{e^{j2\pi(\omega-n\omega_s)/\omega_s}-e^{-\omega_{rc,SE}.\tau_m}}\cdot\frac{1}{1+j(\omega-n\omega_s)/\omega_{rc,SE}}$$

(5)

Where $\omega_{rc}=1/((R_S+R_L)C)$. Moreover; $H_{n,m}(j\omega)$ defines the n[th] harmonic transfer for the m[th] path of the N-path filter (m=1, 2 ,..., N). In (5) $G(j\omega)$ as discussed in [6, 22] is the frequency transfer response which is generated by the initial and end conditions added at the beginning and subtracted at the end of each time interval. In fact if we apply a complex exponential as $A\exp(j\omega t)$ to the input of a single path in Fig. 3d the output at discrete moments can be found as $v_{out}(nT_s)=G(j\omega)(A\exp(j\omega nT_s))$. The frequency transfer at other discrete moments can be found as an added phase shifts to this value [22].

In order to find the overall frequency response we need to add the frequency response for all paths considering the phase shift defined by the term $e^{-jn\omega_s\sigma_m}$ in the first equation in (5). For an ideal N-path filter we assume $\tau_0=\tau_1=...=\tau_{N-1}=\tau=DT_S$ in Fig. 5, where $D=(1/N)$ is the duty cycle of the multiphase clocks. As a result $H_{n,m}(j\omega)$ and $G(j\omega)$ will be similar for all paths.

We will now derive equations for $H_0(j\omega)$ to find the desired part of the transfer function in (3). Analysis of (5) shows that $H_n(j\omega)$ is undefined for *n*=0, but we can take the limit of (5) when "*n*" approaches continuously to zero to find $H_0(j\omega)$. Moreover, in deriving (5) we assumed $D=(1/N)$ (non-overlapped switching). When $D<(1/N)$, there are periodic time intervals that all of the switches are off and $V_{SC}(j\omega)$ is tracking the input signal. The output spectrum contribution generated due to this fact is not considered in (3). In order to include this effect in $H_0(j\omega)$, the factor (1-ND) should be added to the part which is derived from (5) by taking the limit for "n" to zero. Finally for the single-ended filter we find:

$$H_{0,SE}(j\omega)=\frac{N}{1+j\dfrac{\omega}{\omega_{rc,SE}}}\times\left(D+\frac{1-e^{j\omega(T_S-\tau)}}{2\pi\dfrac{\omega_{rc,SE}}{\omega_s}}\left(\frac{e^{j\omega\tau}-e^{-\omega_{rc,SE}.\tau}}{e^{j2\pi\omega/\omega_S}-e^{-\omega_{rc,SE}.\tau}}\cdot\frac{1}{1+j\dfrac{\omega}{\omega_{rc,SE}}}\right)\right)+(1-ND)$$

(6)

C. Differential Notch Filter Harmonic Transfers

For the differential circuit in Fig. 3e the state space analysis results in the following result for $H_n(j\omega)$ in (1):

$$H_{n,D}(j\omega)=\sum_{m=0}^{N-1}e^{-jn\omega_s\sigma_m}H_{n,m,D}(j\omega)$$

$$H_{n,m,D}(j\omega)=\frac{1}{1+j\dfrac{\omega}{\omega_{rc,D}}}\times\left(\frac{1-e^{-jn\omega_s\tau_m}}{j2\pi n}+\frac{1+e^{j(\omega-n\omega_s)(T_s/2-\tau_m)-jn\omega_s\tau_m}}{2\pi\dfrac{\omega_{rc,D}}{\omega_s}}G_D(j\omega)\right)$$

$$G_D(j\omega)=-\frac{e^{j(\omega-n\omega_s)\tau_m}-e^{-\omega_{rc,D}\tau_m}}{e^{j\pi(\omega-n\omega_s)/\omega_s}+e^{-\omega_{rc,D}.\tau_m}}\cdot\frac{1}{1+j(\omega-n\omega_S)/\omega_{rc,D}}$$

(7)

In which $\omega_{rc,D}=1/(\pi(R_S+R_L)C)$. Please note that $\omega_{rc,D}$ for the differential circuit is twice as its counterpart for the SE circuit ($\omega_{rc,SE}$) and this is due to the fact that the effective resistance seen by the capacitors in each period is halved for the differential circuit. Similar to the single ended version $H_0(j\omega)$ for an ideal differential N-path filter can be found as:

$$H_{0,D}(j\omega)=\frac{N}{1+j\dfrac{\omega}{\omega_{rc,D}}}\times\left(D+\frac{1+e^{j\omega(T_s/2-\tau)}}{2\pi\dfrac{\omega_{rc,D}}{\omega_s}}\left(-\frac{e^{j\omega\tau}-e^{-\omega_{rc,D}.\tau}}{e^{j\pi\omega/\omega_s}+e^{-\omega_{rc,D}.\tau}}\cdot\frac{1}{1+j\dfrac{\omega}{\omega_{rc,D}}}\right)\right)+(1-ND)$$

(8)

Comparing the frequency transfers in (6) and (8) for the single-ended and the differential circuits, the most noticeable difference is in the denominator which demonstrates a repetitive

pattern for the frequency poles of the transfers. From (6) and (8) the poles of $H_{0,SE}(f)$ and $H_{0,D}(f)$ for the single-ended and the differential circuits are $s_{SE}=-D\omega_{rc,SE}+jk\omega_s$ and $s_D=-2D\omega_{rc,D}+j(2k+1)\omega_s$ respectively, where k=0, ±1, ±2, …. For k=0 we get the poles around ω_S. When comparing the location of the frequency poles for the single-ended and the differential circuit, it is clear that the differential topology does not have poles at the even harmonics of the switching frequency. This is indeed consistent with the fact that in the differential architecture there is no frequency selectivity around the even harmonics of the switching frequency, unlike the single-ended case.

Fig. 6 shows the transfer curves of a single-ended and differential 8-paths filters with C=7pF and R_S=R_L=50Ω applying equations (3), (6) and (8). These values are applied in the real implementation which is discussed in section V. The theoretical curves fall exactly on top of the simulation results carried out with pss-pac in Spectre-RF with ideal capacitors and switches. By assuming $\omega_s >> \omega_{rc}$ the RC time constant becomes much larger than the "ON" times of the switches. As a result the interaction between these poles becomes negligible and as discussed in section III-D, the switched-capacitor network in Fig. 3d/e can be modeled as a RLC tank resonator around the switching frequency.

D. RLC MODEL for Single-Ended Notch Filter

As we showed for the N-path differential bandpass filter in [6] the switched capacitor part can be modeled as a parallel tank circuit for the frequencies close to the switching frequency. Here we provide the RLC model in general and simplified form for the single-ended and differential notch filter. Parallel tank model circuits are shown in Fig. 7 for the N-path notch filters. To find the parallel resistance R_P we approximate $H_{0,SE}(j\omega)$ and $H_{0,D}(j\omega)$ in (6) and (8) for $\omega_s >> \omega_{rc}$ $\omega \approx n\omega_s$ for all values of n, resulting in:

$$H_0(n\omega_s) \approx \frac{2N(1-\cos(2\pi nD)}{4D(n\pi)^2} + (1-ND) \qquad 0 < D \le 1/N \tag{9}$$

Equation (9) is the same for both the differential and the single-ended circuits with only one difference that for the differential circuit it is valid only for odd values of "n".

From (9) the impedance of the switched-capacitor part around the harmonics of the switching frequency can be found as $Z_{SE}(jn\omega_s) = H_{0,SE}(j\omega_s)(R_S+R_L)/(1-H_{0,SE}(j\omega_s))$. $Z_D(jn\omega_s)$ can be find similarly. Interestingly the impedance becomes purly resistive around

the harmonics of the switching frequency. Please note that for the differential architecture this is true just for the odd harmonics of ω_S.

Finally putting the poles around the switching frequency which are calculated in previous section, equal to the poles of a parallel tank circuit we can find the following model parameters:

$$R_P = \frac{N\sin^2(\pi D) + D\pi^2(1-ND)}{N((D\pi)^2 - \sin^2(\pi D))} R_T = \frac{N^2\sin^2(\pi/N)}{\pi^2 - N^2\sin^2(\pi/N)} R_T\,|_{D=1/N}$$

$$C_P = \frac{ND\pi^2}{m(N\sin^2(\pi D) + D\pi^2(1-ND))} C = \frac{\pi^2}{mN\sin^2(\pi/N)} C\,|_{D=1/N}$$

$$L_P = \frac{1}{(2\pi f_S)^2 C_P}$$

(10)

Where m=2 for the single ended circuit and m=8 for the differential network; moreover, $R_T = R_S + R_L$. Please note that R_P in (10) corresponds to "Z_{sh}" as derived in a different approach in [13, 14]. In (10) R_P and C_P are not frequency dependent which illustrates the fact that the bandwidth of the notch filter is not dependent to the switching frequency and is fixed while the inductor L_P is changing with the switching frequency, determining the center frequency of the notch filter. In (10) the presence of "m" states that in the RLC model for the differential circuit the capacitance will be four times smaller than for the SE case, while L_P is four times larger. This means with the same source and load resistances, Q for the differential case is four times smaller and the bandwidth will be four times larger. This is also intuitive since firstly for the differential circuit there are two series capacitors in each path and secondly each capacitor is exposed to the source and load resistors twice in each period which makes the effective resistance seen by the capacitors half compared to the single-ended version.

By applying the RLC model the main filter characteristics can be readily determined. As an example for an 8-path single-ended notch filter with N=8, $R_L = R_S = 50\Omega$ and C=7pF we find:

$$R_P \approx 19(R_L + R_S) = 1.9k\Omega$$
$$C_P \approx 4.2C = 29.4pF$$
$$Notch\_Depth = 20\log(1 + R_P/(R_L + R_S)) = 26dB$$
$$BW_{3dB} = \sqrt{(1 + R_P/(R_L + R_S))^2 - 2}/(2\pi R_P C_P) = 57MHz \quad (11)$$

According to (11) notch depth is determined by the number of the paths which theoretically is limited to 26dB for N=8. Increasing the number of paths will increase the depth of the notch.

IV. NON-IDEALITIES

A. *Switch Resistance and Clock Rise and Fall Times*

Switch resistance can readily be modeled in the RLC tank circuit as illustrated in Fig. 8 with R_{SW}. Moreover, the effect of rise and fall times can be approximated as a reduced duty cycle in (3) and (4). For the frequencies close to the switching frequency, the effect of the duty cycle is already modeled in (9) and (10). The effect of reducing the duty cycle on the pass band can be extracted from (7) and (8), noting that the term (1-ND) becomes dominant in the pass band. To include the effects of the switch resistance and reduced duty cycle we modify the model as shown in Fig. 8, where $R_D = (1-ND)(R_L + R_S + R_{SW})/(ND)$. Then the tank circuit should also be modified based on (10), substituting the actual D<(1/N) and $R_T = R_L + R_S + R_{SW}$. Consequently R_P will be increased. Meanwhile changes of C_P and L_P are rather small. The consequence of extra resistance is increased insertion loss in the pass band, while the depth of the notch filter relative to the pass-band will also be increased. The transfer function for an 8-path notch filter and RLC model is illustrated in Fig. 9 for $R_{SW} = 6\Omega$ in case the duty cycle is reduced by 15% compared to the ideal case (so 85% of 1/8). As can be seen, the insertion loss is increased by 2dB and the depth of the notch by 3dB.

B. *Harmonic Mixing*

So far the properties of the desired part in (2) which is represented as $V_{de}(j\omega)$ in (3), have been discussed. In this section we explore the unwanted terms of (2) which are represented as $V_{un}(j\omega)$ in (4). According to (4), $H_n(j\omega)$ for n=±1, ±2, …determines the possible unwanted terms. In (5) and (6) $H_{n,SE}(j\omega)$ and $H_{n,D}(j\omega)$ are non-zero for $n = kN$ where k=0, ±1, ±2, … and is zero for other values of "n". This implies that the unwanted terms will

include folding from Nf_S+1 and Nf_S-1 due to $H_{\pm N}(j\omega)$ and this will repeat for $H_{\pm 2N}(j\omega)$, $H_{\pm 3N}(j\omega)$, …

Now as an example for an 8-path single-ended notch filter, from (4), (5) we define $H_{n,un,SE}(j\omega) = (R_L/(R_L + R_S))H_{n,SE}(j\omega)$ for n=8,16,24,… $H_{n,un,D}(j\omega)$ is represented for the differential architecture in the same way. $H_{n,un,SE}(j\omega)$ and $H_{n,un,D}(j\omega)$ determine the harmonic mixing coefficients in (4). In Fig. 10 for an 8-path single-ended and differential architecture $H_{n,un,SE}(j\omega)$, $H_{n,un,D}(j\omega)$ and also $V_{de}(j\omega)/V_S(j\omega)$ are shown.

In Fig. 11 the desired term and the undesired term $H_{n,un,D}(j\omega)$ is illustrated for n=8 and for the case the physical capacitor is increased as C=5, 10, 20pF in each path. As we expect the amount of folding back components are decreased by increasing the capacitor. Accordingly similar to all N-path filters some time-invariant pre-filtering might be required in order to suppress unwanted folding terms sufficiently. Increasing the number of paths will move the aliasing components further away while increasing RC time constant also will decrease the unwanted terms which relax the requirements of the pre-filter.

C. *Noise*

If the switches in Fig. 3 and the driving clock phases are ideal, neglecting the noise of R_L then all the noise which appears at the output originates from the input resistance R_S. In the passband the transfer function for the noise of R_S which goes to the output, similar to the desired input signal, complies with (2) which includes the direct transfer and folding of uncorrelated noise power from higher harmonics. As an example two folding components that occur in an 8-path system with $H_{\pm 8}(j\omega)$ are shown in Fig. 12.

As a result the output noise can be readily calculated from (2). For an 8-path notch filter shown in Fig. 10 the folding back components are negligible and simulation and calculation from (2) renders a noise figure of NF<0.1dB for an ideal 8-path filter.

If we include the non-idealities of the switch resistance and the reduced duty cycle, NF will degrade. If the duty cycle is smaller than 1/N then the circuit behavior in the pass-band can be modeled as in Fig. 13. The tank circuit is modeled as a short circuit and the reduced duty cycle is modeled as a switch (mixer) which is on except for the clock overlap time of $PW=(1-ND)T_S$. This mixer will cause extra noise folding and also increased insertion loss in the pass-band. The noise at the output can be found by calculating the Fourier series coefficients as:

$$N_{out}=\left((\frac{R_L}{R_T}ND)^2+\sum_{n=1}^{+\infty}\left(-\frac{R_L}{R_T}\frac{2}{n\pi}\sin(n\pi(1-ND))\right)^2\right)(4kT(R_S+R_{SW}) \quad (12)$$

Where $R_T=R_L+R_S+R_{SW}$. Finally, the noise factor can be calculated as $F=N_{out}/(A_v^2N_{in})$, where $N_{in}=4kTR_S$. As an example for an 8-path single-ended notch filter if we assume $R_{SW}=5\Omega$ and 15% reduction compared to the 1/8 duty cycle, we find NF=1.7dB and an insertion loss in the pass band of 2.2dB. As a rough rule of thumb practical values of the noise figure are close to the insertion loss in dB.

D. *Mismatch and Phase Imbalance*

As discussed in section III-D an interesting property of an N-path system is that many unwanted terms in $H_n(j\omega)$ are canceled. As we derived in (5) and (6), this is due to the fact that different paths in an N-path system have equal amplitude responses but different phase shifts such that the vectorial summation is zero. In case there is any mismatch between different paths or phase imbalance in multiphase clocks, the cancellation becomes imperfect so that unwanted terms come up. We can quantify this effect with the derivations in (5) and (6). As an example we consider an 8-path single-ended system with a phase imbalance in the clock. Suppose one of the clock phases has a different duty cycle from other paths. Then as shown in Fig. 14 the first harmonic of $H_1(j\omega)$ which is cancelled in the ideal case is showing itself as an undesired term. The strength of the unwanted transfer curves are related to the amount of mismatch.

E. Parasitic capacitance

In a practical implementation the parasitic capacitance of switches and the parasitic bottom-plate capacitance of the floating capacitors in Fig. 3 can be a limiting factor at high frequencies. For instance considering the single ended notch filter and C=7pF in Fig. 3d, in case of applying MIM capacitors, which can have a typical bottom plate parasitic in the order of 5% of the total value of the capacitor, the total parasitic capacitance for 8 floating capacitors will be $C_P=8\times 7pF\times 0.05=2.8pF$. Considering a source and load resistance of 50Ω, this can produce a pole at $f_{LP}=2/(2\pi R_SC_P)\approx 2.3G$, where 3dB loss would occur

The bottom plate parasitic for CMOS capacitors might be in the order of 20% which for C=7pF of floating capacitors generates a pole at 568MHz. So in general, parasitic capacitors to ground can introduce passband insertion loss which should be minimized.

F. Cock Phase Noise Effect

The impact of phase noise of the switching clock can be understood intuitively by assuming that a blocker exists close to the switching frequency. Considering the reciprocal mixing as discussed for bandpass N-path filters in [9], the blocker can be down-mixed and up-mixed with the main clock, but also with phase noise components on the clock. As a result a blocker close to the switching frequency will show up as folded components around the switching frequency and consequently degrade the noise figure of the notch filter close to the notch frequency. This might limit the applicable passband close to the notch frequency. Although; as it is discussed in section VI, the applicable offset frequency is also determined by the input power matching. If the blocker resides in the passband of the filter, the notch filter more or less act as a short circuit, and the effect of phase noise becomes insignificant.

V. IMPLEMENTATION

Both a prototype of the SE and differential notch filter were implemented in a 65nm CMOS technology. The schematic is shown in Fig. 15 and a chip photo in Fig. 16. The switches are realized by low threshold NMOS transistors and the capacitors with MIM technology. Large switch sizes (W/L=100u/65nm) are used resulting in a switch resistance of 6Ω when driven by a swing of 0.9V (the DC voltage on the source/drains of the switches is set to 300mV to avoid reliability issues at high input swings).

The linearity of the N-path notch filters is mainly determined by the linearity of the NMOS switches and the capacitors. Apart from reducing the switch resistance, applying a large switch size will improve the linearity of the filter as well. Moreover, MIM capacitors have better linearity compared to CMOS capacitors with a comparable capacitance density. Thus a very high linearity for the N-path notch filters is achievable in the new CMOS technologies. Larger switches would increase the insertion loss at high frequencies due to the parasitic capacitance at the RF-nodes and would require higher digital drive power. In the SE filter C=7pF is chosen in each path targeting to suppress a blocker with 6MHz bandwidth (e.g. a strong TV channel which blocks a Cognitive Radio receiver exploiting TV white spaces as allowed by the FCC [16]). For the differential architecture 32 NMOS transistors are realizing

the left and right mixers in Fig. 15. Two capacitors are in series and in order to get the same RC product as the SE version we have doubled the capacitor value (C=14pF). Please note that for the differential architecture in the measurement setup the (differential) source and load resistors are 100Ω while it is 50Ω in the SE notch filter. As a result the factor of four in the Q reduction in compare with the single-ended filter as we discussed in section III-B is compensated by doubling the capacitor size and source and load resistors for the differential architecture.

As shown in Fig. 16 both the input and the output switches for the differential architecture are placed in one side of the capacitors to facilitate the routing of the 8-phase clock to 32 switches in the layout avoiding resistive and capacitive mismatch. Moreover in order to provide enough isolation between switches, they are realized inside separate deep N-wells.

For each filter, a divide-by-8 ring counter is implemented to provide a proper phase balance. The divider is composed of 8 transmission gate flip-flops in a ring (see Fig. 17 and 18). During startup the output of the first flip-flop is set to VDD and the outputs of the other flip-flops are set to ground. Then a clock activates the ring divider and at the output of the 8 flip-flops multiphase clocks with 1/8 duty cycle and with the frequency of 1/8 of the clock frequency are generated. This architecture inherently has a good phase performance since just the rising edge of the clock is used. Moreover different phases are directly generated in the ring without applying any extra logic circuits which might add errors to the multiphase clocks. The input frequency range of the clock divider is 0.8-9.6GHz. The generated phases in the divider are buffered and fed to the switches.

VI. Measurement Results and Comparison

Measurement results of the main characteristics of the SE and the differential notch filters are shown in Fig. 19 and 20 respectively for f_S at 500MHz. The maximum depth of the notch filters is limited to 24dB for $f_S = 500MHz$ while it is reduced to 21dB as the switching frequency increased. Remember the theoretical value of the maximum rejection for an ideal 8-path filter as calculated in section III is 26dB. The deviation between the measured and calculated rejection at f_S is due to the charge injection in the switches and small charge sharing between different capacitors at high frequencies. S_{21} renders 1.4-2.5dB insertion loss in the pass-band in the SE filter. The amount of insertion loss for the differential filter is 1.4-2.8dB in the pass-band. At $f_S = 500MHz$ according to the simulation results, the rise and fall

times of the clock phases driving the switches are approximately 18ps which presents approximately 15% of the pulse width ($T_S/8 = 250ps$). As we showed through an example in section IV-A and in Fig. 9 with 15% reduction in the duty cycle and the on resistance of 6Ω for NMOS switches, in the RLC model the insertion loss is 2dB. Please note 15% of duty cycle reduction in this case is quite pessimistic since the NMOS switches even during the rise and fall times are conducting. By increasing the switching frequency the rise and fall times of the multiphase clocks consist a significant portion of the pulse width which result in reduced the effective duty cycle and consequently increased insertion loss.

Power matching is provided in the pass-band for both filters. As expected the incident signal is reflected at the switching frequency and passes through for other bands except the harmonics of the switching frequency. The corner frequencies for S_{11}<-10dB are also shown in Fig. 19 and 20.

The measured IIP3 is better than +17dBm and P_{1dB} is between 2-6dBm. P_{1dB} in the pass-band is measured as -3dBm when a blocker with a power of 0dBm is applied at f_S . The NF, measured in the pass-band is 1.2-2.8 for the SE and 1.6-2.5dB for the differential filter for the switching frequencies of 0.1-1.2GHz which is roughly the same as the loss in dB. NF increases at the notch frequency due to the fact that the signal is attenuated around the switching frequency, while the noise from the switch resistance and also folded back noise from higher harmonics still can appear at the output.

For the differential filter as we expect there is no rejection at the second harmonic. The increased noise figure around the second harmonic in this case is due to the leakage of the second harmonic of the clock. The tunability of the filter is illustrated in Fig. 21, showing S_{21} of the SE filter for $f_S = 0.1 - 1.2GHz$. The differential filter shows the same behavior.

The group delay of the SE filter is measured and shown in Fig. 22 and compared to the prediction by the RLC model in Fig. 8. Similar to a passive tank circuit the group delay becomes flat in the pass-band representing a linear phase operation. In order to check the effect of the phase imbalance and mismatch on the performance of the filter we have measured the harmonic mixing effect in 10 samples for 3 switching frequencies in the SE and differential notch filters. Fig. 23 illustrates the worst-case numbers of harmonic mixing in the pass-band.

We also tried to measure the noise figure in the pass-band, under blocking conditions. In simulation we found that by applying a blocker of -5dBm at f_S , the NF in the pass-band

degrades by 1dB . Due to the noise floor of our signal generator we didn't manage to measure this directly.

The maximum rejection of the filters is measured with the existence of a blocker at the notch frequency (see Fig. 24). The amount of rejection is degraded by increasing the blocker power, but this only happens at high blocker power levels. Interesting difference are observed here between the SE and differential filter. The SE filter input port might be chosen at the capacitor side (left in Fig. 15), but also at the switching side (right side). As it is shown in Fig. 24 choosing the switching side as the input port is better in terms of notch depth under strong blocking conditions (the rejection degrades starting at -3dBm versus -8dBm). The reason for the degradation of the notch depth is charge leakage from the capacitors with the existence of the large input power. Note that the DC level on the drain/source of the switches is 300mV. If the input swing is larger than 300mV then the voltage on the source/drain of the switches might become negative and as a result some of switches which are supposed to be off with zero gate voltage, start to conduct and unwanted charge leakage happens which reduces the amount of the maximum rejection at notch frequency.

Now assume that in the SE filter we apply a sinusoidal signal with the frequency of the switching frequency to the capacitor side. The voltages over the capacitors will have a constant value. This voltage is in fact the average of the portion of the signal which is seen by each capacitor periodically. As a result the voltage on the drain/source of the switches will be the input signal with a shifted DC level which can be negative also for the negative parts of the input signal. Then the voltage on the source/drain of the switches might be even more negative which results in severe charge leakage compared to the case of choosing the switching side as the input.

Although the differential filter is reciprocal for small signals, this may change at large signals. Unlike the input set of switches, the set of the switches at the output will not experience a large swing with the existence of a large blocker at the input. As a result the charge leakage from the capacitors will be limited and consequently the blocker performance of the differential notch filter is significantly better than the single-ended version.

The measured clock leakage at the input port for the SE and the differential filter is better than -75dBm and -60dBm respectively at the switching frequency. These values are lower than -57dBm spurious domain emission limit for frequencies lower than 1GHz, as specified by FCC part 15 [23]. The larger LO leakage in the differential architecture is mainly due to the larger overlap between input/output lines and the clock lines in the layout for the differential filter.

To put these results in perspective, the key measured parameters of both filters are compared with results of two Q-enhanced notch filters [24, 25]. Compared to the Q-enhancement techniques a much larger tuning range with higher dynamic range is achievable with the N-path technique. Also, Q-enhanced notch filters cannot handle large blockers: the maximum rejection of 44dB reduces to 3dB with a blocker level of -5dBm while the implemented 8-path notch filters still provide their default 24dB of rejection with the existence of -5dBm blocker level. The center frequency is determined with the clock frequency which is very robust while in the LC resonator based architectures the sensitivity of the center frequency to PVT variations is significant. Moreover the die area is much smaller, especially at low GHz bands.

VII. CONCLUSIONS

Widely tunable filters with good linearity and blocking performance are very much wanted to address blocking issues in both multi-mode wireless transceiver systems co-existing on a single chip as well as software defined and cognitive radio systems. In this context N-path filtering seems quite promising, as it provides digital programmability of the center frequency via a digital clock frequency with a small sensitivity to the PVT variations, offers good linearity and compression performance by using passive mixers with capacitors driven by digital clock, which all fit nicely to CMOS technology scaling. This paper discusses N-path notch filter circuits and models their performance, quantifying both transfer properties and several important non-idealities. The filter performance is verified for both a single ended and differential notch filter in 65nm CMOS, digitally tunable over more than a decade from 100MHz-1.2GHz. Measured filter transfer and noise properties fit well to theory, showing 1.2-2.8 conversion loss in the pass-band, and a rejection in the notch which is always >18dB over 6MHz bandwidth over the entire tuning range. Unwanted folding is present, but up to the 8^{th} harmonic, rejection is better than -50dBc. Linearity is consistently high (IIP3>17dBm) and compression points well above 0dBm are achievable. Compared to Q-enhanced LC filters with similar Q-value, the filter maintains shape up to much higher blocking levels.

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Figure and Table Captions

Fig.1. Coexistence problem in (a) Multi-standard system (b) A frequency division duplexing (FDD) system.

Fig.2. (a) LC Q-enhanced notch filter [1] (b) Frequency translated notch filter [2]

Fig.3. (a) Up-converted high-pass filter represents a notch filter at LO. (b) Single-ended (SE) N-path notch filter. (c) Multiphase clock which drives the switches in the N-path filter. (d) Simplified SE N-path filter. (e) Differential N-path filter.

Fig.4. A typical timing diagram of the input-output voltages in an 8-path notch filter with a sine wave input signal with a frequency equal to the clock frequency of the switches.

Fig.5. Time intervals for the state space analysis.

Fig.6. The Single-ended and differential 8-path notch filter transfer function for C=7pF and $R_S=R_L=50\Omega$

Fig. 7. RLC model of the ideal single-ended and differential N-path notch filters for the frequencies close to the switching frequency.

Fig. 8. RLC model of the N-path notch filter including the effect of the switch resistance and the clock duty cycle.

Fig. 9. RLC model transfer function versus the N-path notch filter.

Fig. 10. Desired (de) and unwanted folding back transfers Q_n for n=8,16,24 in (a) a single-ended 8-path notch filter (b) a differential 8-path notch filter.

Fig. 11. The effect of increasing "C" on the desired and undesired transfers of an N-path notch filter.

Fig. 12. Noise folding in an 8-path notch filter.

Fig. 13. Modeling of clock rise/fall times as a mixer.

Fig. 14. The effect of phase imbalance on the N-path notch filter desired and undesired transfers.

Fig. 15. An 8-path single ended and a differential notch filters.

Fig. 16. Chip micrograph in 65nm CMOS technology.

Fig. 17. A divide by 8 ring counter.

Fig. 18. Transmission gate D flip-flop used in the ring counter.

Fig. 19. S_{21}, S_{11}, NF, P_{1dB} and IIP3 of the single-ended notch filter.

Fig. 20. . S_{21}, S_{11}, NF, P_{1dB} and IIP3 of the differential notch filter.

Fig. 21. S_{21} in the single-ended filter for the switching frequency of f_s=0.1-1.2GHz.

Fig. 22. Measured group delay of the single-ended notch filter compared with the RLC model at f_s=500MHz.

Fig. 23. Measured harmonic mixing of 10 samples for (a) single-ended (b) differential notch filters.

Fig. 24. Measured maximum rejection of notch filters with a blocker at notch frequency: Case 1- The differential notch filter. Case 2-The single-ended notch filter when the input is the switching side of the filter. Case 3- The single-ended notch filter when the input is the capacitor side of the filter.

TABLE I COMPARISON WITH OTHER DESIGNS

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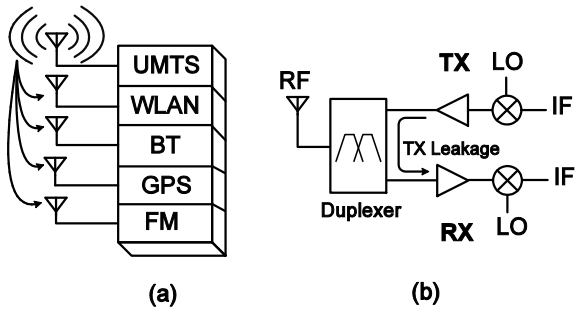

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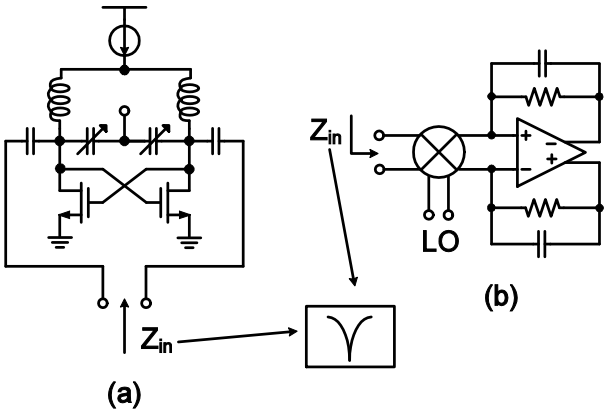

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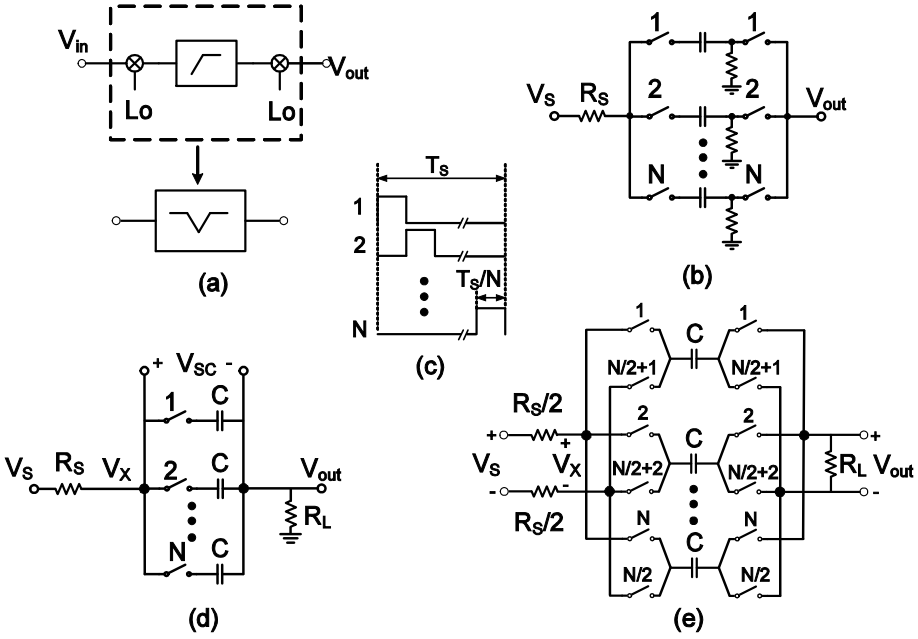

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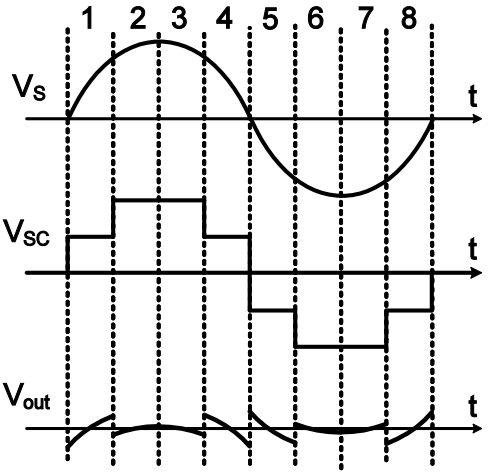

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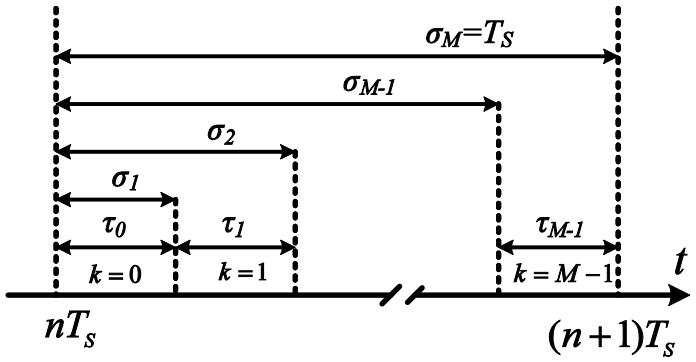

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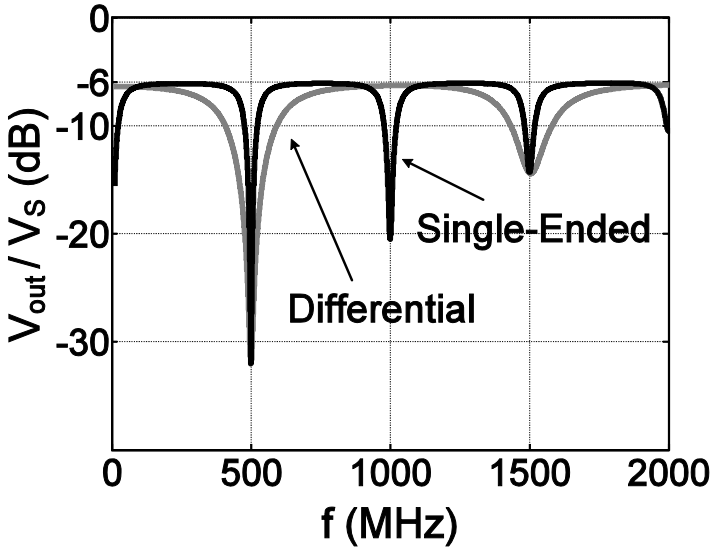

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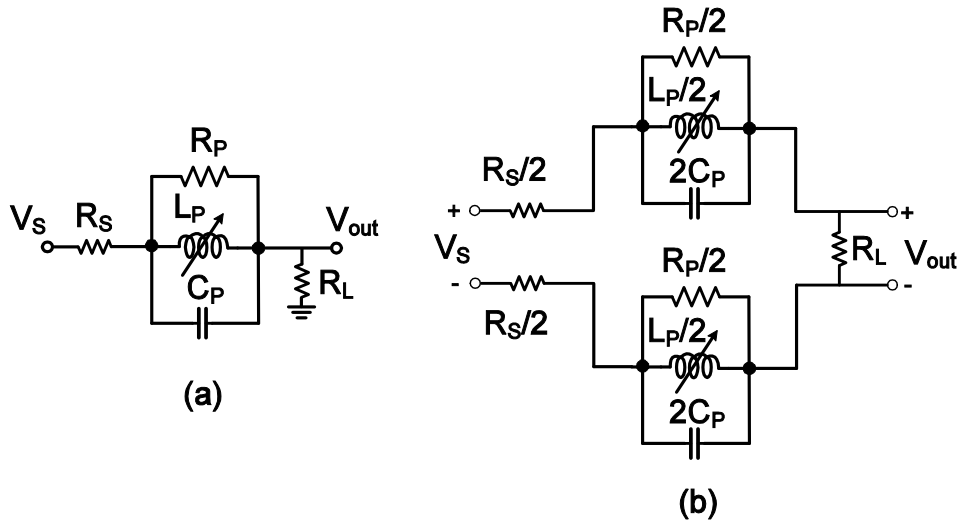

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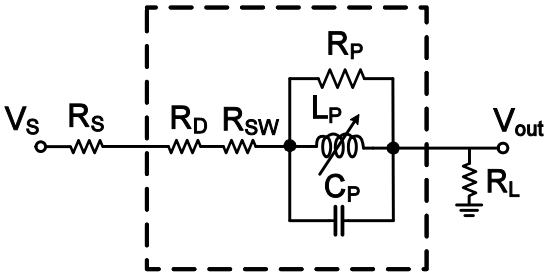

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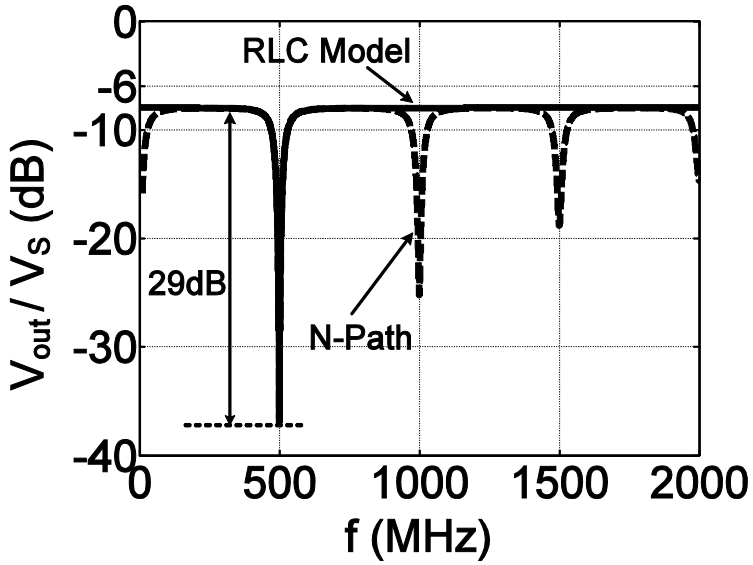

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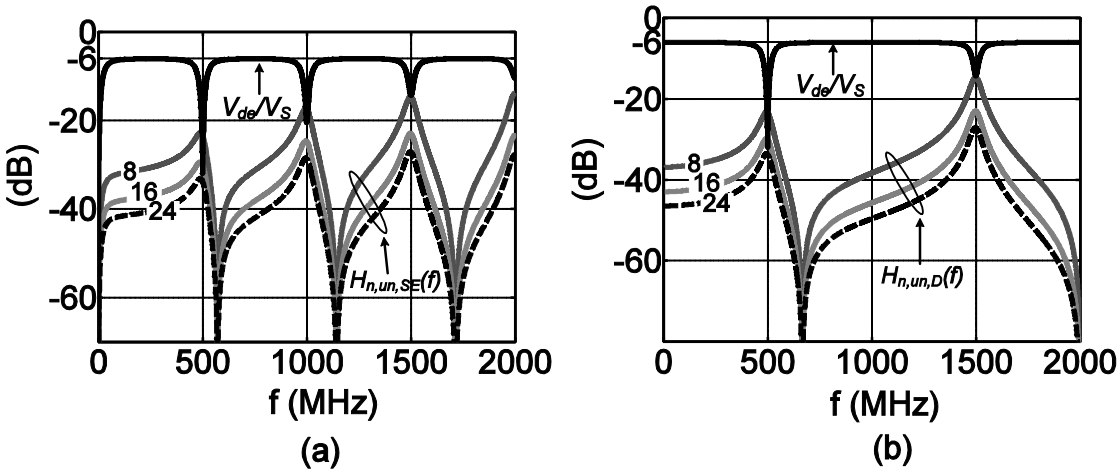

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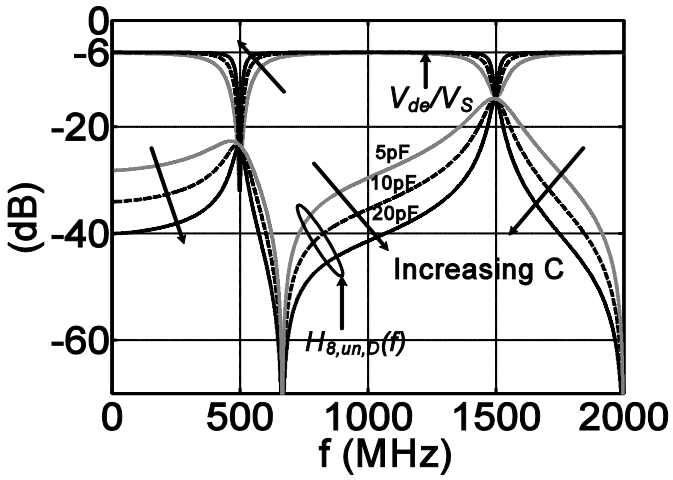

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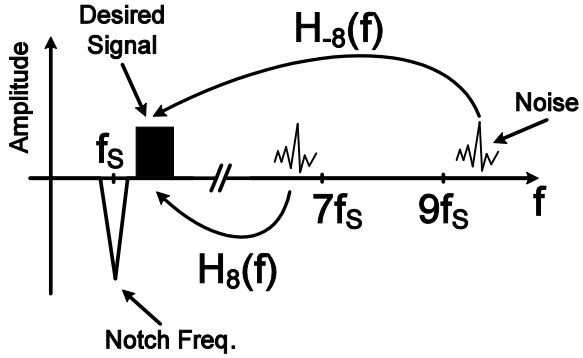

Fig. 12. Noise folding in an 8-path notch filter.

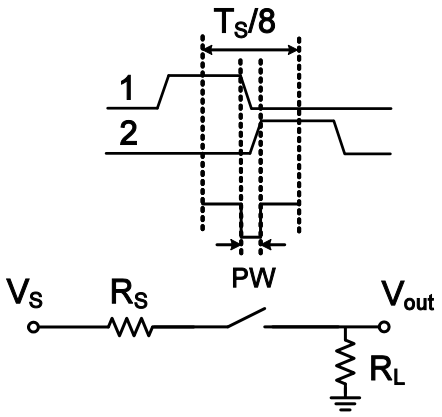

Fig. 13. Modeling of clock rise/fall times as a mixer.

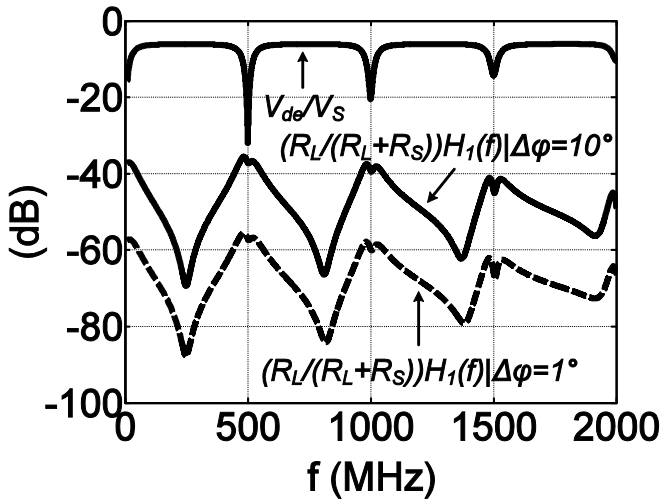

Fig. 14. The effect of phase imbalance on the N-path notch filter desired and undesired transfers.

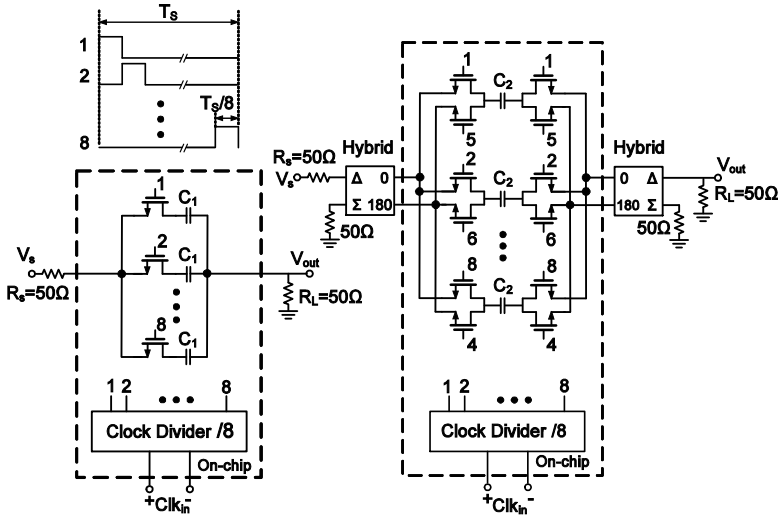

Fig. 15. An 8-path single ended and a differential notch filters.

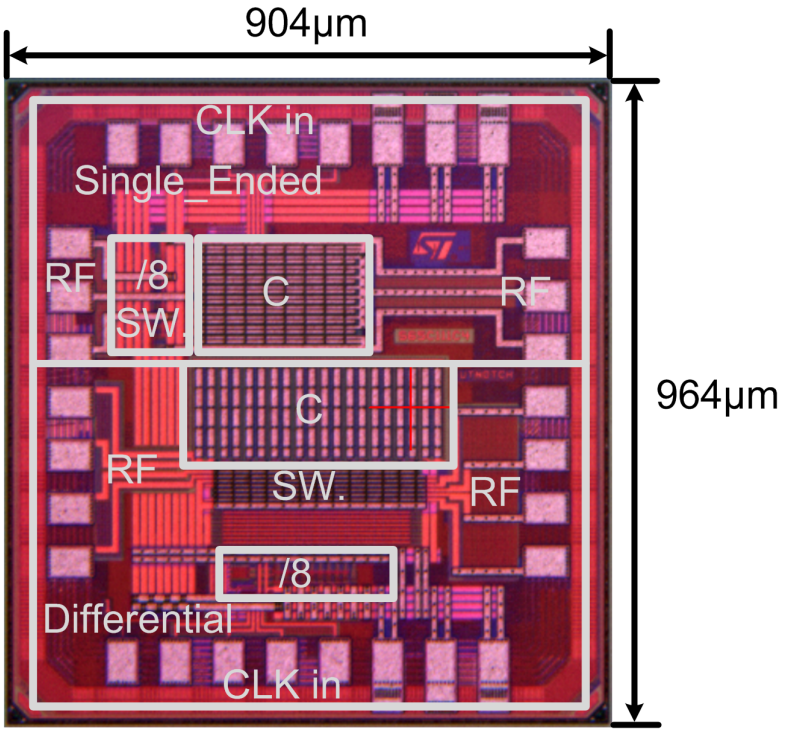

Fig. 16. Chip micrograph in 65nm CMOS technology.

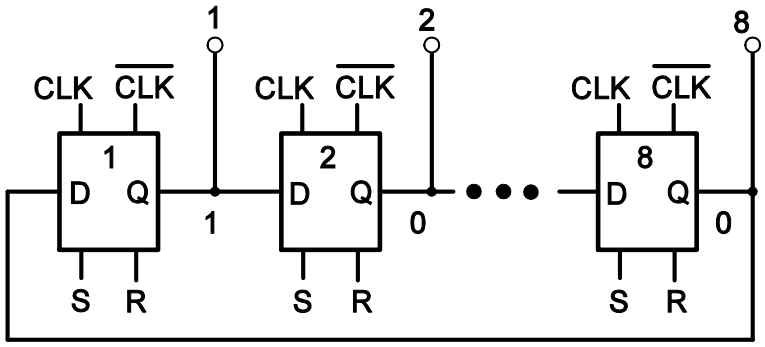

Fig. 17. A divide by 8 ring counter.

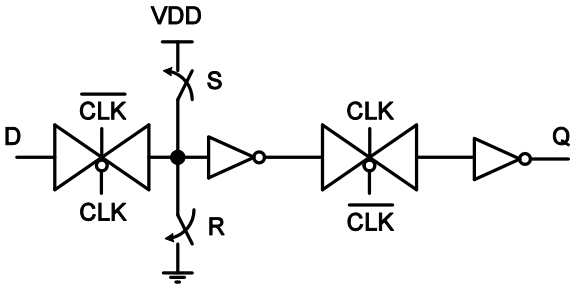

Fig. 18. Transmission gate D flip-flop used in the ring counter.

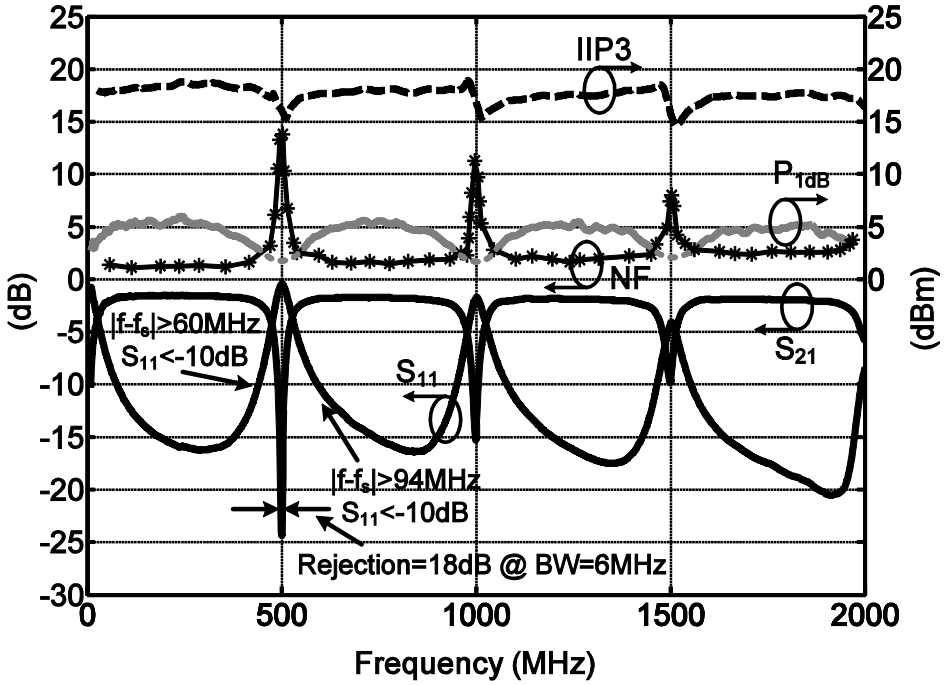

Fig. 19. S_{21}, S_{11}, NF, P_{1dB} and IIP3 of the single-ended notch filter.

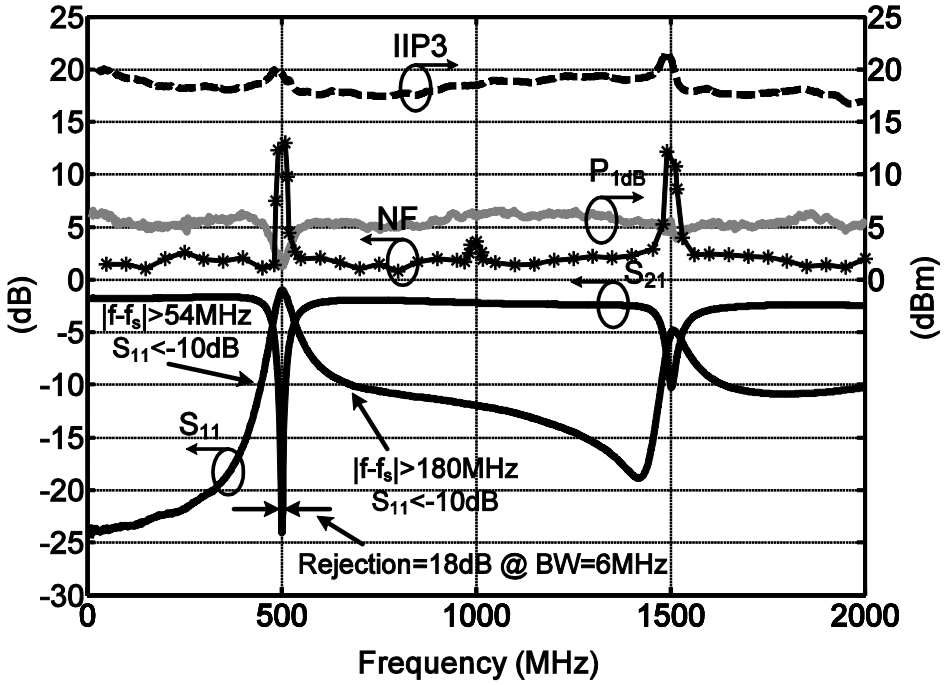

Fig. 20. . S_{21}, S_{11}, NF, P_{1dB} and IIP3 of the differential notch filter.

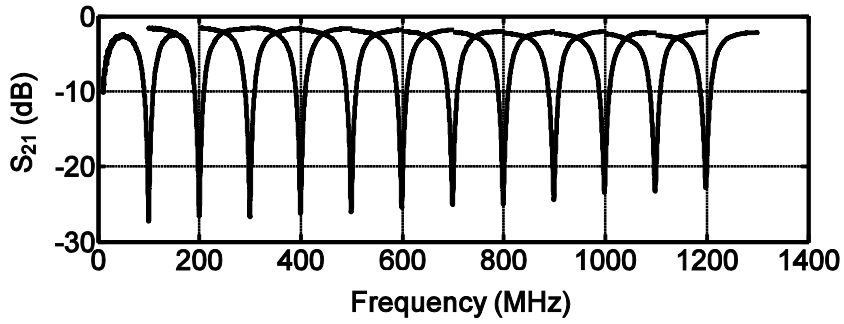

Fig. 21. S_{21} in the single-ended filter for the switching frequency of f_s=0.1-1.2GHz.

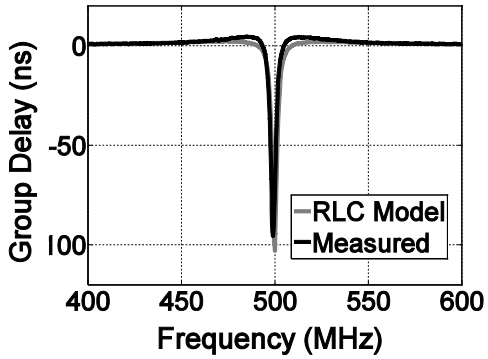

Fig. 22. Measured group delay of the single-ended notch filter compared with the RLC model at f_s=500MHz.

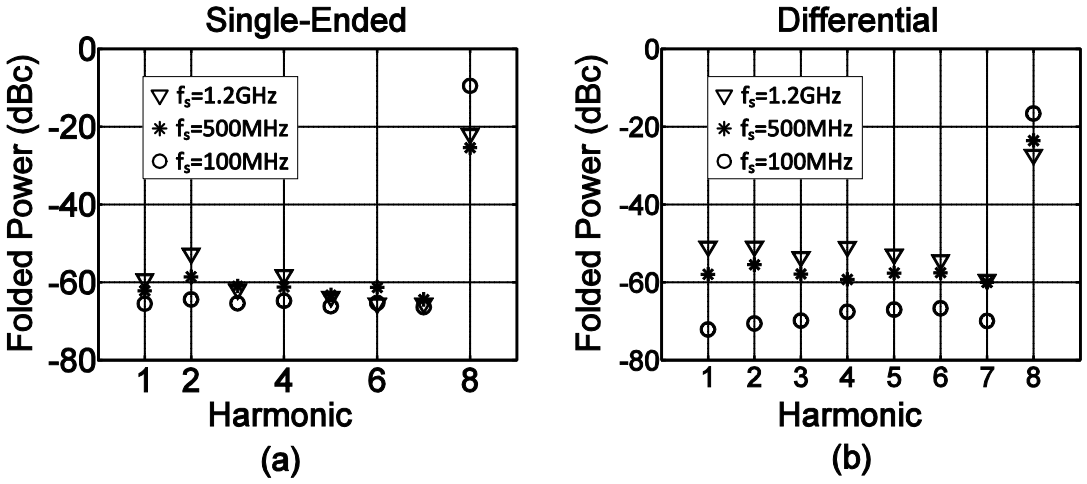

Fig. 23. Measured harmonic mixing of 10 samples for (a) single-ended (b) differential notch filters.

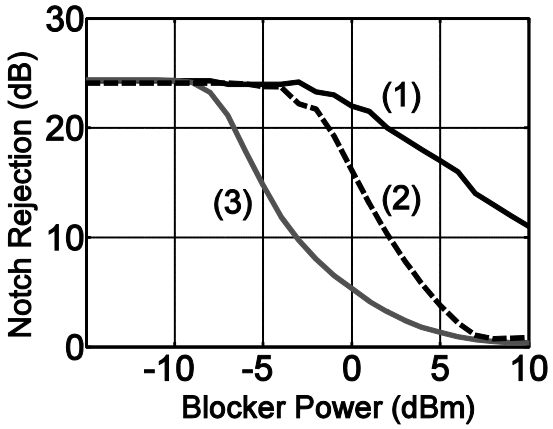

Fig. 24. Measured maximum rejection of notch filters with a blocker at notch frequency: Case 1- The differential notch filter. Case 2-The single-ended notch filter when the input is the switching side of the filter. Case 3- The single-ended notch filter when the input is the capacitor side of the filter.

TABLE I

COMPARISON WITH OTHER DESIGNS

	Differential	Single-Ended	[24]	[25]
Technology	CMOS 65nm	CMOS 65nm	CMOS 0.13um	CMOS 0.18um
Active Area	$0.14mm^2/0.87mm^2$	$0.07mm^2/0.87mm^2$	$1.6mm^{2(1)}$	$0.51mm^{2(1)}$
Tuning Range	100MHz-1.2GHz	100MHz-1.2GHz	4.7-5.4GHz	5.4-6GHz
Max. Rejection	21-24dB	21-24dB	44dB	35.7dB
Max. Rejection with -5dBm Blocker @ Notch Freq.	24dB @ f_S=500MHz	24dB @ f_S=500MHz	3dB	NA
Rejection	18dB @ 6MHz	18dB @ 6MHz	10dB @ 20MHz	NA
Pass-Band Gain	-1.4dB to -2.8dB	-1.4 to -2.5dB	$19.4dB^{(1)}$	$14.7dB^{(1)}$
NF (dB)	1.6dB-2.5dB	1.2-2.8dB	$3.5dB^{(1)}$	$5.3dB^{(1)}$
P_{1dB} (dBm)	6	2-6	$-9.4^{(1)}$	NA
IIP3 (dBm)	>17	>18	$-2.9^{(1)}$	$-2.5^{(1)}$
LO Leakage (dBm)	<-60	<-75	-	-
Power Consumption	3.5mW-30mW @ (100MHz-1.2GHz)	2mW-16mW @ (100MHz-1.2GHz)	7.5mW	1.8mW

A notch filter with an LNA are included in the reported numbers.