Analog IC Design at the University of Twente

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Introduction

This article describes some recent research results from the IC Design group of the University of Twente, Located in Enschede, The Netherlands.

Our research focuses on *analog* CMOS circuit design with emphasis on high frequency and broadband circuits. With the trend of system integration in mind, we try to develop new circuit techniques that enable the next steps in system integration in nanometer CMOS technology. Our research funding comes from industry, as well as from governmental organizations. We aim to find fundamental solutions for practical problems of integrated circuits realized in industrial Silicon technologies.

CMOS IC technology is dictated by optimal cost and performance of digital circuits and is certainly not optimized for nice analog behavior. As analog designers, we do not have the illusion to be able to change the CMOS technology, so we have to "live with it" and solve the problems by design. In this article several examples will be shown, where problematic analog behavior, such as noise and distortion, can be tackled with new circuit design techniques. These circuit techniques are developed in such a way that they do benefit from the modern technology and thus enable further integration. This way we can improve various analog building blocks for wireless, wire-line and optical communication. Below some examples are given.

Thermal Noise Cancelling

Noise is an important issue: in communication circuits the sensitivity of the receiver is limited by the noise level of the circuits. Especially the noise of the first amplifier in the receiving chain is of high importance, since after that amplifier the signal is stronger and the allowable noise levels are higher. For narrowband receivers the added noise of the amplifier can be reduced relatively easily. This is done by using resonant structures, built with - for example - integrated spiral inductors and capacitors which provide voltage gain of the narrowband signals and therefore needing less gain from "noisy" transistors. For wideband systems, e.g. for TV tuners, UWB (Ultra Wide

Band) communication and future software defined radio, several octaves of bandwidth are needed and simple resonant structures cannot be used. For these applications, low noise gain stages using noisy transistors have to be used which is quite a challenge. Apart from the gain and noise demands, additional demands such as input impedance matching and good linearity need to be satisfied.

Figure 1a shows a wide band first amplifier stage, denoted as a common-source feedback amplifier. The input impedance is $1/g_m$ of M1, and must be equal to the source impedance R_s , usually 50 Ohms. With this in mind the g_m of M1 is fixed by design resulting in poor noise behavior of the amplifier: The "noise figure" is always larger than 3dB. In order to reduce the noise one would like to increase the g_m of M1 (preferably $g_m \gg 1/R_s$ for minimal noise figure) but then the input impedance does not match anymore. Conventionally, additional feedback techniques are used to break this paradox, but at the cost of stability and bandwidth issues.

PhD Student Federico Bruccoleri realized, however, that generated noise can be cancelled by proper circuit design. If we take a look at Fig. 1b, we can see how the noise current of M1 flows in the circuit; this is indicated by the red arrow. The noise current due to M1 flows in a loop, through R_s . This noise current generates a noise voltage at nodes X and Y which are of different magnitude but of *the same phase*. The signals nodes X and Y are in anti-phase due to the inverting nature of this amplifier. So somehow it should be possible to separate the signal from the noise!

By adding an additional amplifier "A" we can construct an output signal in such a way the wanted signals at nodes X and Y are added and that the noise at nodes X and Y are cancelled [1]. This way we can cancel the noise of M1; which holds for both thermal and 1/f noise. Of course amplifier "A" will now add additional noise, but this needs not to be a problem. The reason for this is that in contrast to M1, we can choose the g_m of the input stage of amplifier "A" relatively large, and thus make it low-noise. So we don't break the laws of physics: we still have to burn power (in amplifier "A") to get a low-noise amplifier, but we have created a degree of freedom by decoupling the input matching ($g_{m1}=1/R_s$) and allowing a large g_m ($g_{mA} \gg 1/R_s$) in the amplifier A. The noise of I_{bias} is cancelled as well. A prototype amplifier has been realized on silicon and it worked well: the noise figure was well below 3dB, which proves the concept of noise canceling. Also the robustness to mismatch in the two noise paths is good. [1]. Other topologies are also possible offering "balun" functionality [1,2]

Low Frequency noise reduction in MOSFETS

Low frequency (LF) transistor noise, also denoted as $1/f$ noise, is of great importance in today's circuit design. Especially baseband circuits suffer from this noise phenomenon which can be dominant well above 10MHz. Also high-frequency oscillators suffer from LF noise, since this noise is up-converted and appears close to the carrier frequency of the oscillator degrading the close-in phase noise.

A while ago an MSc student Gian Hoogzaad did calculations on the phase noise of CMOS inverter-based ring oscillators. These oscillators were free running, and we expected a large close-in phase noise due to the low frequency noise of the MOSFETs in the oscillator. Measurements, however, showed a much lower, 8dB less, close-in phase noise than we expected from the LF noise of those single transistors. The student and his supervisor Sander Gierkink were very confident of his calculations, and we were thus wondering what caused the 8dB lower close-in phase noise.

Finally, we suspected that the large signal switching behavior in the inverters caused the strange effect and we carried out measurements on stand-alone transistors under normal bias and under "switched bias". Figure 2a illustrates these conditions. One would expect 6 dB less noise from the switched bias transistors compared to the normal one: 3dB reduction due to the 50% duty-cycle of the noise and another 3dB due to up-conversion of the LF noise. Measurements however showed $6 + 8 = 14$ dB reduction for frequencies lower than the switching frequency, as illustrated with the red curve in Fig. 2b. This matched to the 8dB reduction of phase noise in the inverter ring-oscillator. This reduction takes place for frequencies lower than the switching frequency. Later, we discovered that a similar noise phenomenon had been observed before in physicists' device experiments; [3] however we could not find a citation to this paper.

So, in fact, all inverter based ring oscillators benefited already from this phenomenon while none of the designers apparently realized this. To a large extent this is because the "switched bias" noise reduction is not modeled in today's simulators. Also, the effect can be masked by the very large spread which is normally present in LF noise, especially for small area devices. After a study carried out in the PhD projects by Arnoud van der Wel and Jay Kolhatkar, the phenomena could be explained by the bias dependency of the emission and capture time constants which are responsible for the trapping and de-trapping of oxide-charge in MOSFETs. This trapping and de-trapping causes so-called random telegraph signals, which determine the low frequency noise of the transistors. The reduction effect is found to be present in all technologies investigated: from $10\mu\text{m}$ down to $0.12\mu\text{m}$, both N and P

MOSFETs and works for switching frequencies up to at least 3GHz.

For large-geometry transistors we generally see a significant reduction, whereas for very small-sized modern devices the noise can decrease but also increase. This is due to the very small number of traps in the transistors (sometimes only one trap) while the phenomenon depends strongly on the energy distribution of the traps. Details can be found in [4].

Other known techniques to reduce the effect of LF noise in electronic circuits are chopping and correlated double sampling. The LF noise can also be reduced by increasing gate area of the MOSFETS, at the cost of area and/or power consumption. The switched bias technique offers an orthogonal method to reduce the intrinsic LF noise in the transistor itself. It is beneficial especially in circuits where switching already occurs, such as oscillators and discrete time circuits.

Distortion Cancelling using Poly-Phase Technique

In deep submicron technology, distortion becomes an increasing problem. Large signals are required for dynamic range reasons or simply because for a given radio standard dictates the output power to be delivered by a Power Amplifier. The transistors however have less voltage gain and exhibit very non-linear behavior, which makes linear circuit design a challenge.

We know that in differential circuit the even harmonics are cancelled if the signals are in anti-phase. With this in mind, MSc student Eisse Mensink investigated whether it would be possible to use more than 2 paths and multiple phases of the signal (poly-phase) and cancel more than 2 harmonics. The basic idea is shown in Fig. 3a, where the signal path is split in N separate parallel paths. $N=2$ equals the well-known differential circuit topology to cancel even harmonics. If phase shifters are available before and after the nonlinear circuit, the structure of Fig. 3a can cancel the harmonics up to $N-1$. [5] The problem is however that wide-band phase shifters are very hard to implement with analog circuits. For this reason, we choose to use mixers as second phase shifters, as shown in Fig. 3b. The mixers each have a Local Oscillator (LO) input with each a different phase, equally divided over $360/N$ degrees. Since we automatically get up-conversion of our input signal with these mixers, we strategically changed our plan and decided to build an RF power up-converter. In this up-converter the first phase shifters are assumed to be implemented in the digital baseband, while in the up-conversion mixers all problematic harmonics due to nonlinearities of the N power amplifier stages can be cancelled via the poly-phase technique in combination with a 1/3 duty-cycle LO-signal [6]

A silicon realization, designed by MSc Student Rameswor Shrestha, is based on the circuit of Fig. 3c with $N=18$ [6]. The colors in Fig. 3c correspond to the colors of the functional blocks of Fig. 3b. Rameswor demonstrated a power up-conversion mixer, which is driven in compression while all harmonics and their sidebands, up to the 17th harmonic, still remain under -40dBc. Without this poly-phase topology (i.e. for $N=1$) the harmonics would be below only -6dBc, which clearly demonstrates the effectiveness of the technique: 34 dB improvement. The RF frequency could be varied from DC to 2.5GHz and the final accuracy of the technique was limited by timing of the LO phases.

Conventional RF up-converters require expensive post-filters, dedicated for every RF frequency to filter out the harmonics and sidebands in order to satisfy the radio transmit mask. With this poly-phase up-converter the harmonics can be rejected and the filter demands can be much relaxed. Applications of this poly-phase up-converter can probably be found in wide band flexible up-converters and software radio transmitters, where the actual RF frequency is a priori not known and is free to choose in a given range.

Pulse Width Modulation Cable Equalizer

For digital data communication over copper cables, electronic equalizer circuits are used to compensate for the losses and reflections over the cables. Thanks to these electronic circuits, higher data rates can be achieved over relatively cheap cables. Examples are USB and LAN.

A well known technique used at the transmitter side is pre/de-emphasis, effectively high-pass filtering the transmitted signal. This way the low-pass characteristic of the cable is compensated for. These transmit pre-emphasis filters are generally implemented with Finite Impulse Response (FIR) filters, most often with just a few symbol spaced taps.

As an alternative to FIR filters Daniel Schinkel and Jan-Rutger Schrader proposed Pulse Width Modulation (PWM) on a digitally coded signal. [7,8]: if a '1'-bit has to be transmitted, a 1-0 pattern is transmitted in one bit time and if a '0'-bit has to be transmitted a 0-1 pattern is transmitted in one bit time. This is similar to Manchester coding but with adjustable, non-50% duty-cycle. The duty-cycle of the 1-0 and 0-1 pattern is chosen in such a way that it compensates for the cable loss. This is illustrated in Fig. 4a, where the duty-cycle of a 1-0 pattern is varied and the corresponding cable responses are plotted. Thus by changing the duty-cycle, the transmitted spectrum, in which the lower frequencies are attenuated, is tuned for the high-frequency loss of the cable. In a real application an adaptive loop with return-channel communication takes care for

this tuning, similar as in a conventional FIR approach. A test chip achieved 5Gb/s over 25m of RG-58U coaxial cable which has a loss of 33 dB at the Nyquist frequency of 2.5GHz [8] . The eye diagram for various duty-cycles is shown in figure 4b: for this 10m long cable 66% is the optimum duty-cycle. The PWM technique can compensate for higher loss compensation (33 dB in contrast to approx. 20dB for 2 tap symbol-spaced FIR) because the resulting spectrum has a better match to the skin-effect and dielectric loss of the cable. Still only one tuning "knob" is required to fit the transfer function to the cable. Moreover the technique is insensitive to slew-rate distortion and requires only two discrete amplitudes at the TX output (with a continuously adjustable duty-cycle), which makes it suitable for modern CMOS technologies. The technique was also successfully applied earlier for very long on-chip RC limited interconnects by Daniel Schinkel and Eisse Mensink [7]

Optical Detectors in Standard CMOS

Traditionally, in optical communication extremely high data rates have to be achieved over long distances. Therefore optical communication is the domain of expensive exotic technologies and the high costs associated with it can be shared between many users. For optical communication over short distances (meters) or very short distances (optical interconnect), cost issues however do play a crucial role. Therefore we started a project to integrate an optical detector in standard CMOS technology; the optical data signal can now shine directly on a digital CMOS chip. Due to the availability of low-cost high-speed laser at 850nm wavelength and the compatibility with both inexpensive plastic fibers and with photo-generation in silicon, our work mainly uses this 850nm. An essential part of an optical detector in CMOS is the integrated photodiode structure, shown in the leftmost inset in Fig. 5. Incident photons are absorbed in the silicon at tens of microns deep: much deeper than any junction in standard CMOS. In the absorption process, electrons and holes are generated and most of them slowly diffuse to the pn-junctions where the actual detection takes place. The slow diffusion causes the -3dB bandwidth of the photodiode to be in the order of 5 MHz, which causes a serious speed problem. In literature authors generally modify the technology, e.g. to allow high voltages and very wide depletion layers to boost the speed of the carriers, however this implies that non-standard CMOS has to be used. The maximal speed reported in standard CMOS so far was 700Mbit/sec. Ph.D. student Sasa Radovanovic implemented another solution. Although the -3dB frequency is very low, the roll-off per decade of frequency appears to be very low as well: only 3 to 4 dB per decade, up to in the low GHz region. Therefore Sasa used an

analog equalizer, with opposite frequency characteristic after the transimpedance amplifier following the diode to get a flat overall response up to a few GHz. One might assume that the production spread in time constants between the equalizer and the diode itself might ruin the performance, but thanks to the low roll off, even +/- 20% spread in time constants hardly affects the time pulses. The resulting chip achieved 3Gbit/sec in standard 0.18 μ m CMOS, with a BER of 10^{-11} at an optical input power of 25 μ W [9]. The speed limitation was in the electronic circuit, and is expected to scale with technology. This result enables high speed optical inputs for standard CMOS chips.

Conclusion:

Several examples of new design methodologies have been illustrated. These methodologies benefit from modern CMOS technology and may be helpful for future system integration. More work can be found at the URL: <http://icd.ewi.utwente.nl>

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FIGURE CAPTIONS

Fig 1a: common source LNA with impedance matching, the signals at nodes X and Y have opposite sign.

Fig 1b: The noise of M1 generates in-phase noise voltages at nodes X and Y.

Fig 1c: Basic idea of noise cancelling; the noise due to M1 is cancelled.

Fig. 2a: MOSFET under constant bias (blue) and switched bias (red)

Fig. 2b: Measured LF noise of a MOSFET under constant bias (blue), expected 6 dB reduction under switched bias (red dashed curve) and measured behavior with intrinsic reduced noise (red)

Fig. 3a: N path poly-phase circuit can cancel up to the $N-1^{th}$ harmonic.

Fig 3b: Wide band phase shifters can be implemented with mixers, resulting in up-converter behavior.

Fig 3c: Basic circuit of Power up-converter.

Fig. 4a: Transmitting a "1" using PWM pre-emphasis: tuning the duty-cycle of the 1-0 pattern can compensate for the cable response.

Fig 4b: 5Gb/s eye patterns of transmitted signals (TX) and received signals (RX) for duty-cycle settings of 100% (normal data) , 66% (optimal PWM) and 50% (overcompensated PWM) over 10m RG-58CU cable.

Fig 5: Optical detector in standard $0.18\mu\text{m}$ CMOS achieves 3Gb/s thanks to an analog equalizer.

Figure 1a

Figure 1b

Figure 1c

Fig 2a

Fig 2b

Fig 3a

Fig 3b

Fig 3c

Fig 4a

100% duty cycle:

66% duty cycle:

50% duty cycle:

TX:

RX:

1 bit time

Fig 4b