The Detection of Defects in a Niobium Tri-Layer Process

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Abstract—Niobium (Nb) LTS processes are emerging as the technology for future ultra high-speed systems especially in the digital domain. As the number of Josephson Junctions (JJ) per chip has recently increased to around 90,000, the quality of the process has to be assured so as to realize these complex circuits. Until now, very little or no information is available in the literature on how to achieve this. In this paper we present an approach and results of a study conducted on an RSFQ process. Measurements and SEM inspection were carried out on sample chips and a list of possible defects has been identified and described in detail. We have also developed test-structures for detection of the top-ranking defects, which will be used for yield analysis and the determination of the probability distribution of faults in the process. A test chip has been designed, based on the results of this study, and certain types of defects were introduced in the design to study the behavior of faulty junctions and interconnections.

Index Terms—Defect-based testing, PDM, RSFQ circuit testing, structural testing, superconductor devices.

I. INTRODUCTION

THE requirement for high-speed electronics in various areas like telecommunication and computing is increasing rapidly. Current semiconductor technologies will not be able to handle the future requirements in speed and accuracy. Even at this immature stage, superconductor electronics is capable of handling these tasks. Examples of these complex designs are a Superconductor ADC [1] and the Flux microprocessor chip [2].

As the complexity of the circuits is increasing to almost 100 000 JJ's per chip [2], realization of the design becomes a difficult task. Although extended research is going on in making complex circuits and scaling down the minimum sizes, very little or no information is available in literature on the methodology for achieving high yield for superconductor electronics. The yield levels are much lower than in the semiconductor industry. This is due to the fact that while much research has been carried out about the defects in semiconductor manufacturing processes [3], little information is available on superconductor processes. Special structures have been developed and realized along with the normal Integrated Circuits (IC). The information gathered using these special structures are used for yield analysis and Defect Based-Testing

(DBT) [4]. Fault models have been developed after studying the behavior of the test structures. In this way, the semiconductor industry has developed methodologies and techniques to achieve high yields.

In this paper, the structural defects that can occur in a niobium tri-layer based technology and its testing are discussed. The organization of the paper is as follows. The next section explains briefly general defects and testing strategies. In Section III, the tri-layer process is described followed by the defect analysis. Associated test structures are presented in Section IV.

II. DEFECTS AND DEFECT TESTING

The type of defects that can occur in an IC manufacturing process flow can be divided into two categories: design failures and manufacturing defects. We will only consider manufacturing defects, which can be classified into two subclasses:

- 1) Local (random) defects
- 2) Gross manufacturing defects

Defects that affect a large area, even a complete wafer, are called gross manufacturing defects. Random defects are important because they contribute to the majority of the defects in a mature process.

The most common defects that occur are shorts between the same metal layer resulting from extra material and bridges between different metal layers due to thin oxide layers. In addition there are opens in layers or in vias resulting from the absence of material. Another category is pinholes in oxide layers. Cracking of metal layers due to step-coverage problems is another issue, which, in the worst case, can become a open in the layer.

The effective detection and avoidance of these defects in a manufacturing process is essential for the quality of the devices developed in that technology. Information about these defects in a process is gathered by using specially designed test modules called Process Control Monitors (PCM). According to the information that can be acquired, there are four types of test structures that can be used for:

- a) Evaluating the functional properties of IC building blocks (test circuits)
- b) Extractions of IC geometric parameters like dimension
- c) Determination of the structural defect distribution and their influence on yield (short, breaks etc.)
- d) Determination of electrical parameters like I_c

In this paper we will discuss the third type of test structures. The information gathered using this structure is the basis for defect-based testing (DBT). Inductive fault analysis (IFA) is a widely used technique for DBT. It is based on the fact that the

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Fig. 1. Cross-section of the JeSEF process.

probability of a defect occurring is a function of the local layout geometry and the distribution of failure mechanisms observed from the manufacturing process. A defect ranking is used to create a realistic fault list. Faults are the defects that can cause malfunctioning of the realized circuit in the technology under study. In IFA, the faults are sprinkled on a fault-free layout according to the probability distribution of defects. Then, a detailed simulation of the circuit performance is carried out to evaluate faulty circuit behavior.

III. THE TRI-LAYER PROCESS AND ASSOCIATED DEFECTS

The process that we have been investigating is the JeSEF (Jena Superconductor Electronics Foundry) Nb tri-layer process. It has three Nb metal layers including the ground plane (M0, M1 and M2). A cross-section of the process is shown in Fig. 1. The minimum dimensions for interconnection width and spacing are $5\ \mu\text{m}$. The critical current density, J_c for the process is $1\ \text{kA}/\text{cm}^2$ and the sheet resistance of the Mo-resistor layer (R1) is $1\ \Omega/\text{square}$. The junction capacitance for the process is $0.05\ \text{pF}/\mu\text{m}^2$. Further details on the process are given in reference [5].

Until now, most research has been done on parametric defects in superconductor processes. As the processes become more mature, the importance of detecting the structural defects increases. This is due to the fact that the occurrence of gross manufacturing errors and deviation of parametric values are decreasing due to the maturity of the process. However, random defects can still occur due to various reasons like the presence of impurities, local wafer defects and human errors.

The present method to achieve robust design is carrying out margin calculations for RSFQ circuits to fabricate them with optimum values. To a certain extent, this ensures that the allowed gross process variations and the allowed random local variations will not affect the accepted performance of the circuit. During the test phase, the common practice for digital circuits is to load the data into a shift-register (SR) at low-speed, run the system “at-speed”, and store the processed data in the output SR. Finally, the readout is carried out at low-speed and the response is subsequently verified. This (functional) test will show whether or not the processed circuit will work. Further information about faults or defects is not available by this approach. Structural testing overcomes this problem because the faults are mapped to the physical defects in the process.

We have conducted an investigation [6] to get information about the types of defects that can occur in the JeSEF process. Looking at processed circuits, along with the design rules,

(a)

(b)

Fig. 2. SEM photographs of defective samples; a) M2-M1 cracked edge, b) same as a, but extra material that can cause potential shorts to nearby lines.

27 possible defects have been theoretically predicted for this process. These defects have been grouped and ranked into a list of probable defect locations. The primary defects are related to the thin oxide-barrier of a JJ. Shorts, opens and pinholes are believed to cause junctions to malfunction. At the immature stage of a process, the chance of a failure of a JJ is one in a thousand. Opens and near-opens in the top metal layer (M2) form the second ranking defect, resulting from the step coverage profile of the underlying SiO₂ isolation layer. A SEM photograph (Fig. 2) of this situation supports these arguments. Different other possibilities of opens or shorts in the different layers follow. A comprehensive list of the most probable defects is given in Table I.

IV. TEST STRUCTURES

A test chip has been designed in the JeSEF process, that allows detection and localization of the defects listed in Table I. Development of simple and easily-testable structures was crucial during the design phase. We came up with two types of structures: One set for low temperature (LT), 4K measurements

TABLE I
LIST OF MOST PROBABLE DEFECTS IN OUR TRI-LAYER PROCESS

No.	Defect Type	Nature of the defect
1.	Junction defects	Shorts, opens, excessive size of pin holes, excessive number of pin holes
2.	M2 defects	Opens or near-opens as a result of underlying steps in M1
3.	Resistor defects	Opens or near-opens in the M2-to-resistor contact, opens and near-opens in M2 at underlying steps, opens and near-opens in the Mo resistor, shorts between bias resistor terminals.
4.	M2 via defects	Opens or near-opens as a result of underlying vias

and the other set for room temperature (RT), 294K measurements [7]. If necessary, the LT structures can be tested at RT and vice versa. The 4K structures are placed at the four edges of the chip for easy bonding access. The RT structures are positioned at the center of the chip, which can be accessed by the probes of an automatic tester.

A. Junction Defects

Detection of the most probable defect is achieved at 4.2 K using a structure designed to reveal the most important junction quality parameters such as V_m [8], [9] (a measure of the junction leakage) and the critical current of the unshunted junction. It has been suggested in literature [10] that the switching properties of the JJ's can be used to find a single defect in a long chain of series connected JJ's. A model has been developed for detecting and pinpointing possible junction defects. The detection method has been developed to reduce the number of thermal cycles needed, thus reducing test cost and test time.

The method consists of an IV-curve measurement on several long series of JJ's. From the IV-curves it can be determined whether one of the long series possibly contains a defective JJ. A long series that is thought to contain a defect can be further investigated in detail by performing IV-curve measurements on segments of the long series. The procedure can be repeated down to segments containing 20 JJ's in series (Fig. 3).

The test chip contains three structures at the top, left and bottom edges of the chip, which each contain 2,560 JJ's in series. The JJ area has been varied among the three structures to determine possible area dependencies. The critical currents of the JJ's in the structures are 100 μ A, 200 μ A and 300 μ A respectively.

A separate test structure has been designed in which deliberate defects have been introduced into the JJ's by means of layout modifications. Shorts have been introduced by removing rectangular portions of different sizes from the tri-layer definition (T1) in the layout (Fig. 4(a)). Opens have been created by removing rectangular portions from both tri-layer and anodization definitions (I1A) (Fig. 4(b)). The purpose of this structure is to compare measurements on good and defective JJ's, to com-

Fig. 3. Part of the layout of the JJ chains designed to test for junction defects.

Fig. 4. Introduction of defects into the JJ and its cross-sectional view. a) short in the tri-layer and b) open in the tri-layer.

pare measurement and theory, and to develop a realistic fault model for the JJ.

B. Other Defects

Metal layer defects can be detected using a structure in which the metal runs over repeated steps of the underlying layer [11]: in our case, M2 running over repeated steps in underlying M1 (Fig. 5). At room temperature, the resistance of this path is measured and compared with the resistance of a reference path, called "v/d Pol structure" [12], with the same layout, though without the steps in M1. Deviations from the average measured resistance ratio will reveal opens or near opens in any of the test structures. A structure similar to the above has been designed to test for M2-via defects. The basis for the measurements is forcing current and measuring the voltage at fixed power dissipation.

Fig. 5. Part of the layout of the test structure to detect opens and near-opens in M2.

Fig. 6. Part of the layout of the structure for the detection of defects in the shunt resistors.

Resistors occur in two forms in superconductor electronics: as shunts for the JJ's and as bias resistors. Test structures have been designed for both types. They consist of a series chain of resistors in which defects can be detected by determining the total resistance of such a chain at room temperature.

V. CONCLUSION

This paper discusses the methodology for the development of a Nb tri-layer process to achieve higher yield. This forms the

basis for a systematic test scheme for RSFQ circuits. The probable defects that can occur in such a process were enumerated. Test structures were described in detail, which can be used to gather statistical information, i.e., the probability of the occurrence of defects in the process. This forms the basis for DBT, the first step for IFA.

The defect statistics obtained from the above test structures will be used for IFA. Depending upon the type of defect occurring in the processed circuit, it can be classified as semiconductor-like defects and special defects that apply to superconductor circuits. Resistive bridges and shorts are examples of semiconductor-like defects that can occur in the circuit. Shorts in a JJ are an example of the second kind. Our early study on this subject was published in reference [13]. The induced faults in the developed test structures will be used to validate the results of our earlier studies. The details of the test results from the test structures and further study on the actual defect behavior are subject for a future paper.

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