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Controlled Doping Methods for Radial p/n Junctions in Silicon

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P/n and n/p junctions with depths of 200 nm to several micrometers have been created in flat silicon substrates as well as on 3D microstructures by means of a variety of methods, including solid source dotation (SSD), low-pressure chemical vapor deposition (LPCVD), atmospheric pressure chemical vapor deposition, and plasma-enhanced chemical vapor deposition. Radial junctions in Si micropillars are inspected by optical and scanning electron microscopies, using a CrO_3-based staining solution, which enables visualization of the junction depth. When applying identical-doping parameters to flat substrates, ball grooving, followed by staining and optical microscopy, yields similar junction depth values as high-resolution scanning electron microscopy imaging on stained cross-sections and secondary ion mass spectrometry depth profilometry. For the investigated 3D microstructures, doping based on SSD and LPCVD give uniform and conformal junctions. Junctions made with SSD-boron doping and CVD-phosphorus doping could be accurately predicted with a model based on Fick's diffusion law. 3D-microstructured silicon pillar arrays show an increased efficiency for sunlight capturing. The functionality of micropillar arrays with radial junctions is evidenced by improved short-circuit current densities and photovoltaic efficiencies compared with flat surfaces, for both n- and p-type wafers (average pillar arrays efficiencies of 9.4% and 11%, respectively, compared with 8.3% and 6.4% for the flat samples).

1. Introduction

In the field of solar energy technology, (sub)micrometer p/n junctions in crystalline silicon are used for achieving charge separation at the surface of a solar cell.[1,2] To increase the efficiency of light capturing of solar cells, research has focused on nano/micro structures, e.g., wires, with shallow junctions.[3,4] Such structures have advantages over thin film and bulk silicon surfaces, such as higher surface areas and improved light-trapping capabilities.[5–8] Although both nano- and microstructures can be utilized, nanostructures put lower demands on the silicon quality due to shorter minority carrier diffusion lengths,[9] whereas micrometer-sized features can be created with more commonly used fabrication methods. Silicon micropillars, with diameters of a few micrometers and heights of tens of micrometers containing radial p/n junctions, have also received increased attention, not only for solar cells, but also for solar-to-fuel applications, as they can be functionalized in a controlled manner with various catalysts.[10–13] Using radial junctions, increased efficiencies over flat surfaces can be obtained, due to greatly enhanced carrier collection in nano/micropillars.[7,13] In addition, the radial junction contributes to a lower surface recombination rate for the overall device.[14,15] Here, we investigate different doping methods applied to silicon micropillars, in order to obtain optimal geometry control of the pillars and p/n junctions therein, as well as ease of utilization for further applications. Silicon-based p/n junctions can be realized by various doping methods. Standard doping techniques reported in literature include ion implantation,[16] solid source dotation (SSD),[17] monolayer doping,[18] spin-on dopant,[19] as well as regular chemical vapor deposition (CVD), low-pressure chemical vapor deposition (LPCVD), plasma-enhanced chemical vapor deposition (PECVD), and atmospheric pressure chemical vapor deposition (APCVD).[20] Not all techniques are suited for 3D structures, for example, ion implantation is limited to flat surfaces because of its directionality, while PECVD, in contrast to LPCVD, does not give conformal step coverages, except for highly tuned process conditions.[21] Furthermore, high-density pillar arrays with small pillar spacing and/or large aspect ratios can suffer from

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nonuniform doping of the 3D structures, in particular across the height of the structures.[22,23] Thorough investigations of whether common doping techniques lead to a controlled junction depth in doped micro- and/or nanopillars have not been reported. Here, we present different doping methods for both n-type (phosphorus, P) and p-type (boron, B) doping of 3D crystalline silicon microstructures. We used SSD in the case of boron doping, and several CVD techniques (LPCVD, APCVD, and PECVD) for phosphorous doping. For comparison, junction depth analysis after doping with these techniques is done also on flat surfaces, using ball grooving and chemical staining. Junctions in ridges and micropillars were analyzed by cross-sectional imaging using high-resolution scanning electron microscopy (HR-SEM). Secondary ion mass spectrometry (SIMS) was applied to flat samples to verify junction depths and surface concentrations. *J–V* measurements were performed under the standardized AM (air mass) 1.5 G (global) illumination. The experimental results were compared with finite element calculations of the dopant diffusion processes in flat and pillar structures. This combination of experimental analysis and numerical simulations forms a route to determine the optimal settings for structured solar cells and solar-to-fuel devices.

2. Materials and Methods

2.1. Fabrication of Microstructure Arrays

On p- and n-type silicon substrates (<100>-oriented, resistivity 5–10 Ω cm (p-type) and 1–10 Ω cm (n-type), 100 mm diameter, thickness 525 µm (p-type) and 375 µm (n-type), single side polished, Okmetic Finland), arrays of silicon microstructures were fabricated. Prior to processing, the substrates were cleaned by immersion in 100% nitric acid (HNO_3) (2 × 5 min), and in fuming 69% nitric acid (15 min), which was followed by quick dump rinsing in demineralized (DI) water, immersion in 1% aqueous hydrofluoric (HF) acid to remove the native oxide prior to silicon nitride deposition and another quick dump rinsing cycle. After spin drying (6000 rpm) of the wafers, 100 nm thick nitrogen-rich silicon (SiRN) was deposited using LPCVD, to prevent doping the backside of the wafer. With reactive-ion etching (RIE) (Adixen AMS100DE; octafluorocyclobutane (C_4F_8) and methane (CH_4)) the SiRN layer on the front side of the wafer was removed, followed by an oxygen plasma treatment and piranha (mixture of sulfuric acid and 30% aqueous hydrogen peroxide, 3:1 (v/v), 20 min) cleaning to remove any contamination. For use as a hard mask during etching, a layer of 2 µm silicon dioxide (SiO_2) was grown using wet oxidation (1150 °C). By means of standard UV-lithography (on wafer scale) for each 2 × 2 cm^2 sample, a centered 0.5 × 0.5 cm^2 area with an array of micropillars (diameter 4 µm, spacing 2 µm, hexagonally stacked with a packing density of 35%) or ridges (width 100 µm, spacing 100 µm, height 30 µm) was defined in photoresist (Olin 907-17), and postbaked for 10 min at 120 °C after development. The photoresist pattern was transferred into the SiO_2 layer by means of RIE (Adixen AMS100DE; C_4F_8, CH_4). The photoresist, in combination with the SiO_2, acted as a mask layer during deep reactive-ion etching (DRIE) (Adixen AMS100SE) of silicon using the Bosch process, i.e., a cyclic process employing sulfur hexafluoride (SF_6) for etching silicon and C_4F_8 to create a passivation layer on the sidewalls. The height of the pillars was determined by the etch duration, and was set to 20 min, resulting in pillar heights of approximately 60 µm. After etching, the photoresist mask was stripped with oxygen plasma, followed by piranha cleaning (20 min). Subsequently, the SiO_2 layer was removed with 50% aqueous HF. The substrate was cleaned from the remaining fluorocarbons in the DRIE process by oxidizing the surface at 800 °C (30 min), immersion in 1% aqueous HF (10 min), rinsing in DI water and drying.

2.2. Doping Methods

Doping of the arrays of silicon micropillars was done using various techniques, i.e., SSD, LPCVD, APCVD, and PECVD. In all cases a dopant-containing oxide layer was formed on the silicon surface, which was followed by a thermal drive-in step to transfer the dopant into the silicon. In this work, the drive-in temperature ranged from 900–1050 °C and the drive-in time was in the range of 15–120 min. Prior to processing, all wafers were immersed in 1% aqueous HF acid (10 min), rinsing in DI water and drying, to expose a H-terminated Si surface. To remove the dopant oxide layer after the doping process, wafers were immersed in buffered hydrogen fluoride (1:7, 10 min), oxidized at 800 °C for 15 min and etched in 1% HF (15 min), rinsed and dried. Below for each doping method details are given on the formation of the dopant containing oxide layer.

2.2.1. Solid Source Dotation

In the case of SSD of boron, n-type silicon wafers were placed in-between boron nitride wafers, in a wafer boat. By increasing the temperature up to 800 °C and supplying sufficient amounts of oxygen under a continuous oxygen flow (6000 sccm), a boron oxide (B_2O_5) layer (≈200 nm) was grown on the surface of the Si wafers in 30 min. The temperature is then increased further to start the diffusion process for the desired time and temperature. Meanwhile the boron oxide layer will continue growing as well.

2.2.2. Chemical Vapor Deposition

For CVD, three different processes were used; an atmospheric pressure CVD (APCVD), a low-pressure CVD (LPCVD), and a plasma-enhanced CVD (PECVD). For the APCVD of phosphorus on p-type Si, gas-phase deposition was used to create a dopant oxide layer: at 950 °C a mixture of 4500 sccm phosphine (PH_3) and 1200 sccm O_2 was flushed through the furnace for 30 min. In the LPCVD process, wafers were loaded in a boat filled with dummy wafers, for optimal growth conditions on wafers. For a deposition time of 30 min at 650 °C, a gas flow of 330 sccm PH_3 and 150 sccm O_2 was used to grow the phosphorus oxide (at a pressure of 350 mTorr). PECVD was utilized to deposit a phosphorus glass layer on flat p-Si wafers. At 300 °C and 1050 mTorr, a gas flow of PH_3 (100 sccm) was flushed through the chamber for 15 min, in combination with 200 sccm N_2O and 700 sccm N_2. A DC voltage of 50 W was used.

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2.3. Analysis Methods

2.3.1. Ball Grooving and Staining

To analyze the p/n junctions on flat surfaces, a stainless steel ball (60 mm diameter) was used to expose the junction, by grooving the surface.[24] To improve the grooving rate, diamond paste was applied to the ball. Typically only a few seconds were required to grind sufficiently deep (i.e., through the junction) to a depth of 2–3 µm. After grooving, the samples were cleaned with ethanol.

Revealing the depth of a p/n junction was done using an etching solution for delineation along the p/n junction region, following the procedure as described in a patent by Roman and Wilson.[25] Chromium trioxide (CrO_3) was mixed with DI water in a ratio of 1 to 3 (w/w), subsequently a 50% aqueous HF solution (10 vol% of the starting solution) was added to the CrO_3 solution. Samples were placed in the resulting solution for 25 s, and subsequently rinsed with DI water and dried with a stream of nitrogen. After this staining reaction, a contrast difference is visible under a normal light microscope, in which the p-type Si area becomes darker than the n-type Si. **Figure 1** shows schematic cross-sectional and top views of a stained groove. The same is possible for n-type doping in a p-type wafer. Although the contrast is less pronounced in this case, the contrast circle is still clearly visible.

To calculate the junction depth (x_j) after staining of the groove, the diameters (*a,b*) of the two formed circles were determined. Then x_j (µm) was calculated as:

$$x_j = \frac{a^2 - b^2}{8 \times R} \quad (1)$$

where *a* is the outer diameter of the circle (µm), *b* the inner diameter (µm), and *R* the radius of the stainless steel ball (µm). A light microscope (Olympus BHMJL, 5× magnification, Analysis software) was used to measure *a* and *b*.

2.3.2. High-Resolution Scanning Electron Microscopy

To analyze the junctions, HR-SEM images of cross-sections of doped ridges and micropillars were taken on an Analysis Zeiss-Merlin HR-SEM system with an InLens detector. For ridges, samples were broken with a diamond pen perpendicular to the length of the ridges. Focused ion beam (FIB) and RIE were used to open up and image the micropillars.

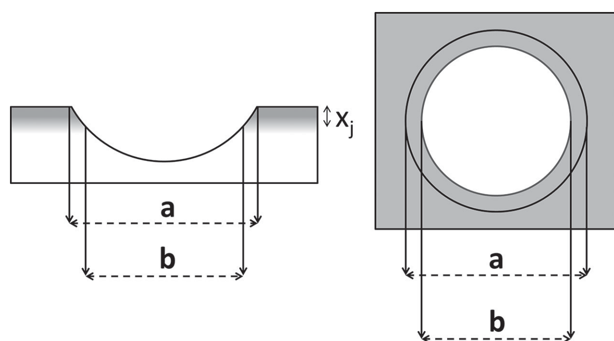

Figure 1. Schematic cross section (left) and top view (right) of a stained groove on a flat silicon surface. The dark-gray area indicates the boron-doped Si layer, whereas the white part is the bulk n-type Si.

FIB structures and images were made with a Nova 600 Dual-Beam—SEM/FIB setup. A Ga^+ liquid metal ion source was used to mill away enough of a pillar to be able to accurately determine the junction location, with a beam current of 0.92 nA and 10 kV extraction voltage.

2.3.3. Secondary Ion Mass Spectrometry Measurements

SIMS depth profiles of doped flat samples were recorded using a Cameca ims6f using 7.5 keV O_2^+ primary ions in positive mode. Secondary ions ($^{31}P^+$ or $^{11}B^+$) and $^{28}Si^{28}Si^+$ as a reference were detected. Quantification and depth calibration were based on reference implants. Depth scale calibration was based on final crater depth measurements using optical profilometry. For each dopant setting, only one measurement was performed.

2.3.4. Electrical Characterization

To investigate the electrical properties of the formed junctions, front- and backside contacts were made by sputtering 1 µm aluminum/silicon alloy (99% Al, 1% Si). Samples were placed perpendicular to a 300 W xenon arc light source, which was calibrated to match the intensity of 1 sun (AM 1.5). In case of p/n junctions created on low-doped n-type Si (≈10^{15} atoms cm^{-3}), the backside of samples was doped with phosphorus (similar to the procedure for junction formation) to create n^+ Si. This was necessary to ensure ohmic contact between the aluminum/silicon alloy and n-type silicon. *J–V* measurements were recorded on a VersaSTAT 4 potentiostat. For each dopant setting, at least five different samples were measured.

2.3.5. Finite Element Simulations of Boron and Phosphorus Doping

Junction depths and doping concentrations of p/n junctions created with SSD, LPCVD, and PECVD were simulated in COMSOL Multiphysics (version 4.4) using the finite element method (FEM). All simulations were done with a time-dependent transport of diluted species on rod-like structures of various dimensions (similar to the realized pillar arrays), using a free tetrahedral mesh, with a maximum mesh size of 0.5 µm and a minimum of 1 nm. The boron (or phosphorus) oxide source was simulated as an infinite source of dopant atoms, with a fixed surface concentration (≈10^{22} atoms cm^{-3}). Three drive-in temperatures were simulated in time, i.e., 900 °C, 1000 °C, and 1050 °C. Although heating up and cooling down of the furnace was also included in the simulation, the mentioned drive-in times always correspond to the duration of the drive-in temperature step after stabilization to its desired value.

3. Results and Discussion

Figure 2 shows the schematic illustration of the fabrication of micropillars on a base p-type wafer, radially doped with

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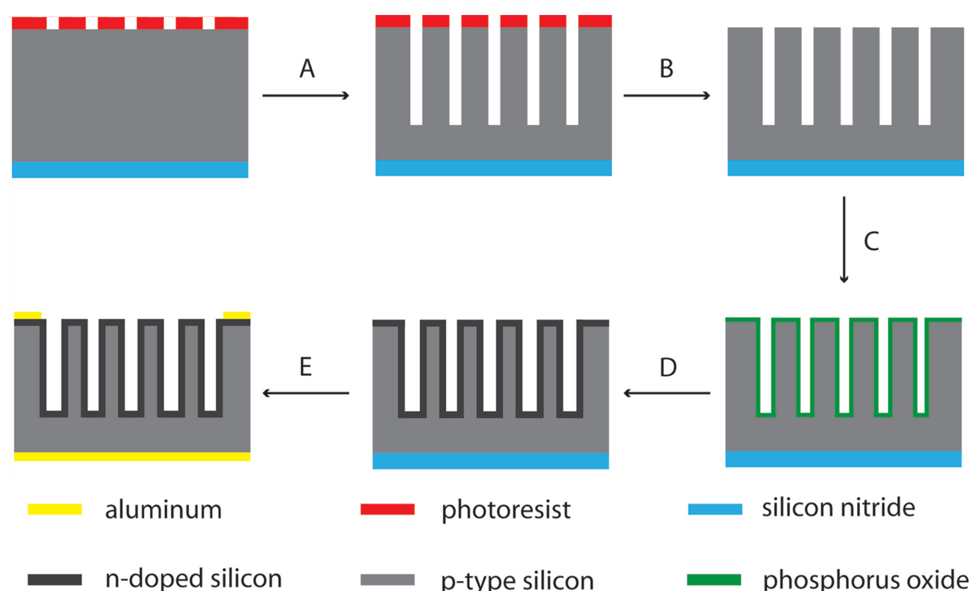

Figure 2. Schematic illustration of the fabrication of radial p/n junctions in silicon micropillars. A) Fabrication of silicon micropillars using DRIE on patterned photoresist on a silicon wafer. B) Removal of residual photoresist by O_2 plasma etching. C) Formation of a phosphorus oxide layer, using CVD. D) In-diffusion of phosphorus into the boron-doped base wafer. E) Removal of silicon nitride backside by HF etching, immediately followed by sputtering of the aluminum contacts. The same procedure was followed for boron doping of n-type Si wafers, with SSD instead of CVD for the deposition of the dopant oxide layer.

phosphorus. First, the backside of the wafer was covered with silicon nitride, which acts as a diffusion barrier to prevent the formation of a junction on the backside. The desired pattern of micropillars was transferred to the wafer using standard photolithography, and dry etching to achieve the desired height of the pillars. In order to fabricate a radial p/n junction a phosphorus oxide was grown by CVD processes. A similar procedure was followed for boron doping of n-type Si wafers, with SSD for the deposition of the dopant oxide layer. Subsequently, a thermal step was done at a set temperature and time, to create a p/n junction with the targeted junction depth. Finally, aluminum contacts were fabricated on the front and backside (upon removal of the SiRN layer) of the wafer to ensure ohmic contact to the silicon. In case of ridges and flat surfaces, the same procedure was followed, but then with larger dimensions and without any photolithographic pattern, respectively.

3.1. Junction Analysis on Flat Substrates

After the diffusion of the dopant, step D in Figure 2, the p/n junctions were analyzed by different methods. For flat surfaces, ball grooving and SIMS measurements were performed. **Figure 3** shows typical grooves, under a light microscope, formed on flat-doped surfaces by a stainless steel ball before (A, C, E) and after (B, D, F) staining. In case of an n-type Si wafer that is boron-doped via SSD (Figure 3A,B), the inner part after staining (Figure 3B) shows the base n-type silicon and the gray-colored outer ring is the p-doped layer. Conversely, for p-type wafers that were doped with phosphorus by means of PECVD (Figure 3C,D) and LPCVD (Figure 3E,F), the inner part (base p-type) is darker than the outer ring (doped n-type), although this effect is less pronounced in the case of LPCVD doping. Diameters of both circles in the stained images were measured with image analysis software and junction depths (**Table 1**) were calculated by means of Equation (1). Thus, although the ball grooving and staining technique was originally developed for junctions with depths of >10 µm, it also functions for junctions with a depth in the range of submicrometers to a few micrometers.

Figure 4 shows depth profiles of dopants as measured by SIMS on various flat doped samples. As the base doping level of the silicon substrates was not measured with SIMS, but only derived from the resistivity, an accurate determination of the junction depth cannot be made. The base doping level varies from 5×10^{14} to 5×10^{15} atoms cm^{-3}, which is in the range of the measurement limitations of the SIMS system. Therefore, an extrapolation over the linear regime (as indicated in Figure 4) was used to estimate the junction depths (Table 1), assuming an average doping level of 10^{15} atoms cm^{-3}. The differences in junction depths as determined with the staining method and the SIMS method are small, about 0.1–0.3 µm, where SIMS indicates generally somewhat deeper junctions. Nevertheless, the observed trends in junction depth as function of drive-in temperature and time are identical for both methods.

When comparing the different doping methods for phosphorus, the junction depths of the APCVD-doped samples differed significantly from the other doping techniques. For the same time and temperature settings (15 min, 1050 °C), APCVD yielded a junction twice as deep as for LPCVD (2.3 vs 1.1 µm). The SIMS profiles (Figure 4) give additional insight in the different doping mechanisms. For P-APCVD, the dopant concentration profiles show a bend at about 1 µm, and the surface concentrations exceed 2×10^{20} atoms cm^{-3}. This is not the case for P-LPCVD and B-SSD doping, for which the diffusion profiles decrease monotonously.

In **Figure 5**, the experimentally determined junction depths are plotted (symbols) for three different temperatures and

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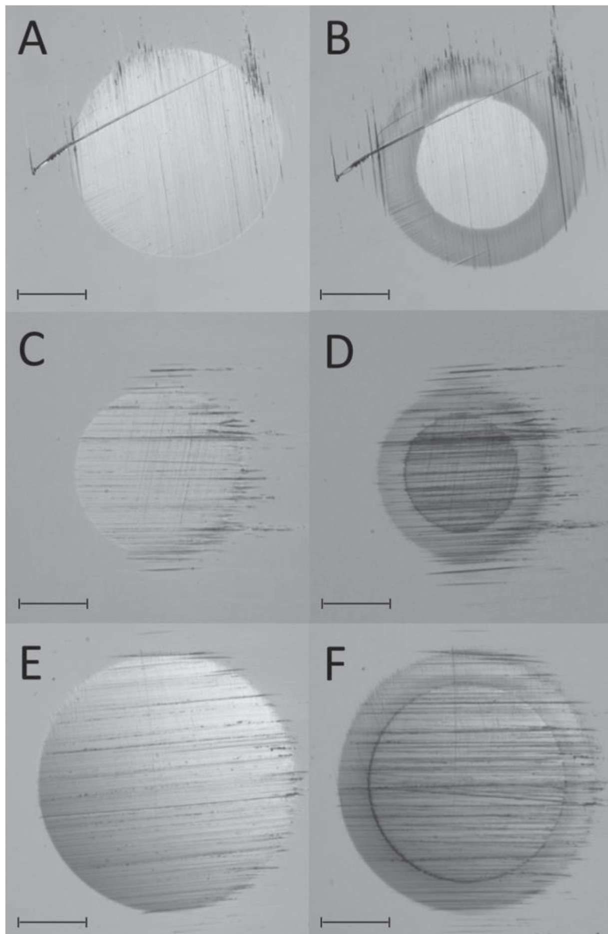

Figure 3. Optical microscopy images of flat, doped Si samples after ball-grooving, before (A, C, E) or after (B, D, F) staining with CrO3/HF. A,B) SSD-boron doped n-type Si (1050 °C, 15 min), C,D) P-PECVD doped p-type Si (1000 °C, 15 min), E, F) P-LPCVD doped p-type Si (1050 °C, 15 min). Scale bars represent 200 μm.

various doping techniques. Each symbol is an average over at least five measurements (ball grooving). Moreover, FEM simulation results, assuming simple Fick's law diffusion, are also given in Figure 5 (solid lines).

Table 1. Junction depth values of boron (SSD) and phosphorus (CVD)-doped samples, based on data obtained from ball-grooving and staining and from SIMS.

	Staining [μm]	SIMS [μm]
P-LPCVD 15 min, 1050 °C	1.1 ± 0.1	1.1 ± 0.1
P-PECVD 15 min, 1050 °C	1.0 ± 0.1	–
P-APCVD 15 min, 1050 °C	2.8 ± 0.1	3.0 ± 0.2
P-APCVD 100 min, 1000 °C	2.3 ± 0.1	2.4 ± 0.2
B-SSD 15 min, 1000 °C	0.6 ± 0.1	0.7 ± 0.1
B-SSD 15 min, 1050 °C	1.0 ± 0.1	1.3 ± 0.1
B-SSD 120 min, 1050 °C	2.2 ± 0.1	2.5 ± 0.2

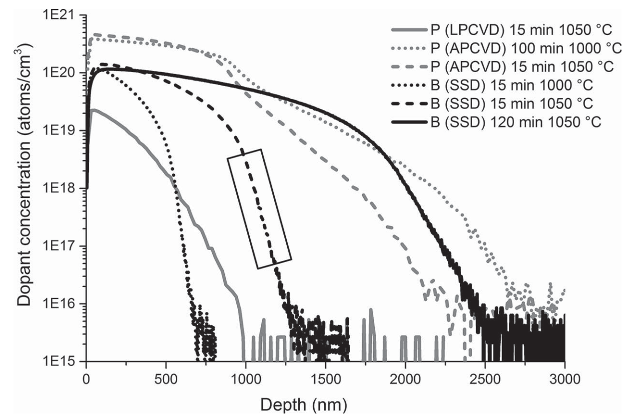

Figure 4. SIMS depth profiles of dopant elements (B/P) of flat, doped samples obtained at different in-diffusion temperature and time settings and using different doping processes (P-LPCVD, P-APCVD, and B-SSD). The marked area is an example of the linear regime, used to extrapolate a more accurate junction depth, for boron doped (SSD) at 1050 °C for 15 min.

Clearly, most of the data points agree with the FEM simulations, except, as expected, the phosphorus-based junctions realized by APCVD. In fact, the junction depths obtained for this doping method are significantly larger than predicted by modeling and those found experimentally using other doping methods. This can be attributed to the high surface concentration of this doping method. High (surface) concentrations of phosphorus can give rise to anomalous kink-and-tail depth-diffusion profiles with a plateau region near the surface.[26] In case of sufficiently high P surface concentrations (> 2×10^{20} atoms cm^{-3} at a drive-in temperature of 1000 °C), the so-called vacancy mechanism governs the dopant diffusion in the plateau region (at depths up to ≈1 μm), while the kick-out mechanism governs it in the deeper regions. In other words, diffusion of self-interstitials—also named point defects—dominates in the kink region, and P interstitials in the tail region. Only at high P concentrations, the vacancy mechanism contributes to P diffusion (and thereby enhances the overall dopant diffusion speed). The change-over from the vacancy mechanism to the kick-out

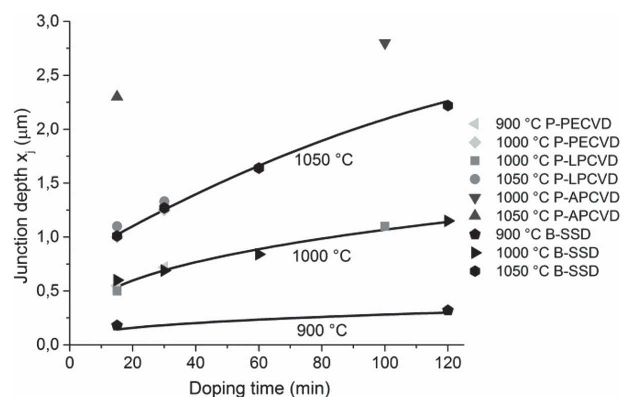

Figure 5. Junction depth as a function of drive-in time and temperature: solid lines represent simulations and symbols represent experimental data by means of ball grooving and staining. Error bars are not shown; the largest standard deviation was 0.09 μm.

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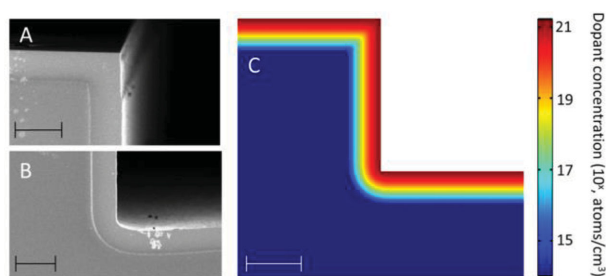

Figure 6. A,B) Cross-sectional HR-SEM images (80° angle) of 100 × 30 μm^2 ridges (SSD-boron doped; 1050 °C, 120 min). Scale bars represent 3 μm. C) Cross section of FEM simulated doping (SSD-boron doped; 1050 °C, 120 min) of a ridge structure.

mechanism is responsible for the appearance of the kink-and-tail depth-diffusion profiles visible in Figure 4 (APCVD data). In contrast, for low P surface concentrations, only the kick-out mechanism affects the depth-diffusion profiles, and no plateau appears. In this case, Fick's diffusion law is valid as a model for P (and B) diffusion into silicon, as shown for the investigated PECVD, LPCVD, and SSD settings. Due to the anomalous diffusion mechanism in the case of P-APCVD doping, this method is excluded from further analysis.

3.2. Junction Analysis in Structured Substrates

3D ridge and pillar structures, boron-doped using SSD (1050 °C for 120 min), were investigated subsequently. **Figure 6**A,B show HR-SEM images of cross sections of ridge samples after staining with CrO_3/HF. Similar to staining on flat-doped surfaces, the staining is clearly visible in terms of a line on the junction interface. The junction depth of 2.2 μm agrees with FEM simulations (Figure 6C) and with the staining experiments on flat surfaces (see above). The latter indicates that ball grooving of flat surfaces suffices to get a good indication of the junction depth also of micrometer-sized 3D structures. The sharp edge on the top (convex corner Figure 6B) and the round shape in the bottom corner (concave corner Figure 6C) are also present in the simulated ridge (Figure 6A). The images and simulations clearly indicate that boron-SSD on 3D structures yields a uniform thickness of the doped layer.

Subsequently, the staining method was applied to micropillar structures. Two different approaches were used to stain the interior of pillars. In the first approach, the top of doped pillars was removed by means of a maskless DRIE step, as shown in **Figure 7**C. This enables a top view on such "chopped" pillars with SEM imaging (Figure 7A). Chopped pillars were also exposed to the staining solution, resulting in the appearance of a clear line on the inside of the pillar, as shown in Figure 7B, which resembles the p/n interface. The second approach employed FIB etching to laterally remove half of a pillar. This enabled visualization of the junction along the height of a pillar (Figure 7D).

In case of the first approach—pillar chopping and staining (Figure 7A,B)—the stained pillar clearly reveals the junction and junction depth (2 μm). This stained line was also observed for the second approach, in which a pillar was cleaved vertically.

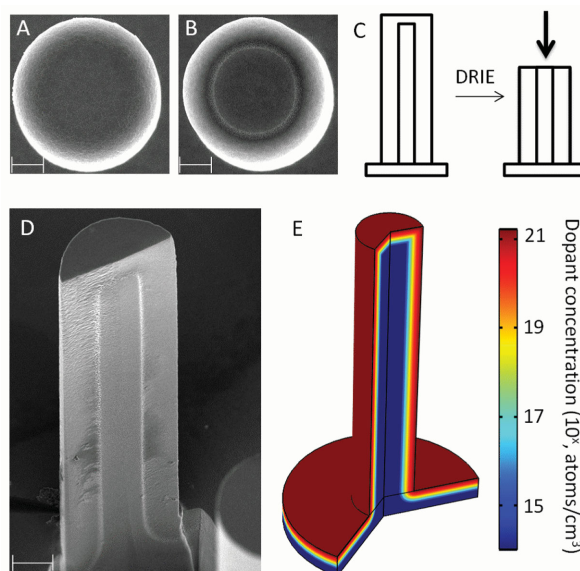

Figure 7. A,B) Top view SEM images of unstained (A) and stained (B) pillars (boron doped SSD at 1050 °C, 120 min). C) Schematic view of maskless DRIE in a pillar (cross section), to reveal the interior of the pillar. The thick arrow indicates the imaging direction of A and B. D) Side view of a split (using FIB) and stained pillar. E) FEM simulation of a pillar with similar dimensions (4 μm width, 20 μm height, boron doped at 1050 °C, 15 min). Scale bars represent 2 μm.

As expected, the staining line perfectly follows the contour of the pillar: a uniform thickness (2 μm) of the doped layer along the pillar circumference can be seen. The difference in surface roughness at the FIB interface visible between the left-hand and right-hand side of the cleaved pillar in Figure 7D is an artifact from a second FIB step.

The seemingly thinner junction at the top side of the pillar is merely a result of the large angle at which the image was taken. Junction depths as determined with both approaches are in agreement with previous measurements on flat samples (see above) and FEM simulations (Figure 7E, 2.2 μm).

Similar results regarding uniform doping along the pillar height were obtained for P-LPCVD-doped samples. In the case of P-PECVD-doped pillars, no contrast was visible along the pillar height, which is believed to be caused by directionality during formation of the dopant layer. For this reason, the P-PECVD samples were excluded from the *J*–*V* measurements.

3.3. Electrical Characterization

In order to verify the influence of radial p/n junctions on light capturing capabilities, *J*–*V* measurements were performed on doped flat surfaces and similarly radially doped micropillar arrays, i.e., SSD-boron on n-Si and LPCVD-phosphorus on p-Si (1050 °C, 15 min). *J*–*V* plots are shown in **Figure 8**. The open-circuit voltage (V_{OC}) for boron-doped samples is approx. 0.5 V, whereas for phosphorus doped samples the V_{OC} is approx. 0.45 V, which is slightly lower than the 0.5–0.7 V reported in literature for silicon.[1,2,27] It has to be noted that,

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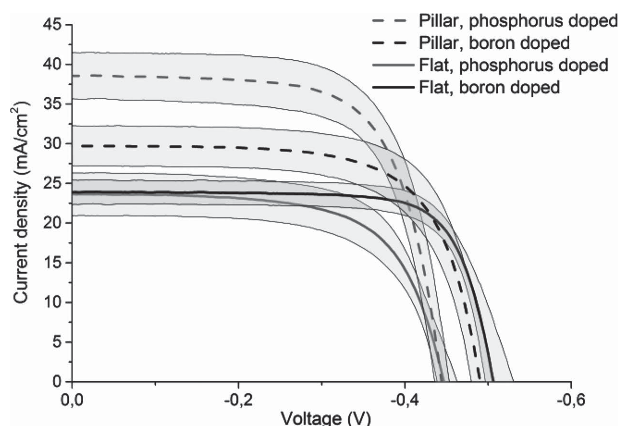

Figure 8. *J–V* measurements of different samples: flat junctions (continuous lines) and radial junctions in pillar arrays (dashed lines) for boron and phosphorus dopants. The light grey areas indicate the 1σ-range around the average (at least five samples were analyzed for each configuration). The current density is normalized to the sample area (not the actual surface area of the pillars).

in contrast to many literature studies, neither back reflector nor surface passivation was applied in our work. For both boron and phosphorus doping, the short-circuit current density (J_{SC}) values were significantly higher for pillar samples—30 and 38 mA cm^{-2} for boron and phosphorus doping, respectively—compared with doped flat samples (ca. 24 mA cm^{-2}).

Using the fill factor (FF), V_{OC} and J_{SC}, the overall efficiency η can be calculated (Equation (2)):

$$\eta = \frac{V_{OC} J_{SC} FF}{P_{in}} \quad (2)$$

where P_{in} is the input power, which is 100 mW cm^{-2} (AM 1.5).

For boron-doped samples, the efficiency increased from 8.3% for flat samples to 9.4% for pillar arrays, whereas phosphorus-doped samples showed η values of 6.4% and 11.0% for flat and pillared samples, respectively. These efficiencies for radially doped p/n junctions are in agreement with literature values, typically showing efficiencies above 5%.[1,2,19,27,28] Thus, properly doped radial p/n junctions indeed enhance the light trapping via an increase in effective junction area on a given footprint (0.5×0.5 cm^2).

A pillar array with a junction depth larger than 2 µm (SSD-boron of n-Si, drive-in settings: 1050 °C/120 min) was also subjected to *J–V* analysis. In this case, the junction depth is larger than the pillar radius, leading to completely doped-through pillars. Such over-doped pillar arrays displayed a low J_{SC} value (7 mA cm^{-2}), which can be attributed to a loss of effective junction area on the 0.5×0.5 cm^2 footprint: 35% of the sample footprint is covered with pillars. Although the pillars themselves do lower the reflectivity of the sample, this is apparently not sufficient to compensate for the loss in effective junction area. As expected, over-doped pillars showed a poor efficiency (2%). Altogether, these results show the potential of using radially doped micropillars for more efficient light capturing, at the same time emphasizing the need for proper control of the doping process to achieve the appropriate junction depth.

4. Conclusion

All investigated doping methods, i.e., SSD, LPCVD, APCVD, PECVD, gave uniform p/n junctions on horizontal/flat surfaces. SSD and LPCVD also yielded homogeneous junction depths on 3D structures (i.e., microridges, micropillars) in silicon. Ball grooving and staining on flat surfaces yielded accurate values for junction depths, and the values are similar to data based on HR-SEM (on flat and 3D samples) and SIMS. Junctions made by doping using B-SSD, P-LPCVD, or P-PECVD can be accurately predicted using Fick's law. In case of P-APCVD junctions, the measured dopant concentration profiles (and hence junction depths) deviated from model results, typically resulting in much deeper junctions. This is attributed to an additional diffusion mechanism (i.e., vacancy mechanism).

Radial junctions made by SSD (boron) and LPCVD (phosphorus) doping had higher J_{SC} values and efficiencies compared with doped flat surfaces. The positive effect on light capturing by arrays of properly doped radial junctions was further evidenced with experiments on over-doped pillar arrays, which displayed an even lower J_{SC} than doped flat substrates.

Future experiments will focus on the effect of the junction depth in micropillar arrays and footprint size on the light capturing efficiency. Moreover, such pillar arrays with radial junctions will be implemented in solar-to-fuel devices.

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