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TECHNICAL BRIEFS

GREEN ELECTRONIC DEVICES—RECENT TRENDS



*Albert Chin
National Chiao-Tung
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The IC chips consume a large amount of energy globally and will continue to increase in the future. In an IC chip set with system-on-chip functions, the rate of using energy, or power, is consumed in complementary metal-oxide-semiconductor field-effect transistors (CMOSFETs), volatile DRAM memory, and non-volatile flash memory. Here both DC and AC switching power (P_{DC} and P_{AC}) consumptions need to consider in these devices. Because no DC current flows in a CMOS inverter, the P_{DC} only counts the leakage current in the MOSFET. The P_{AC} in these capacitive devices equals $CV_s^2f/2$; here C , V_s , and f are the capacitance, switching voltage, and operation frequency, respectively. In a typical chip set, the P_{AC} is mainly consumed in logic CMOS and DRAM, since the flash memory operates at a much slower f . The DRAM has extra P_{DC} and P_{AC} consumptions compared with MOSFET, due to its one-transistor one-capacitor (1T1C) structure. To reach ultra-low P_{DC} and P_{AC} , novel materials, structure, and device physics are needed that lead to the Green Electronic Devices.

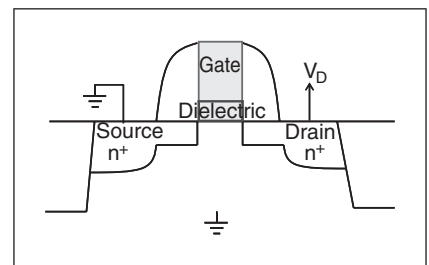


Fig. 1 schematic diagram of an nMOSFET.

Figure 1 shows the schematic diagram of an nMOSFET. The figures of merit of a MOSFET are the low drain off leakage ($I_{D,OFF}$), high drain on current ($I_{D,ON}$), and low gate dielectric leakage (I_G). The low $I_{D,OFF}$ and I_G are necessary for low P_{DC} , while the high $I_{D,ON}$ is important to charge the load capacitors and reach a high circuit speed. The $I_{D,ON}$ per gate width

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YOUR COMMENTS SOLICITED

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at
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NEWSLETTER DEADLINES

ISSUE	DUE DATE
January	October 1st
April	January 1st
July	April 1st
October	July 1st

The EDS Newsletter archive can be found on the Society web site at <http://eds.ieee.org/eds-newsletters.html>. The archive contains issues from July 1994 to the present.

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GREEN ELECTRONIC DEVICES—RECENT TRENDS

(continued from page 1)

of a MOSFET equals gate voltage (V_G) induced charge ($Q_i = C_i \times (V_G - V_T)$) multiplying effective velocity (v_{eff}) in a semiconductor, where C_i , $V_G - V_T$, and V_T are the gate capacitance, gate overdrive voltage, and transistor's threshold voltage, respectively. One method to reach a higher I_{D-ON} is to increase the $C_i (= \epsilon_0 \kappa / t_{ox})$ by using a thinner gate oxide (t_{ox}); the ϵ_0 and κ are the respective vacuum permittivity and dielectric constant. The thinner t_{ox} also improves the gate controllability and suppresses the short channel effect in a highly scaled device. Therefore, the SiO_2 gate dielectric was continuously scaled down into an ultra-thin 1.2 nm at the 65 nm CMOS node. However, this device suffers from a very high direct tunneling current through the 1.2 nm SiO_2 layer. Such high I_G causes intolerable high P_{DC} in a VLSI IC. To address this issue, high- κ gate dielectric with a higher C_i , larger thickness, and lower gate leakage current than SiO_2 must be used. To further increase the C_i , conventional doped poly-Si gate electrode was replaced by metal-gate to reduce the parasitic capacitance between poly-Si and high- κ layer. Currently, the high- κ and metal-gate technologies are widely implemented in IC manufacture that can improve the P_{DC} for more than one order of magnitude.

One important driving force to continuously scale down the device is the lower drain voltage (V_D) and P_{AC} , in addition to the higher integration density and lower cost. However, as shown in Fig. 2, downscaling also increases the I_{D-OFF} and P_{DC} . To solve these drawbacks, the transistor turn-on sub-threshold slope (SS) needs to be improved. This can be realized by using an ultra-thin Si body in a Si-on-Insulator (SOI), FinFET or tri-gate structure, with better carrier confinement and gate controllability. The FinFET has been successfully implemented in the sub-20 nm

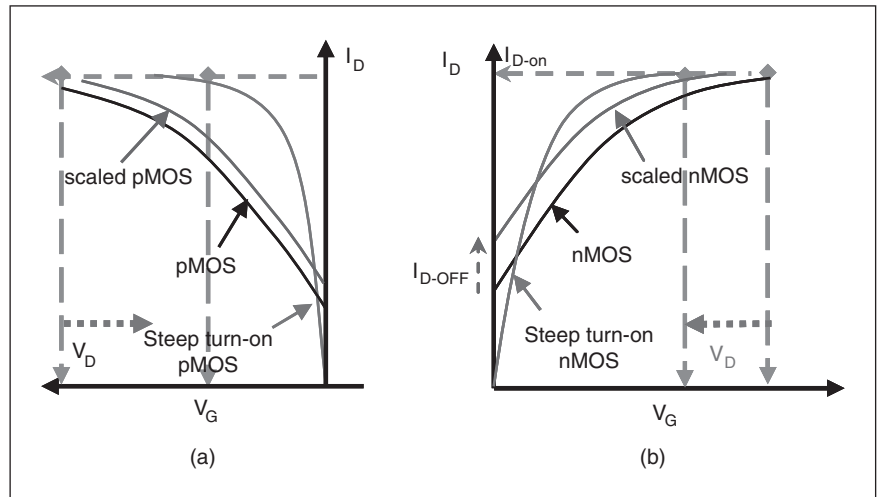


Fig. 2 The I_D - V_G characteristics of (a) pMOSFET and (b) nMOSFET before and after downscaling. Although the downscaling lowers V_D and P_{AC} , the I_{D-OFF} and P_{DC} become worse. One solution is to improve the turn-on SS.

CMOS, together with the metal-gate/high- κ technology.

To further scale down into sub-10 nm, the I_{D-OFF} increases again in a FinFET due to quantum-mechanical tunneling current from small source-drain distance. One potential solution is to operate the MOSFET at a lower electric field and voltage. To compensate the I_{D-ON} degradation at a lower $V_G = V_D$, higher v_{eff} or effective mobility (μ_{eff}) semiconductor materials need to be used. Fig. 3 shows the μ_{eff} as a function of gate effective field (E_{eff}) of the Ge-on-Insulator (GOI) pMOSFET. The 2.6X higher hole mobility than universal SiO_2/Si pMOSFET was obtained at a lower 0.5 MV/cm E_{eff} . Because the MOSFET is generally operated at >1 MV/cm E_{eff} , the low E_{eff} allows the device operating at >2 times lower voltage that in turn improves the I_{D-OFF} , P_{DC} , and P_{AC} . Similar lower voltage operation was also reached in high electron mobility InGaAs nMOSFET, although low I_{D-OFF} still needs to demonstrate for InGaAs nMOSFET on Si substrate.

The ultimate limitation of Ge-pFinFET/InGaAs-nFinFET is the 60 mV/

decade transistor turn-on SS at room temperature, governed by the mechanism of carrier injection over the source energy barrier. Although the tunnel FET (TFET) has a small SS < 60 mV/dec, the I_{D-ON} is significantly lower than conventional MOSFET. This becomes even worse in p-TFET due to its large hole mass for tunneling. Alternatively, steep turn-on CMOS using ferroelectric gate dielectric was proposed. As shown in Fig. 4, experimental pMOSFET using novel ferroelectric high- κ HfZrO shows a very steep turn-on SS (1.8–60 mV/dec) and an extremely low I_{D-OFF} , which are already better than those of FinFET. This low SS MOSFET has good potential to realize ultra-low power green transistor that is additive to FinFET for performance improvement.

The conventional 1T1C DRAM consumes significant P_{DC} and P_{AC} . The lacking of higher κ material and increased aspect ratio are the difficult challenges for DRAM capacitor. It is important to notice that the ferroelectric high- κ HfZrO pMOSFET can also be used as a capacitor-less 1T DRAM. Good DRAM-like functions of a 5 ns switching time, 10^{12} on/off endurance cycles, and

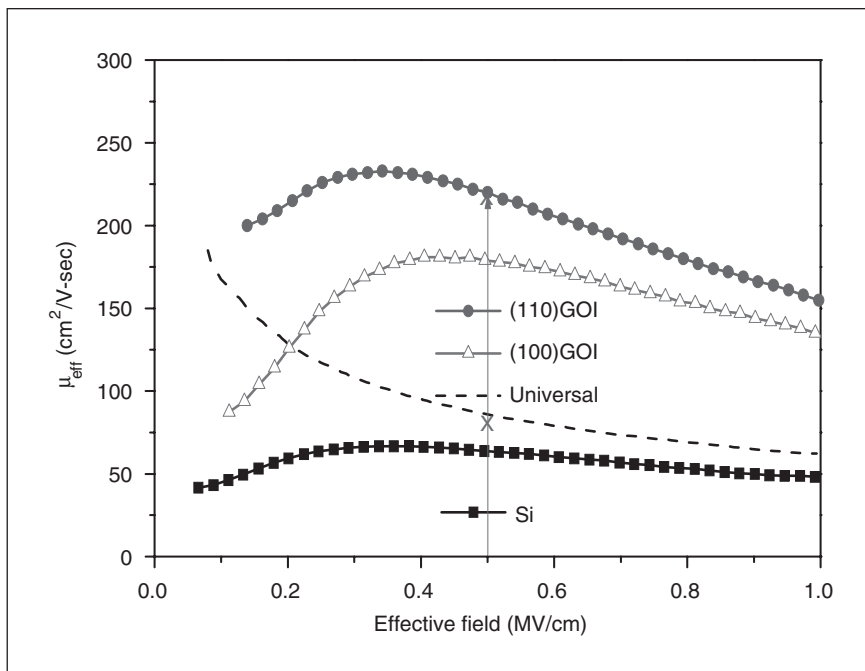


Fig. 3 The $\mu_{\text{eff}}-E_{\text{eff}}$ characteristics of the metal-gate/high- κ /GOI pMOSFETs (data from D. S. Yu, Albert Chin, C. C. Laio, C. F. Lee, C. F. Cheng, W. J. Chen, C. Zhu, M.-F. Li, S. P. McAlister, and D. L. Kwong, "3D GOI CMOSFETs with Novel $\text{IrO}_2(\text{Hf})$ Dual Gates and High- κ Dielectric on 1P6M-0.18 μm -CMOS," IEDM Tech. Dig., pp. 181-184, 2004).

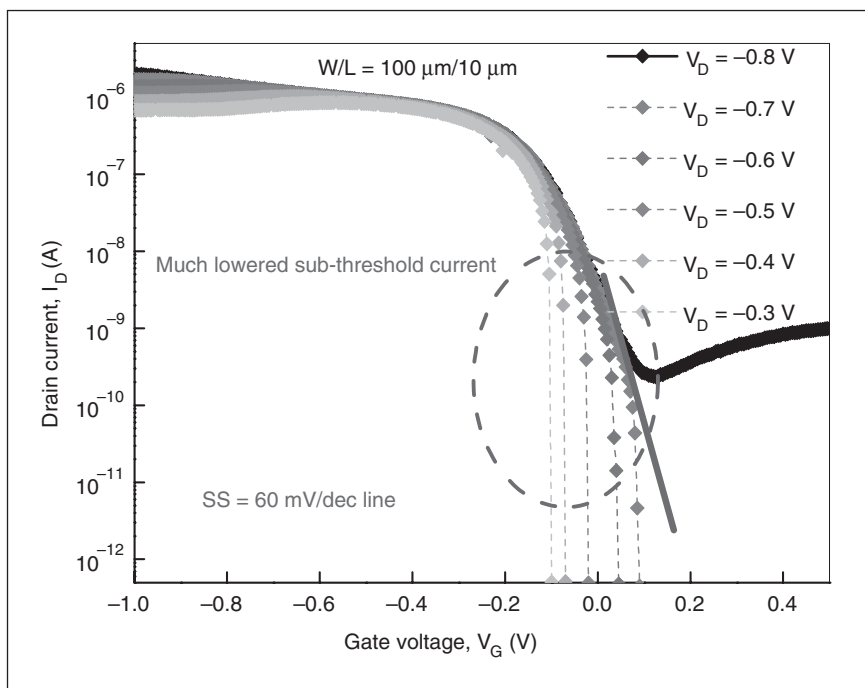


Fig. 4. Measured I_D-V_G characteristics of TaN/HfZrO p-MOSFETs having full process compatibility with metal-gate/high- κ CMOS (data from C. H. Cheng and Albert Chin, "Low-Voltage Steep Turn-on p-MOSFET Using Ferroelectric High- κ Gate Dielectric," IEEE Electron Device Lett., vol. 35, pp. 274-276, Feb. 2014).

30 times on/off retention windows at 5 s and 85°C were achieved. Besides, a simple 1T process and a considerably low off-state leakage of $3 \times 10^{-12} \text{ A}/\mu\text{m}$ were obtained, which are impossible for existing 1T1C DRAM devices. This new device may be the solution for DRAM downscaling into sub-10 nm regime.

In summary, low PDC high- κ gate dielectric CMOS and FinFET have already been successfully implemented in CMOS IC manufacture. Further even lower P_{DC} and P_{AC} Green Electronic Devices may be realized by novel materials, steep turn-on device physics, and ferroelectric effect.

Albert Chin received Ph.D. from University of Michigan and B.S. from National Tsing Hua University. He was with AT&T Bell Labs (89-90), General Electric E-Lab (90-92), Texas Instruments SPDC (96-97), and visiting Professor at National University of Singapore (02-06). He has been a distinguished professor, vice executive officer of diamond project, and deputy director of National Chiao Tung University. He is a pioneer of low DC-power high- κ CMOS & Steep Turn-On CMOS, planar high- κ Flash memory, high mobility Ge-On-Insulator (GeOI) CMOS, low AC-power 3D IC, high RF-power asymmetric-MOSFET, Si fs/THz devices, and resonant-cavity photo-detector. He co-authored >450 papers and 7 "Highly Cited Papers" (top 1% citation). His high- κ CMOS, GeOI, Flash memory, and RF devices were also cited by ITRS. Dr. Chin served as the Subcommittee Chair and Asian Arrangements Co-Chair/Chair of IEDM Executive Committee. He is an IEEE Fellow, Optical Society of America Fellow, and Asia Pacific Academy of Materials Academician. He currently serves as Editor of IEEE Electron Device Letters and IEEE EDS Technical Committee Chair on Electronic Materials.

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TECHNICAL SUMMARY OF 2014 IEEE PVSC CONFERENCE

With more than 1050 presentations in over 100 plenary, oral and poster sessions, the 40th IEEE Photovoltaic Specialists Conference (PVSC) can be called the world's premier event in photovoltaics research, development and engineering. This year the technical program of the conference was outstanding, and featured the presentation of multiple world record efficiencies for various photovoltaic (PV) cell materials.

Three breakthrough records of 25% efficiency and higher were reported for large-area interdigitated-back-contact (IBC) silicon solar cells: 25.6% for a heterojunction cell (K. Masuko, Sanyo/Panasonic), 25.1% (J. Nakamura, Sharp) and 25% (D. Smith, SunPower). Moreover, a copper indium gallium diselenide (CIGS) thin-film solar cell with a 21% record efficiency was presented by Solibro. Solar Frontier, showed a 11.4%-efficient kesterite sub-module with a graded bandgap. Also, in the field of concentrator PV, more information was given by F. Dimroth of Fraunhofer ISE on the 44.7%-efficient 4-junction concentrator III-V solar cell manufactured by wafer bonding.

Two new certified world records for thin-film silicon PV were reported: 11% for single-junction microcrystalline cells (H. Sai, AIST); and 12.6% for micromorph tandem cells (M. Boccard, EPFL, now at ASU). Continued success was reported in the area of organic photovoltaics (OPV), with a world record 10.6% efficiency for a single-junction polymer-fullerene OPV cell (A. Facchetti, Northwestern Univ./Polyera) and >15% efficiency for a perovskite solar cell (M. Nazeeruddin, EPFL). 20% indoor OPV efficiency was presented by K. Knops of IMEC. Interesting joint sessions were held on perovskite solar cells, III-V on Si epitaxy, next-generation hot-carrier and intermediate-band solar cells (J. Adams, Microlink).

In the area of characterization, new work on luminescent imaging was discussed to quantitatively understand the spatially resolved recombination, shunt, and series losses in cells and modules (B. Michl, FhG-ISE and others). A new method, electron channeling contrast imaging (ECCI), was presented for using readily available scanning electron microscopy (SEM) to obtain the same type of crystal dislocation imaging as in transmission electron microscopy (TEM) over

large areas, approximately 10 times more rapidly, and without the arduous sample preparation required by TEM (S. Carnevale, Ohio State).

In the area of PV systems, a new draft standard addressing the complex task of system energy performance testing was presented, as well as a PV power plant case study (S. Kurtz, NREL), and new testing procedures and techniques for evaluating advanced inverters as they are expected to operate in future PV systems: IEEE 1547.1 and UL1741 (A. Hoke, NREL). Novel power-modification electronics received a great deal of attention, such as micro-inverters, module-level power optimizers and sub-module string maximum-power-point trackers (MPPT) (C. Deline, NREL) (T. Peshek, Case Western Univ.). Promising news for the reliability of PV systems was presented: data from almost 50,000 PV systems showed that the vast majority (90%) of PV systems had actual performance in the field within 90% of their projected performance (D. Jordan, NREL).

Angèle Reinders
2014 PVSC Technical Program Chair
University of Twente
The Netherlands

2014 ESSDERC/ESSCIRC

The 44th European Solid State Device Research Conference (ESSDERC) and the 40th European Solid-State Circuits Conference (ESSCIRC) will take place in Venice Lido, Italy, from Monday through Friday September 22–26, 2014. The aim of ESSDERC and ESSCIRC is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The increasing level of integration for system-on-chip design made available

by advances in silicon technology is, more than ever before, calling for a deeper interaction among technologists, device experts, IC designers, and system architects. While keeping separate Technical Program Committees, ESSCIRC and ESSDERC are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the

scheduled parallel sessions, regardless to which conference they belong, and to participate to the joint opening reception and gala dinner events.

ESSCIRC/ESSDERC 2014 joint plenary talks are: "A Semiconductor Memory Manufacturing and Development Perspective" by Scott DeBoer of Micron, USA; "Terahertz Electronics: The Last Frontier" by Thomas H. Lee of Stanford University, USA; "Automotive Electronics: Application & Technology Megatrends" by Fabio Marchiò,

STMicroelectronics, Italy; "How Chips Helped Discover the Higgs Boson at CERN" by Walter Snoeys, CERN, Switzerland; "Logic Scaling Beyond 10 nm, a Power-Performance-Area-Cost Trade-off" by An Steegen, IMEC, Belgium and "Tremendous Benefits of Moore's Law Have Yet to Come" by Sehat Sutardja, Marvell Semiconductor, USA.

Apart from these, 3 plenary talks at ESSDERC include "FinFET vs. FD-SOI: Technology and Design Issues" by Bruce Doris, IBM, USA; "Energy Efficiency and Conversion in 1D and 2D Electronics" by Eric Pop, Stanford University, USA and "Bionic Skins Using Flexible Organic Devices" by Takao Someya, University of Tokyo, Japan. Three plenary talks at

ESSCIRC are "Blocker Tolerant Software Defined Receivers" by Hooman Darabi of, Broadcom, USA; "Emerging ADCs" by Un-Ku Moon, Oregon State University, USA and "Ultra-Low Power Short Range Radios" by Kathleen Philips, IMEC-Holst Centre, The Netherlands.

The first day of the conference is dedicated to Six different Tutorials—two full day and four half day events in the areas of CMOS technology at the nm scale era, Power Management for SoCs, RRAM: from technology to applications, 3D: from technology to applications, High performance amplifier and Phase Noise: from fundamentals to circuit aspects. Conference technical sessions span

the next three days in which Plenary talks and the contributed papers are included. The last day of the conference is filled with Four Workshops in the areas of *Beyond-CMOS for advanced More Moore and More than Moore applications*, *MOS-AK: Over Two Decades of Enabling Compact Modeling R&D Exchange*, *Status of the GaN and SiC based device development* and *Marie Curie ARWC*.

For details about ESSDERC/ESSCIRC 2014 visit: <http://www.esscerc-essderc2014.org/>

Gaudenzio Meneghesso
2014 ESSDERC/ESSCIRC General Chair
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2014 ISPSD SUMMARY

The 26th International Symposium on Power Semiconductor Devices & ICs (ISPSD'2014) was held from June 15–19, 2014, in Waikoloa, Hawaii. The mission of this event is to cultivate an international forum for professionals in the field of power semiconductor devices, power integrated circuits, and related fields to meet regularly and exchange ideas and developments in the field and promote the growth of this field. Sponsorship of ISPSD has been provided by the IEEE Electron Devices Society (EDS) and co-sponsorship has been provided by IEEE Power Electronics Society (PELS) and IEE Japan (IEEJ).

This year's symposium attracted 355 attendees, with fairly uniform distribution of attendees from North America, Japan, Europe and other regions. The program included a one-day short course with lectures on integrated voltage regulators, smart electronics (GaN & CMOS), photovoltaic systems, devices for hybrid electric vehicles, ESD protection, and SiC switches. The single-track conference spanned four days and featured three invited plenary talks given by experts from IBM (USA), TMEIC (Japan) and



The ISPSD 2014 welcome reception at the Hilton Waikoloa included a beautiful Hawaiian sunset

TU Munich (Germany), 48 oral presentations, and 62 poster presentations. Papers were divided into the major categories of Low Voltage, High Voltage, Wide Bandgap, Integrated Power, and Packaging. Thanks to the record high 235 submissions, a low acceptance ratio of 45% was achieved. There was a notable increase in the number of Wide Bandgap papers submitted, underscoring the growing activity in this area.

The Charitat Award for the best paper by a young researcher (< 30 years

of age) was presented to Rina Tanaka for the paper entitled "Impact of Grounding the Bottom Oxide Protection Layer on the Short Circuit Rugedness of 4H-SiC Trench MOSFET."

The next ISPSD will be held in May 2015 in Hong Kong. See www.ispsd.org for more information.

Don Disney
2014 ISPSD General Chair

Jan Vobecky
Editor EDS Newsletter

UPCOMING TECHNICAL MEETINGS

2014 IEEE INTERNATIONAL INTEGRATED RELIABILITY WORKSHOP (IIRW)

The 2014 IEEE International Integrated Reliability Workshop (IIRW), sponsored by the IEEE Reliability Society and the IEEE Electron Devices Society, will be held at the Stanford Sierra Conference Center on the shores of Fallen Leaf Lake near South Lake Tahoe, California, October 12–16, 2014. This workshop provides a unique forum for open and frank discussions of all areas of reliability research and technology for present and future semiconductor applications.

Some of the highlights of this year's technical program will include:

- A keynote speech "Accelerated Testing—How fast is too fast?" given by J.W. Mc Pherson
- A strong collection of invited speakers including (but not limited to): Umberto Celano (IMEC)—Scanning Probe Tomography; Christian Schlunder (Infineon)—BTI; Sean King (Intel)—Low-k Dielectrics and Cu Interconnects; Aivars Lelis (Army Research Lab)—Power Devices; Chris Hinkle (UT Dallas)—TMD materials (MoS₂), Dmitry Veksler (Sematech)—RRAM devices; Jacopo Franco (IMEC), BTI Reliability of High Mobility Channel Devices; Brian Downey (NRL), III-V Failure Devices.
- A tutorial program (organized by Andreas Aal, Volkswagen, and, Bill McMahon, Globalfoundries) will cover many hot reliability topics including (but not limited to) FEOL and advanced non-volatile memories, the reliability issues induced by packaging-IC interaction, the reliability constraints for the robust design of electronic automotive systems, the reliability of power devices (power MOSFET, GaN devices) and III-V technologies.



View from the ski dock at the Stanford Sierra Conference Center. The Stanford Sierra Conference Center provides lodging, meals and meeting facilities as well as excellent recreation including hiking in the Desolation Wilderness and boating on Fallen Leaf Lake

The IIRW is also an excellent forum to present new and original technical works. Hot reliability topics for this year's workshop include: SiGe and strained Si, III-V, SOI, high-k and nitrided SiO₂ gate dielectrics, reliability assessment of novel devices, organic electronics, emerging memory technologies (RRAM etc.) and future "nano"-technologies, NEMS/MEMS, photovoltaics, transistor reliability including hot carriers and NBTI/PBTI, Cu interconnects and low-k dielectrics, product reliability and burn-in strategy, impact of transistor degradation on circuit reliability, reliability modeling and simulation, optoelectronics, single event upsets, as well as the traditional topics of wafer level reliability (WLR) and built-in reliability (BIR). The Call for Papers can be found at the web address (www.iirw.org). The abstract submission deadline is July 11, 2014. Contact the Technical Program Chair, Jason Ryan, NIST (jason.ryan@nist.gov) for further details. Also, visit www.iirw.org for continued updates about the conference. Also note that all attendees have the opportunity to present a "walk-in" poster of their latest work. This is a great way to share that new

project you are working on and to get world-class feedback.

IIRW is fairly different from a typical technical conference. Located 6000 ft. high in the Sierra Nevada Mountains, the Stanford Sierra Conference Center provides an ideal atmosphere for a relaxing yet informative workshop. Nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake, attendees stay in cabins furnished in the rustic style of an alpine resort. All cabins have decks with magnificent views of Fallen

Leaf Lake and the surrounding Sierra peaks. Comfortable, informal dress is encouraged, affiliations are downplayed, and meals are provided family-style in the lodge dining room.

All aspects of the workshop, including the physical isolation of the venue, the absence of distractions such as in-room phone and televisions, and the format of the technical program encourage extensive interaction among the workshop attendees. Such opportunity is seldom available at most other conferences. Participants spend their evenings at poster sessions, discussion groups, and special interest groups, all complemented with refreshments and snacks. The evening moderated discussion groups provide a forum with unparalleled access to world experts to discuss a wide array of relevant reliability issues. Often these discussions lead to the formation of a smaller special interest group, whose discussions extend long after the conclusion of the workshop.

The technical program is purposely kept open for Wednesday afternoon to allow attendees to enjoy a variety of the outdoor activities which the Stanford Sierra Conference

Center location has to offer. These include hiking, sailing or kayaking, walking, or simply continuing that intriguing conversation from the night before. This free afternoon is a great way to not only network, but also to build long-lasting friendships.

Additional information about the workshop is available on the IIRW

website at www.iirw.org, or by contacting Tibor Grasser of TU Wien, 2014 IIRW General Chair, (grasser@iue.tuwien.ac.at) Note: If you want to take part in this event, please register early as space at the Stanford Sierra Conference Center is limited to roughly 120 attendees and the workshop has sold out in the past.

On behalf of the 2014 IIRW Committee, I look forward to meeting you in Lake Tahoe!

Luca Larcher
2013 IIRW Communications Chair
University of Modena and
Reggio Emilia
Reggio Emilia, RE, Italy

2014 IEEE COMPOUND SEMICONDUCTOR IC SYMPOSIUM (CSICS)

The 2014 IEEE CSICS will be held October 19–22, at the Hyatt Regency La Jolla at Aventine located in San Diego, California, USA.

CSICS is a comprehensive technical conference and exhibition, with coverage of GaN, GaAs, InP, SiGe, and nanoscale CMOS technologies and their application to microwave/mm-wave, THz, analog mixed signal, power conversion, and optoelectronic integrated circuit design. After 36 years of refinement, CSICS has become the premier symposium at which to present innovations demonstrating extreme results in the areas of circuit switching speed, RF frequency of operation, RF output power, PA efficiency, and noise performance. CSICS also showcases the very latest advances in emerging semiconductor device technology, modeling and manufacturing.

The symposium consists of a three-day dual track technical program, two short courses, a primer course, and a technology exhibition. The technical program includes 60–70 high quality papers and 4 topical panel sessions. This year, CSICS is proud to announce 18 internationally renowned invited speakers, notably: Ichiro Fujimori (Broadcom), Joel Harmann (STM), Daniel Green (DARPA/MTO), Hervé Blanck (UMS), Paul Saunier (TriQuint), Peide Ye (Purdue), Augusto Gutierrez (NGAS), Craig Appel (CISCO), and Mark Rodwell (UCSB). Among the

interesting topics they will be covering are Multi-Gb/s wireline TXRX, FDSOI CMOS, heterogeneous integration, the future of the III–V's in Europe, GaN HEMTs, Graphene FETs, and Si-photonics.

CSICS offers two in-depth short courses on Sunday, October 19th. The first course is GaN HEMT Device Modeling and will be presented by leading experts Ilcho Angelov (Chalmers), Robert Trew (NCSSU), and David Root (Agilent). Comprising three 100 minute lectures, this course details the contending methods used to model GaN HEMT devices: equivalent circuit, physics-based, and behavioural. The basis, merits and limitations of each one will be examined closely with comparisons made to prior GaAs models. The course will also cover parameter extraction and fitting techniques and should prove invaluable for anyone involved in GaN technology and circuit design.



The second short course, Fundamentals of Power Conversion and Envelope Tracking, will be taught by Dragan Maksimovic (UC Boulder) and Donald Kimball (MaXentric). Enveloping tracking (ET) is

an RF amplifier design approach used to optimize system efficiency for complex modulation schemes. The course starts with fundamentals of power conversion, which is a vital aspect of the approach. It then explores the characteristics and implementation of ET amplifiers. The material is covered in two 90 minute lectures.

On Sunday evening, Waleed Khalil (Ohio State) will teach an expanded Primer Course on Si RFIC design. This 3.5 hour lecture is intended for participants of all technical backgrounds who wish to learn or refresh their understanding of the fundamentals of designing the principal circuit building blocks in radio and radar SoCs.

Among the blocks covered are PAs, LNAs, Mixers, VCOs, as well as integrated passives, with examples drawn from both CMOS and SiGe technology. The primer is an excellent way to start the symposium and is guaranteed to enhance attendee appreciation of the technical program.

For registration and up-to-date information please visit



HYATT REGENCY LA JOLLA AT AVENTINE

the CSICS website at www.csics.org. Further questions may be addressed to the Symposium Chair: Douglas S. McPherson, phone:

+1-613-670-3371, e-mail: dmcphers@ciena.com.

We hope you can attend, 2014 IEEE CSICS Organizing Committee.

Brian Moser
2014 CSICS Publicity Chair
RFMD
Greensboro, NC, USA

2014 IEEE BIPOLAR/BI-CMOS CIRCUITS AND TECHNOLOGY MEETING (BCTM)

On behalf of the IEEE BCTM'14 Executive Committee, we are honored and delighted to invite you to the 2014 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) at the beautiful Coronado Island, San Diego, California, September 28–October 1, 2014. We invite you to participate at the 2014 BCTM where the highlights include:

- a keynote address by **Dean of College of Engineering and Professor Larry Larson of Brown University** on "Advances in the highly efficient RF Power Amplifiers using Bipolar Technologies: devices, circuits and systems"
- a day-long short course on "**SiGe BiCMOS Circuit Design for Wireless, Wireline and Radar Applications**", where Dr. Sean Nicolson from Broadcom will discuss "System specification and SiGe BiCMOS Circuit Design for W-Band Cellular Backhaul;" Prof. John Long on "The Design of RF Transceiver Front-Ends in SiGe BiCMOS;" Prof. Gabriel Rebeiz on "SiGe BiCMOS Circuit Design for Phase Array Radar Applications;" and Prof. Sorin Voinescu on "Nanoscale SiGe BiCMOS technology and circuit design for 64-125 GBAUD wireline and fiber optics applications."
- a forward-looking **Emerging Technologies Session** with invited speakers from Dr. Hagen Klauk (Max Planck Institute for Solid State Research) on "Low-Voltage Organic Field-Effect Transistors for



Donald Y.C. Lie
General Chair
Texas Tech
University



Prof. Jean-Baptiste
Begueret
Technical Program
Chair
University of Bordeaux

Flexible Electronics;" Prof. Zhen-qiang (Jack) Ma (University of Wisconsin-Madison) on "Radio Frequency Flexible Electronics: Transistors and Passives;"

Dr. Milton Feng (University of Illinois) on "Transistor Laser for Optical Interconnect and Photonics Integrated Circuits;" and Dr. Supratik Guha, Director Physical Sciences Department, IBM Thomas J. Watson Research Center on "Technologies for future information processing systems."

- invited papers exploring advances in process technology, device physics, wireless design, analog/mixed-signal, and modeling
- technical papers covering the latest advances in physics, design, performance, fabrication, characterization, modeling, and application of Si/SiGe/SiC bipolar, BiCMOS, and GaN ICs
- a luncheon & plenary speaker from Prof. Todd Martz: Scripps Institution of Oceanography, UCSD on the latest research in oceanography

- an evening dinner banquet at the beautiful Coronado Bay

The IEEE BCTM is a forum for technical communication focused on the needs and interests of the bipolar and BiCMOS community. Papers covering the design, performance, fabrication, testing and application of bipolar and BiCMOS integrated circuits, bipolar phenomena, and discrete bipolar devices are solicited. A Special Issue of the *IEEE Journal of Solid-State Circuits* will include selected papers from BCTM 2014.

General Contact Information

Visit the conference website: www.ieee-bctm.org, or contact: Catherine Shaw, Conference Manager, Phone 1-732 501-3334, e-mail: cshaw.mpevents@gmail.com

The IEEE BCTM is the world's premier forum focused on the needs and interests of the bipolar and BiCMOS community. If you are interested in leading edge bipolar/BiCMOS devices and technology, circuits, and applications, as well as networking with experts in these areas, please kindly join us this year at the beautiful Coronado Island at San Diego, California, USA!

Donald Y.C. Lie
2014 BCTM General Chair
Texas Tech University

Jean-Baptiste Begueret
2014 BCTM Technical Program Chair
University of Bordeaux

SOCIETY NEWS

PRESIDENT'S MESSAGE



Albert Wang
EDS President,
2014-2015

Dear Fellow EDS Members,

Indeed time flies. By the time you see this message, I will have been cheer-leading the EDS volunteer activities for half a year! With a 10K-strong army of

volunteers and members standing with me, never try to convince me to calm down please!

EDS faces opportunities and challenges now more than ever. Everything, especially technology, is changing so rapidly today, if we do not have our "sensors" working 24/7 and make ourselves highly adaptive, EDS could be eventually another dinosaur in a museum someday. Fortunately, many volunteers are well aware of it and have been enthusiastically offering their observations, comments and suggestions to ensure that EDS will remain on the forefront of any and all electron devices topics.

For example, Prof. Rajendra Singh of Clemson University and Dr. Krishna Shenai of Argonne National Laboratory offered their observations on recent development in area of solid-state power electronics and their power applications, which have landed on the Power Devices and ICs Committee chaired by Dr. Don Disney for further discussions. This and other emerging sub-topics related to the Field of Interests of EDS are coordinated by the VP of Technical Committees and Meetings, Prof. Leda Lunardi. With the enthusiastic involvement of EDS volunteers and dedicated efforts of our technical committees, I am confident that EDS is maintain its technical preeminence down the road.

Another example of the challenges and opportunities before the Society comes from our new Open-Access (OA) journal, the Journal of Electron Devices Society (JEDS). JEDS was launched in 2013 to answer the general call for a quick and open online publication venue with high-quality. Although we are facing a big challenge in terms of establishing the global awareness of JEDS, we certainly are on track to catch the emerging trend of online OA mechanism. To help get the word out about JEDS, and to stimulate submissions, there have been extensive discussions at the EDS Presidents Strategic Meetings, the Publication Committee, and the Editors-in-Chief (EiC) corps led by Dr. Bin Zhao, VP for Publications and Products and Prof. Renuka Jindal, EiC of JEDS. A list of action items has been adopted for the JEDS Editorial team to execute. This action plan includes:

- Identifying new hot areas where qualified Editor candidates around the world are needed.
- Catching the emerging, sizzling topics for possible Special Issues as a quick venue for top-tier experts to present their discoveries and opinions on any new device-related subjects
- Considering Special Issues for selected conferences sponsored by EDS.
- Addressing emerging subjects for comprehensive and up-to-date technical reviews by world-class researchers, etc.

While it still seems to be a "Bingo" business to run a brand new journal, we are action-oriented and not afraid of taking any challenge. I am confident that, with all the big efforts planned, JEDS will be a success story in the years ahead.

Membership development is certainly the core of EDS business, while delivering the right products to our members has always been the job focus of the ExCom team. Under Prof. Mikael Ostling, VP for Membership and Services, and Dr. Fernando Guarin, the chair for the Education Committee, the popular Webinars and Tutorials program is being enhanced and EDS members will enjoy a list of quality webinars and tutorials this year. On the Regions and Chapters front, our VP, Prof. Xing Zhou, has been working with all local chapters and activists to boost the EDS programs around the globe. At the time of this writing, a petition for a new Romania EDS chapter is moving into the approval channel. In Region 9, the biennial ICCDCS meeting and MQ were just successfully completed.

And, let's never forget about the students, our future members and really the future of EDS. The IEEE has recently relaunched the Young Professionals (formerly G.O.L.D.) community. EDS is fortunate to have Daniel Mauricio Camacho of Intel to serve as our YP Chair, spearheading our many YP-related activities such as the networking event slated for our Photovoltaics Specialists Conference this Spring. My warm call to all professors in the EDS community around the world is to join Daniel in this effort. You have so many graduate students conducting electron devices research in your Labs, but is there a student chapter in your school? If not, take action now please. The obligation of a professor is well beyond just advising students on research. You ought to care about the students' future career, and getting your students involved in EDS activities now will benefit them forever. You know it!

Lastly, another BIG thing just up and running is the EDS Mission Fund, which is recently established to enhance the humanitarian, educational and research initiatives of EDS. All EDS friends can take this opportunity to contribute directly to EDS-critical activities. One of the important things to

make the Fund successful is to show the potential donors a solid initiative plan of using the fund, for which, any good ideas are welcome from EDS volunteers. For more information, and to donate, please visit the EDS website.

Before closing my message, I would like to reiterate that

the well-being of EDS relies on volunteerism. So please, come forward to do anything that you think will make our beloved EDS better and stronger!

*Sincerely,
Albert Wang*

from sunny Southern California

MESSAGE FROM VP REGIONS AND CHAPTERS



*"Joe" Xing Zhou
EDS Vice-President
of Regions/Chapters*

Dear fellow EDS volunteers and members,

In my role as Vice-President of Regions/Chapters (R/C), and in light of the recent Constitution & By-law changes and re-alignment of

ExCom and VP responsibilities, I would like to take this opportunity to share my thoughts in promoting and enhancing regional/chapter activities. Being actively involved as a member of the EDS R/C committee since 2002 and serving as Vice-Chair and Chair of the SRC-AP in 2005–2012, as an active Distinguished Lecturer (DL) since 2000, also as an executive committee member of the REL/CMPT/ED Singapore Chapter since 2002, I have first-hand experiences in the needs and ideas at various chapter, region, and society levels. Members and chapters are the grass-roots of the Society. As a volunteer-led and volunteer-driven organization, our Society's mission is to foster professional growth of its members and to enhance visibility in the field. We have ~180 chapters in 10 regions, and we spent \$110,000 annual budget in supporting various chapter/regional activities such as chapter subsidy, SRC, mini-colloquia (MQ) and DL programs. How can the budgets be best utilized in promoting regional/chapter activities, and better serve members and reward volunteers? With re-alignment of VP responsibilities, we should have a

holistic planning on various budgets to optimize utilization and to evaluate "return on investment."

Our chapters and their needs have a large variety; some have a long history and financially strong and others are new or not as active and in need of support. Chapter subsidy as well as SRC and MQ/DL programs are meant to support chapters and members, while proactive promoting and liaising with various programs is the key. Chapter chairs/executives are encouraged to reach out to SRC/EDS levels for financial support in organizing technical activities while leveraging on other resources. They are also reminded to report such organized events to the Newsletter as well as filing the L31 reports. The SRC and R/C committee can play an active role in helping chapters and linking MQ/DL resources. The Chapter of the Year program is another way to encourage active participation and recognition of volunteers.

Our MQ and DL programs, now under the purview of VP-R/C, have been very successful. DLs are our "messengers" to serve our chapters and members and MQs are coordinated "group DLs." There are various needs in MQ/DL sponsorships depending on chapters; however, something in common is the coordination and leveraging on resources. I would like to call for individual chapter executives and DLs to be proactive in coordinating these activities so as to make the best use of available resources. For example,

chapters (with help from SRC and R/C committee) should look out for those DLs participating in nearby conferences and inviting them for a "side trip," while DLs should try to contact local chapters to offer DL talks when traveling to different regions. MQ organizers should plan those events ahead of time, including joint MQs together with chapters in the region. We strongly encourage resource leverage in organizing MQ/DL activities, including budget sharing from MQ/DL/SRC funds as well as contributions from hosting chapters/institutions. We will work towards general guidelines in MQ/DL budget approval and post evaluation.

Last but not the least, our SRC chairs/vice-chairs and R/C committee members should play a more active role in coordinating and initiating regional activities. They have more authority as well as more responsibilities, serving the roles of chapter mentors in the respective regions. They should proactively link chapters and DLs, organize regional (joint) MQs, and even propose incentives and recognition for volunteers in their regions. Together, at various chapter, region, and society levels, we hope to create such an atmosphere of volunteerism to better serve our members and EDS community. I look forward to working with SRC's and R/C committee to better service our members and reward our volunteers.

*"Joe" Xing Zhou
Nanyang Technological University
Singapore*

MESSAGE FROM EDITOR-IN CHIEF



M K Radhakrishnan
Editor-in Chief
EDS Newsletter

Dear Readers,
While reading the April 2014 issue of the Newsletter, all of you would have noticed that we are introducing some new sections. We have Technical Briefs, Young Profession-

als and Chapter News as new sections and we will continue to have them in future issues along with all other information and Society news. However, as the Editorial team we would like to get the readers' feedback. All the society members are welcome to give their feedback about the articles

and information in the Newsletter and your views about the Society. You may write to edsnewsletter@ieee.org.

Again, we plan to expand the Newsletter as a media to help the member professionals not only in technical front, but in networking and communication. As a first step in this direction, as the Editor-in Chief, I request our young graduates to write their professional experience and expectations to the Young Professionals column. We would like to include such articles in the Newsletter, if they are found noteworthy for other members. Please include your affiliation and IEEE membership details. Also, if any of the members find that an important technical breakthrough is

happening and goes unnoticed in our field, you can inform it to the newsletter team and we will be happy to get a consolidated view about such happenings and publish. Many of our members and Chapters are engaged in humanitarian and societal activities and helping hands, which get unnoticed. We would like to provide visibility of such services to the society. Again, I urge Chapters and members to communicate about all such ventures to the Newsletter. Please e-mail to: edsnewsletter@ieee.org

M K Radhakrishnan
Editor-in Chief, EDS Newsletter
NanoRel, Bangalore, India
e-mail: radhakrishnan@ieee.org

EDS BOARD OF GOVERNORS MEETING HELD IN STOCKHOLM

Hard work and good times went hand-in-hand at the 2014 mid-year EDS Board of Governors (BoG) Meeting Series in Stockholm, Sweden. This meeting was hosted and organized by EDS Vice President of Membership, Mikael Ostling, and his outstanding team at the KTH Royal Institute of Technology, including Gunilla Gabriellson, Sam Vaziri, Anderson D. Smith, and Babak Taghavi. The weekend's events kicked off on

Friday afternoon with a meeting of the EDS presidents and executive staff. Several important committee meetings took place on Saturday, including Fellow Evaluations, Publications, Education & Membership, Newsletter, Regions/Chapters & Region 8 Chapters, and ExCom. The work culminated on Sunday with the EDS Board of Governors meeting.

Spirited discussions abounded in the all-day BoG meeting, which

resulted with the finalization and approval of operating charters for all 10 of EDS's vital standing committees. Adoption of these charters is the next step in the reorganization of the society's governance structure, launched in 2013 (by then President Paul Yu) which will help foster greater flexibility, transparency, and, most importantly, opportunities for vital member engagement in the life and work of the society. As noted by Albert Wang, EDS President, "With the Charters established for all Standing Committees, for the first time and in full compliance with the Constitutions and Bylaws, the EDS operations will be more efficient and transparent to the 10000-plus members."

In addition, the weekend's work resulted in the passing of key items related to the EDS operating budget for 2015 and the nomination review for the 2014 IEEE Fellows candidates submitted to EDS. Our deepest thanks go to EDS Fellow Evaluations Committee Chair, Leda Lundardi, for leading this crucial effort.



EDS Region 8 Chapters Meeting Attendees – KTH Main Campus (May 24, 2014)

With two and half days of back-to-back meetings completed, the attendees were treated to a very special and well-earned event organized by our host, Mikael. The BoG dinner was held at Stockholm's incredible Vasa Museum, and featured a private tour of the world's best kept 17th century warship, the *Vasa*, and a harbor-side dinner. And despite the warm sunshine and perfect weather, things managed to cool down to below freezing at the informal after party held at Stockholm's Ice Bar where everything (bar, furniture, and glassware) is made entirely of ice!

All in all, it was an amazing weekend which not only advanced the society's vital work but also provided attendees with opportunities to meet new colleagues, strengthen ties with



EDS BoG Dinner Attendees – Vasa Museum (May 25, 2014)

old ones, and enrich and energize their professional lives. We extend our deepest thanks and gratitude to

Mikael and his team for their hard work and dedication to the society. Here's to you: Skoal!

CALL FOR NOMINATIONS— EDS BoG (FORMERLY AdCom) MEMBERS-AT-LARGE

The IEEE Electron Devices Society invites nominations for election to its Board of Governors—BoG (formerly AdCom). The next election will be held after the BoG meeting on Sunday, December 14, 2014. This year, eight out of the twenty-two members will be elected for a 3-year term, with a maximum of two consecutive terms.

EDS recently approved a pilot program for one of the eight BoG Member-at-Large seats this year to be elected via the entire EDS membership. All nominees must choose to participate in either the election by EDS membership or the election by the BoG. There must be a minimum of two nominees for the seat elected by membership. If there are less than two nominees for the seat, an election by EDS membership will not be held and the candidate will be moved to the election by the BoG. All electees begin their term in office on January 1, 2015. The nominees need not be present to run for the election. Self-nominations are allowed.

Any EDS member who has previously participated in EDS activities as an EDS Officer, Vice-President, Standing & Technical Committee Chairs or Members, Publication Editor & Chapter Chair for minimum of one year is eligible to be nominated. The electees are expected to attend both BoG Meetings every year. While the December meeting is organized in connection with the IEEE International Electron Devices Meeting, the mid-year meeting is frequently held outside the US. Partial travel support is available to attend both of these meetings.

All nominees must be endorsed by one BoG member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current BoG Members-at-Large. It is the responsibility of the endorser to make sure that, if elected, the nominee is willing to actively serve in the position as a BoG member. In the unlikely event that a nominee must withdraw their name from the election ballot, they must do so by November 1, 2014.

Please submit your EDS BoG nomination by August 1, 2014. Also, all endorsements letters should be sent to the EDS Executive Office, Laura J. Riello via e-mail: l.riello@ieee.org by August 1, 2014. If you have any questions, please feel free to contact Laura Riello (l.riello@ieee.org) with a copy to me at p.yu@ieee.org.

*Paul Yu
EDS Chair of Nominations & Elections
University of California at San Diego
San Diego, CA, USA*

EDS BOARD OF GOVERNORS MEMBERS-AT-LARGE ELECTION PROCESS



Paul Yu
EDS Chair of Nominations & Elections

The Members-at-Large (MAL) of the EDS Board of Governors are elected for staggered 3 year terms, with a maximum of two consecutive terms. The 1993 Constitution and Bylaws changes mandated increasing the number of elected MAL from 18 to 22, and required that there be at least two members from each of the following geographic areas: Regions 1–7 and 9; Region 8; Region 10. In 2003, EDS made changes to its Constitution and Bylaws to require that at least one elected BoG member is a Young Professional (YP – formerly Gold member). A Young Professional member is defined by IEEE as a member who graduated with his/her first professional degree within the last fifteen years. It is also required that there be at least 1.5 candidates for each opening.

EDS recently approved a pilot program for one of the BoG Member-at-Large seats each year to be elected via the entire EDS membership. All nominees must choose to participate in either the election by EDS membership or the election by the BoG. There must be a minimum of two nominees for the seat

elected by membership. If there are less than two nominees for the seat, an election by EDS membership will not be held and the candidate will be moved to the election by the BoG. All electees begin their term in office on January 1, 2015. The nominees need not be present to run for the election. In 2014, eight positions will be filled.

The election procedure begins with the announcement and Call for Nominations in the *EDS Newsletter*. The slate of nominees is developed by the EDS Nominations Committee and includes the noncommittee and self-nominations received. Nominees are asked to submit a two page biographical resume and an optional 50 word personal statement in a standard format. The election for the one BoG seat voted on by the EDS membership will be done using Vote Net. Vote Net is a web based tool that allows members the opportunity to cast their ballots electronically. An e-announcement will be sent to those EDS members who have email addresses in the IEEE database prior to the election launch date. It will give the members an opportunity to indicate their preference to receive an electronic or paper ballot. By default, paper ballots are automatically printed and mailed to EDS members without email on file as well as to those that have indicated they prefer not to receive election material electronically

(based upon the communication preference in their member profile).

Any EDS member who has previously participated in EDS activities as an EDS Officer, Vice-President, Standing & Technical Committee Chair or Member, Publication Editor & Chapter Chair for minimum of one year is eligible to be nominated. All nominees must be endorsed by one BoG member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current BoG Members-at-Large. Self-nomination is allowed. Endorsers can send a brief email to Laura Riello stating that they would like to endorse the candidate. Please note that there is no limit to the number of candidates that a full voting BoG member can endorse.

Nominations are closed after August 1, 2014, and the biographical resumes and endorsement letters are distributed to the ‘full’ voting members of BoG prior to the December BoG meeting. The election is then held after the conclusion of the meeting.

Paul Yu
EDS Chair of Nominations & Elections
University of California at San Diego
San Diego, CA, USA

IEEE ANNUAL ELECTION – DID YOU VOTE?

This is a reminder for EDS members to vote in the 2014 IEEE Annual Election for the following positions and candidates.

Listed below are the positions and candidates that will appear on the 2014 IEEE Annual Election ballot.

Position	Candidate
IEEE President-Elect, 2015	Frederick C. Mintzer (Nominated by IEEE Board of Directors) Barry L. Shoop (Nominated by IEEE Board of Directors)
IEEE Division I Delegate – Elect/Director-Elect, 2015	Renuka P. Jindal (Nominated by IEEE Division I) Rakesh Kumar (Nominated by IEEE Division I) Maciej J. Ogorzalek (Nominated by IEEE Division I)

Position	Candidate
IEEE Region 2 (Eastern USA) Delegate-Elect/Director-Elect, 2015-2016	Carole C. Carey (Nominated by IEEE Region 2) Katherine J. Duncan (Nominated by IEEE Region 2)
IEEE Region 4 (Central USA) Delegate-Elect/Director-Elect, 2015-2016	Bernard T. Sander (Nominated by IEEE Region 4) Hamid Vakilzadian (Nominated by IEEE Region 4)
IEEE Region 6 (Western USA) Delegate-Elect/Director-Elect, 2015-2016	Kathleen A. Kramer (Nominated by IEEE Region 6) Sundaram K. (S.K.) Ramesh (Nominated by IEEE Region 6)
IEEE Region 8 (Europe, Middle East and Africa) Delegate-Elect/Director-Elect, 2015-2016	Margaretha A. Eriksson (Nominated by IEEE Region 8) Magdalena Salazar-Palma (Nominated by IEEE Region 8)
IEEE Region 10 (Asia and Pacific) Delegate-Elect/Director-Elect, 2015-2016	Kukjin Chun (Nominated by IEEE Region 10) ChunChe (Lance) Fung (Nominated by IEEE Region 10) Stefan G. Mozar (Nominated by IEEE Region 10)
IEEE Standards Association Board of Governors Member-at-Large, 2015-2016	Dennis B. Brophy (Nominated by IEEE Standards Association) Mark Epstein (Nominated by IEEE Standards Association) Philip C. Wennblom (Nominated by IEEE Standards Association)
IEEE Standards Association Board of Governors Member-at-Large, 2015-2016	Alexander D. Gelman (Nominated by IEEE Standards Association) Oleg Logvinov (Nominated by IEEE Standards Association) Glenn W. Parsons (Nominated by IEEE Standards Association)
IEEE Technical Activities Vice President-Elect, 2015	Jose M.F. Moura (Nominated by IEEE Technical Activities) Douglas N. Zuckerman (Nominated by IEEE Technical Activities)
IEEE-USA President-Elect, 2015	Peter Alan Eckstein (Nominated by IEEE-USA) Keith D. Grzelak (Nominated by IEEE-USA)
IEEE-USA Member-at-Large, 2015-2016	Scott M. Tamashiro (Nominated by IEEE-USA) Gim Soon Wan (Nominated by IEEE-USA)

Balloting period starts on 15 August and ends at 12:00 noon, Central Time USA (17:00 UTC) on 1 October. All eligible voting members should look for their ballot to arrive via postal mail or access their electronically at www.ieee.org/elections. Forward election questions to corp-election@ieee.org.

IEEE DIVISION I DIRECTOR CANDIDATES, 2015

The on-coming IEEE Division I Director election has 3 candidates in the fray. In order for our members to familiarize their candidacies, goals, etc., we have the following details about them.



Renuka Jindal
Division I Director
Candidate, 2015

Dr. Renuka Jindal is a Professor of Electrical and Computer Engineering at the University of Louisiana at Lafayette, USA, involved in the theory and practice of random processes.

Earlier, Dr. Jindal was with Bell Labs, Murray Hill, New Jersey, as distinguished member of

technical staff for 22 years bridging technical and administrative roles. Highlights include his pioneering work in the '80s uncovering the physical understanding of noise in MOS devices at few hundred nanometers. He was elected Fellow of IEEE in 1991 and a recipient of the IEEE Third Millennium Medal.

As a dual career, 38 year veteran of IEEE, Dr. Jindal rose through the ranks as Editor, Editor-in-Chief, Vice-President of Publications serving as EDS President in 2010-2011. He is involved in chapter activities in region 5 and growth of IEEE's presence in region 10, mushrooming Division I joint chapters in South Asia from 1 to 19. As President he formulated the vision and mission of EDS enhancing member benefits

reversing the decline in EDS membership. An active member of IEEE TAB, he brought together 6 societies and 1 council to launch a highly successful *IEEE Journal of Photovoltaics*. He launched the EDS webinar series, the 1st EDS Open Access Journal (J-EDS), founded QuestEDS, initiated the EDS Celebrated Member program, and mentored the launch of high-school outreach program EDS-ETC.

Statement

To pursue the IEEE Envisioned Future in serving humanity, we must leverage our technical prowess and diversity. While the 5 units of Division I have been successful in pursuing their Visions and Missions, the power of collaborative effort has

yet to be fully harvested. My focus will be to nurture and build upon the synergies that bind us together, by launching joint activities, similar to EDS-ETC, developing a close-knit global community.

An increase in the number of active chapters across the globe with special emphasis on R10 countries China and India with a strong IEEE membership growth potential will be essential. Patterned on success of EDS in Asia, I intend to facilitate this thread for Division I in other parts of the world.

To serve the needs of the global technical community, with input from Division I societies and Councils, I intend to provide actionable feedback at IEEE TAB and BOD level. Also as Division I delegate to the IEEE Assembly, I will actively voice the interests of Division I electorate and produce results. Please contact me at r.jindal@ieee.org.



Rakesh Kumar
Division I Director
Candidate, 2015

Rakesh Kumar, Ph.D., IEEE Life Fellow, President & CEO, Technology Connexions, Inc., Immediate Past-President, Solid-State Circuits Society.

It would be an honor and a pleasure to serve as your representative on the IEEE Board of Directors. My primary goal will be to foster greater communication and cooperation across the various Societies and Councils in Division I. Ours is an extremely important Division for invaluable research and technical contributions to major product drivers – where would smartphones and computers be without the research reported in our Division's Journals and Conferences?

With 44 years of industry experience, and 25 years of volunteering with IEEE, I know that my leadership skills can make a difference. With my participative style I will work tirelessly for you in presenting new opportunities and will pull together cross-functional efforts to bring out

the best in our people, and give our Division a unified voice.

My industry experience spans technical contributions at Motorola, Cadence and Unisys in semiconductor process technology integration, device modeling, DFM, co-design, and packaging. I have extensive leadership, business and management experience (Cadence VP & GM, Unisys Engineering Director), and have leveraged this acumen and technical experience successfully in my own consulting practice for many years. My focus now is to give back to our industry by sharing my microelectronics technical know-how and entrepreneurial experience in educating university students as well as industry participants in many countries around the world. My IEEE experience, and industry and academic connections are a great asset.

I continue playing a leading role across various IEEE organizational units, and am coordinating Technical Activities' participation at the tri-annual worldwide Sections Congress this coming August; we are showcasing the capabilities of our various Societies and Councils.

During my term as the SSCS President (2012–13) our leadership team was able to better articulate value to our members, resulting in Society membership growth, reversing a multi-year decline. There are now 15% more SSCS Chapters around the world, and we continue to organize many DL tours, conduct leading Webinars, and offer needed online education material; all these represent a few of the accomplishments of my term as SSCS President.

I am proud to have played a key role in driving the formulation, approval and launch of two interdisciplinary, online publications—the RFIC VJ (with CASS, and MTTs), and the JxCDC, the *IEEE Journal on Solid-State Exploratory Computational Devices and Circuits* (with 4 Societies, and 3 Councils).

I urge you to vote, and thank you for your support.



Maciej J. Ogorzalek
Division I Director
Candidate, 2015

Maciej J. Ogorzalek is Professor and Head of the Department of Information Technologies, Jagiellonian University Krakow, Poland. An author of over 280 publications including one book and Ple-

nary or Keynote speaker at over 40 major international conferences and workshops. IEEE Fellow (1997) and active volunteer for 27 years—including 2008 CASS President and Chairman of IEEE Poland Section 2010-2013. He has been the Editor-in-Chief of the *IEEE Circuits and Systems Magazine* 2004-2007, member of the Editorial Board of Proceedings of IEEE (2006–2009), member of the IEEE Fellow Evaluation Committee (2011–2014), Chairman of the IEEE Prize Papers and Scholarships committee (2012–2013). Dr. Ogorzalek received a number of important recognitions including the CASS Golden Jubilee Medal, Guillemin-Cauer Award, CASS Meritorious Service Award, J. Groszkowski Medal (Poland), Education Medal (Poland) and is an elected Member of the European Academy of Sciences.

Statement

I am committed to IEEE as a transnational, global organization. Delivery of high level products and services is essential for IEEE members—journals, conferences, standards, continuing education, and they have to be available world-wide. If elected, I will strive to improve these aspects of operation as still there exist regions on the globe that are less privileged and need more focus and assistance. For them, delivery of services at affordable and sustainable member prices remains of paramount importance.

I will concentrate on strengthening the links between the electronic industry and IEEE, by bringing compelling design and manufacturing issues to the attention of the IEEE leadership.

Specifically I will work across the Division 1 organizational units to establish a dialogue between industry and academia under the leadership of IEEE.

I will also work to deliver a plan to introduce new areas of science and technology into IEEE scope, just to mention some emerging topics in geosciences, agriculture, chemistry or economics, bringing fantastic new

applications improving our lives. Specifically, electronic waste generation and management, environment-aware design, concepts of participatory design, life cycle engineering, compassionate business and sustainability come into the picture.

We have to work towards better utilization of resources, improvement of designs towards reuse of materials,

and creating new curricula for studies directed to better educate next generation of engineers aware of these above-mentioned problems and capable of bringing efficient new solutions.

I am dedicated to bring these themes to the direct attention of IEEE activities. I have the knowledge, experience, and commitment to pursue this vision.

EDS CHAPTER SUBSIDIES FOR 2015

The deadline for EDS chapters to request a subsidy for 2015 is September 1, 2014. For 2014, the EDS BoG awarded funding to 63 chapters, with most amounts primarily ranging from US\$250 to US\$750. In June, Chapter Chairs were sent an e-mail notifying them of the current funding cycle and providing them with a list of guidelines. In general, activities which are considered fundable include, but are not limited to, membership promotion, travel allowances for invited speakers to chapter events, and support for student activities at local institutions.

Chapter Subsidy requests can be requested by completing the online chapter activity report (<https://adobeforms.central.com/?f=KrG%2A%2AmETwCXtnzrx-xEuSQ#>).

Please note that the report needs to be submitted by September 1st.

Final decisions concerning subsidies will be made in December. Subsidy checks will be issued by early January of the following year. Please visit the EDS website for



more information: <http://eds.ieee.org/chapter-subsidy-program.html>.

NEW ON-LINE SYSTEM FOR IEEE FELLOW NOMINATIONS

The task of nominating a Senior Member for Fellow grade got easier with the new Fellow On-line System. Multiple upgrades were incorporated, but three main enhancements will please nominators. After a nominator logs in the system, the first requirement will be to input the nominee's member number. Entering this information will immediately let the nominator know if the nominee meets the requirements of being an active IEEE Senior or Life Senior Member and if the nominee has been a member in good standing for five years or more. If a nominee is ineligible, the system will prevent the nominator from filling out the entire form and avoid any unnecessary time.

Another new feature that's required is inputting the member number of the references. The nomination must include at least five, but no more than eight references who are IEEE Fellows. Entering this information will immediately inform the nominator, if a reference is eligible or not.

The best feature is allowing nominators the capability to make changes to main text, update e-mail addresses, add and delete reference and endorsement names, and to delete nominations they prepared out of the system up to the 1 March deadline. Providing nominators this kind of flexibility will give them the opportunity to prepare a better nomination.

After the deadline has been reached, the system will authenticate all the data and verify that each nomination package is complete. As soon as this process is finished, a confirmation will be sent to the nominator letting them know whether the nomination will or will not be considered.

The system is now open and ready to accept nominations for the class of 2016. Starting the process early will alleviate last minute issues. You can visit the Fellow Web Site at www.ieee.org/fellows, then click "Online Nomination Form" to begin.

*Rosann Marosy
Manager, Fellow Activities IEEE*

CONGRATULATIONS TO THE 22 EDS MEMBERS RECENTLY ELECTED TO IEEE SENIOR MEMBER GRADE!

Abdelhak Bensaoula
Michael Beunder
Shekhar Bhansali
Wengang (Wayne) Bi
Eugenio Cantatore
Kun-Yung Chang
Te-Kuang Chiang
SeragE Habib
Tuo-Hung Hou
Hidetoshi Koike
Hiroshi Miki

Seiichiro Mizuno
Christian Monzio Compagnoni
Andrew Moor
Ali Asghar Orouji
Nadia Rafat
Gianluca Piazza
Sayeef Salahuddin
Makoto Takamiya
Yen-Hao Shih
Akinobu Teramoto
Chin-Che Tin



If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US \$25 for a new IEEE society membership. Upon request a letter will be sent to employers, recognizing this new status.

For more information on senior member status, visit: http://www.ieee.org/membership_services/membership/senior/index.html

To apply for senior member status, fill out the on-line application https://www.ieee.org/membership_services/membership/senior/application/index.html. You will need to Sign-in with your IEEE account.

Please remember to designate the Electron Devices Society as your nominating entity!

ENHANCE YOUR CAREER WITH IEEE SENIOR MEMBERSHIP



*Mikael Östling
EDS Vice-President
of Membership &
Services*

The Electron Devices Society established the EDS Senior Member Program to both complement and enhance the IEEE's Nominate-a-Senior-Member Initiative and make IEEE/EDS members aware of the opportunity and encourage them to elevate their IEEE membership grade to Senior Member. This is the highest IEEE grade for which an individual can apply and is the first step

to becoming a Fellow of IEEE. If you have been in professional practice of 10 years, you may be eligible for Senior Membership.

Benefits of Senior Membership¹

- **Recognition:** The professional recognition of your peers for technical and professional excellence.
- **Senior member plaque:** Since January 1999, all newly elevated Senior members have received an engraved Senior Member

plaque to be proudly displayed for colleagues, clients and employers to see. The plaque, an attractive fine wood with bronze engraving, is sent within six to eight weeks after elevation.

- **US\$25 coupon:** IEEE will recognize all newly elevated Senior members with a coupon worth up to US\$25. This coupon can be used to join one new IEEE society. The coupon expires on 31 December of the year in which it is received.
- **Letter of commendation:** A letter of commendation will be sent to your employer on the

¹IEEE.org, http://www.ieee.org/membership_services/membership/senior/index.html

achievement of Senior member grade (upon the request of the newly elected Senior member).

- **Announcements:** Announcement of elevation can be made in section/society and/or local newsletters, newspapers and notices.
- **Leadership Eligibility:** Senior members are eligible to hold executive IEEE volunteer positions.
- **Ability to refer other candidates:** Senior members can serve as a reference for other applicants for senior membership.
- **Review panel:** Senior members are invited to be on the panel to review senior member applications.
- **US\$25 referral coupon:** Newly elevated Senior members are encouraged to find the next innovators of tomorrow and invite

them to join IEEE. Invite them to join and the new IEEE member will receive \$25 off their first year of membership.

As part of the IEEE's Nominate-a-Senior-Member Initiative, the nominating entity designated on the member's application form will receive US\$10 from IEEE for each application approved for Senior Member grade when there are at least five approved applications. As an EDS member, we would appreciate it if you could indicate on your Senior Member application form that **EDS** is your nominating entity.

Please be aware that even if you decide to list EDS as your nominating entity, you still need to have an IEEE member nominate you along with two other references. Your

nominator and your references all must be active IEEE members holding Senior Member, Fellow or Honorary Member grade.

For more information on the criteria for elevation to Senior Member, please visit the Senior Membership Portal: http://www.ieee.org/membership_services/membership/senior/index.html.

We strongly encourage you to apply for IEEE Senior Membership to enhance your career. At the same time, you'll be helping EDS. Thank you for supporting IEEE and EDS.

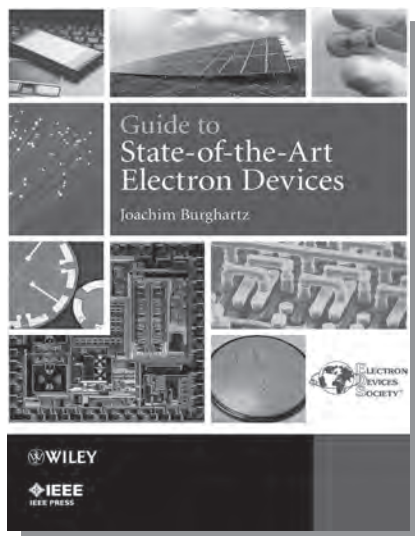
Mikael Östling
EDS Vice-President of Membership
& Services
KTH, Royal Institute of Technology
Sweden

EDS GUIDE WINS PROSE AWARD

As most EDS members know, the *EDS Guide to State-of-the-Art Electron Devices*, edited by long-time EDS volunteer Joachim Burghartz, celebrates over 60 years of the Electron Devices Society's work, from its inception in 1952 as the IRE Professional Group on Electron Devices to its official formation as an IEEE society in 1976.

Since its publication in 2012, the book has engendered high praise from the device engineering community, but recently it received a very special honor. In February, the Association of American Publishers, Inc. announced the winners of the **Professional and Scholarly Excellence (PROSE) award for 2013**. *The EDS Guide to State-of-the-Art Electron Devices* was awarded the PROSE for Engineering & Technology!

For nearly 4 decades, the PROSE awards have been given to distinguished books and journals in over 40



categories. The awards are judged by a panel of peer publishers, librarians, and subject-related professionals. By becoming a PROSE award winner, *the EDS Guide to State-of-the-Art Electron*

Devices becomes an even greater honor for the society. We extend our deepest thanks and congratulations to Joachim and his cadre of 70 contributing authors, all of whom volunteered their time and expertise to create this outstanding book at a greatly reduced cost.

For those unfamiliar with *the EDS Guide to State-of-the-Art Electron Devices*, it is a comprehensive, full-color publication featuring a foreword by Nobel Laureate and EDS Celebrated Member George E. Smith. In addition to over 20 chapters, a historical timeline runs throughout the book highlighting key time periods/eras in the electron device field.

For more information, and to order at the special members-only price, please visit the EDS Website (<http://eds.ieee.org/eds-anniversary-book.html>).

2014 AWARD WINNERS

2014 WILLIAM R. CHERRY AWARD WINNER—DR. RONALD A. SINTON



Ronald A. Sinton
2014 William R.
Cherry Award
Winner

The Photovoltaic Specialist Conference Cherry Committee is proud to announce Dr. Ronald A. Sinton as the winner of the 2014 William R. Cherry Award. This award is named in honor of William R. Cherry, a founder of the photovoltaic community. In the 1950's, he was instrumental in establishing solar cells as the ideal power source for space satellites and for recognizing, advocating, and nurturing the use of photovoltaic systems for terrestrial applications. The William R. Cherry Award was instituted in 1980, shortly after his death. The purpose of the award is to recognize an individual engineer or scientist who devoted a part of their professional life to the advancement of the science and technology of photovoltaic energy conversion. The award winner must have made significant contributions to the science and/or technology of PV energy conversion, with dissemination by substantial publications and presentations.

Ronald A. Sinton is founder and president of Sinton Instruments, based

in Boulder, Colorado. Ron received his PhD in Applied Physics from Stanford University in 1987, following a B.S. in Engineering Physics from the University of Colorado in 1981. His studies at Stanford University included the demonstration of 28%-efficient silicon concentrator solar cells, the physics of high-injection solar cells, detailed device modeling, measurements of Auger recombination, and the test and measurement of concentrator solar cells. As a Research Associate at Stanford, Ron developed simplified versions of the sophisticated point-contact solar cell designs that could maintain the high efficiency while minimizing the process complexity. He continued this work during the early years of SunPower Corporation, focusing on solar cell designs and manufacturing processes potentially suitable for commercialization.

Dr. Sinton founded Sinton Consulting in 1992. The company soon focused on the development of novel test and measurement instruments. This work resulted in many fruitful and very international, collaborations and research papers. Innovations from Sinton Instruments that have become standard within the R&D community and the silicon manufacturing industry include the QSSPC lifetime technique, Suns-Voc

measurements, and novel methodologies for measuring the efficiency of high-efficiency solar cells and modules.

Dr. Sinton has maintained his special interest in the device physics of silicon solar cells. Running a metrology company has proven to be an effective way to be at the center of both of the R&D and manufacturing communities, offering opportunities to contribute at the most technical academic level as well as providing instrumentation to support tens of GWs of silicon solar cell and module production.

Ron received the R&D 500 award in 2005 for developing instruments for measuring bulk lifetime in silicon ingots and bricks. He is well published and has coauthored 4 book chapters. He is an associate editor of the *IEEE Journal of Photovoltaics* and has frequently presented tutorials on silicon solar cells and device physics at the IEEE PVSC conferences, first in 1988 and as recently as 2013. Ron is a frequent contributor to conference program committees; especially the IEEE PVSC, the NREL Silicon Workshop, and the SiliconPV conference.

David M. Wilt
2014 Award Co-Chair
AFRL
New Mexico, USA

EDS BoG MEMBER RECEIVES TWO AWARDS FOR NANOTECHNOLOGY DEVELOPMENT



Dr. Meyya Meyyappan, EDS BoG member, was honored recently by the Engineers' Council with the Outstanding Engineering Achievement Merit Award

for the development and demonstration of a nanoscale vacuum tube. The award was presented on National Engineers Day, February 22, 2014, at the Engineers' Council Annual Banquet in Universal City, California. Vacuum is better than any semiconductor for electron transport due to the absence

of scattering. Meyya and his team, including the 2012 recipient of the EDS Early Career Award, Jin-Woo Han, developed an all silicon based vacuum tube with an anode-cathode gap of 150 nm in the first generation device which exhibited a cut-off frequency of 450 GHz with a drive voltage of only

8 V. With further reduction in gap and better gate control through wrap-around gate, the device is expected to provide THz performance while operating under 2 V. The radiation immunity of the vacuum tube is expected to be beneficial in satellite communication and space electronics.

Meyya has also been recognized recently by the IEEE-USA with a Professional Achievement Award for championing nanotechnology awareness and education through the development of trynano.org. The

award is to be presented at the IEEE-USA Annual Meeting in Providence, Rhode Island on May 17, 2014. The trynano.org website, modeled after IEEE's tryengineering.org website, is meant to educate high school students about nanotechnology. The website, maintained by the IEEE Educational Activities Board (EAB), was developed by IEEE volunteers mostly from EDS and includes descriptions about various nanomaterials, applications in nanoelectronics and many other domains, resources

about universities, games, and lesson plans for high school teachers. In addition to English, the website has been translated into Korean through sponsorship from a Korean University (POSTECH) and based on statistics from EAB, the Korean site appears to be the most popular resource among Korean students. The development team is hoping to produce translations in Chinese, Spanish, Arabic and possibly other languages, pending sponsorship to cover translation and other costs.

IEEE FELLOW AND EDS MEMBER HONORED BY WHITE HOUSE AS CHAMPION OF CHANGE FOR SOLAR DEPLOYMENT



Dr. Rajendra Singh, D Houser Banks Professor in the Holcombe Department of Electrical and Computer Engineering at Clemson University,

has been named by the White House as the 'Solar Champion of Change' in recognition of his immense contribution towards developing alternate source of energy and promoting solar deployment in residential, commercial and industrial sectors. He is among the 9 individuals declared as Champions of Change. The White House said these individuals are driving policy changes at the local level to expand energy choices for Americans, grow jobs, and add new clean energy to the grid.

The pace of solar deployment continues to increase across the world. Last year was a record-breaking year for new solar installations, and the amount of solar power installed in the U.S. has increased around eleven fold—from 1.2 gigawatts in 2008 to an estimated 13 gigawatts today, which is enough to power more than 2.2 million American homes. In fact, every four minutes another American home or business went solar and solar power is now a cost competitive option

that offers financial and environmental benefits. This trend has yielded new economic opportunities for many—job growth in the solar industry is now increasing by 20% each year.

In order to continue the momentum, in June 2013, President Obama launched a comprehensive Climate Action Plan to cut carbon pollution and advance the clean energy economy. As part of that Plan, the President set a goal to double solar, wind, and geothermal electricity generation by 2020 and to more than triple the onsite renewable energy production in federally assisted residential buildings. The Champions of Change program was created as an opportunity for the White House to feature individuals doing extraordinary things to empower and inspire members of their communities.

With proven success in operations, project/program R&D, Dr. Singh is a leading semiconductor and photovoltaic (PV) expert with immense experience, both industrial and academic. Starting as a graduate student in 1974 and working on Silicon Solar Cells as the topic of his PhD thesis dissertation, in the last 40 years Dr. Singh has played the role of visionary leader to advance the technology of PV module manufacturing. On economic considerations, in 1980 he predicted silicon as the dominant PV material. To

transform global electricity infrastructure, he is providing leadership to use PV as the source of local direct current electricity in the US and emerging and underdeveloped economies. To prepare future solar leaders of the 21st century, mentoring students at all levels (including pre high school) is his passion. He is actively involved with civic groups (e.g. Sierra Club) to bring legislation and regulations in South Carolina that will lead to the growth of solar generated electricity.

Dr. Singh has published over 330 papers in various journals and conference proceedings. Currently he is serving as Chair of IEEE Electron Devices Society Technical Committee on Semiconductor. Part of Dr. Singh's awards and honors include Distinguished Technologist of United Nations Development Program (1987), Outstanding Researcher Award and Faculty Excellence from Clemson University, Thomas D. Callinan Award of the Electrochemical Society (1998) and McMaster University Distinguished Alumni Award (2005). In 2010, Photovoltaics World selected him as one of the ten Global «Champions of Photovoltaic Technology.» He is Fellow of IEEE, the Society of Optical Engineering, American Association for the Advancement of Science, and American Society of Metals, ASM.

2014 AWARDS - CALL FOR NOMINATIONS

CALL FOR NOMINATIONS FOR THE EDS CHAPTER OF THE YEAR AWARD

The EDS Chapter of the Year Award is given each year based on the quantity and quality of the activities and programs implemented by the chapters during the prior July 1st–June 30th period.

At the June 2012 EDS BoG (AdCom) Meeting, the BoG (AdCom) approved to increase the number of awards we give out in a given year, starting with the 2013 Award. We will award one Chapter from each of the following Regions:

- Regions 1–7
- Region 8
- Region 9
- Region 10

Nominations for the awards can only be made by SRC Chairs/Vice-Chairs, or self-nominated by Chapter Chairs. Please visit the EDS website to submit your nomination form.

Each winning chapter will receive a plaque and check for \$500 to be presented at an EDS Conference or Chapter Meeting of their choice. Travel reimbursement will not be provided.

The schedule for the award process is as follows:

Action	Date
Call for Nominations E-Mailed to Chapter Chairs, SRC Chairs & SRC Vice-Chairs	June 1st
Deadline for Nominations	September 15th
Regions/Chapters Committee Selects Winners	Early-October
Award given to Chapter Representative at IEDM	First week of December



CALL FOR NOMINATIONS 2014–2015 IEEE ELECTRON DEVICES SOCIETY REGION 9 BIENNIAL OUTSTANDING STUDENT PAPER AWARD



Description: Awarded to promote, recognize, and support meritorious research achievement on the part of Region 9 (Latin America and the Caribbean) students, and their advisors, through the public recognition of their published work, within the Electron Devices Society's field of interest: All aspects of the physics, engineering, theory and phenomena of electron and ion devices such as elemental and compound semiconductor devices, organic and other emerging materials based devices, quantum effect devices, optical devices, displays and imaging devices, photovoltaics, solid-state sensors and actuators, solid-state power devices, high frequency devices, micromechanics, tubes and other vacuum devices. The society is concerned with research, development, design, and manufacture related to the materials, processing, technology, and applications of such devices, and the scientific, technical and other activities that contribute to the advancement of this field.

Prize: A distinction will be conferred in the form of an Award certificate bestowed upon the most outstanding Student Paper nominated for the two-year period. The prize will be presented at either the International Caribbean Conference on Devices, Circuits and Systems (ICCDCS) or the Symposium on Microelectronics Technology and Devices (SBMicro). In addition to the recognition certificate, the recipient will receive a subsidy of up to \$1,500 to attend the conference, where the award is to be presented. There will be a formal announcement of the winner in a future issue of the EDS Newsletter. The winner will also receive up to three years of complimentary IEEE and EDS student membership, as long as winner remains eligible for student membership.

Eligibility: Nominee must be enrolled at a higher education institution located in Region 9. In the case of a co-authored paper, only eligible co-authors may be nominated. Papers should be written in English on an electron devices related topic. Papers should have been published, in full-feature form, during 2014–2015 in an internationally recognized IEEE sponsored journal or conference in the field of electron devices related topics. Statements by the student and by the faculty advisor should accompany the nomination. Nominator must be an IEEE EDS member. Previous winners of this award are ineligible. There must be a minimum of five nominations submitted in order for the award to be administered for that year.

Basis for Judging: Demonstration of Nominee's significant ability to perform outstanding research and report its results in the field of electron devices. Papers will be judged on: technical content merit, originality, structure, clarity of composition, writing skills, overall presentation. These criteria will be weighted by the assessment of the nominee's personal contribution and the linkage of the nominated work to the nominee's career plans.

Nomination Package:

- Nominating letter by an EDS member (it may be the faculty advisor)
- A brief one-page (maximum) biographical sketch of the student
- 1000 words (maximum) statement by the nominated student describing the significance and repercussion of the nominated work within the wider scope of the nominee's career plans
- 400 words (maximum) statement by the faculty advisor under whose guidance the nominated work was carried out. It should unmistakably state the faculty advisor's support of the nomination, and clearly explain the extent of the nominated student's contribution, as well as its relevance for the overall success of the reported work.
- A copy of the published paper

Timetable:

- Nomination packages are due at the EDS Executive Office no later than **15 February 2015**.
- Nomination packages can be submitted by mail, fax or e-mail, but a hard copy must be received at the EDS Office
- Winners will be notified by 15 March 2015.
- Recipients may choose to have the formal presentation of the award at either one of the conferences: ICCDCS 2015 or SBMicro 2015

Send completed package to: IEEE Operations Center
EDS Executive Office
EDS R9 Outstanding Student Paper Award
445 Hoes Lane, Piscataway, NJ 08854 USA

For more information contact: Laura Riello, EDS Executive Office
l.riello@ieee.org or 732-562-3927

YOUNG PROFESSIONALS

Call us the Young Professionals, Please

IEEE Young Professionals is the new name for the group that was known as IEEE Graduates of the Last Decade—or GOLD, for short. The name change approved by IEEE Member and Geographic Activities (MGA) Board in June 2013, has gone into effect throughout the organization.

GOLD was established in 1998, and the program helped recent graduates network, develop their technical and professional skills, and find jobs. Members who qualified were automatically affiliated with the group when they signed up to or renewed their IEEE Membership. In 2013, the group had more than 64,000 members worldwide.

However, the name GOLD had a problem. The name didn't resonate with the audience it was meant to engage, says Ralph Ford, Vice President of MGA, which oversees what is now IEEE Young Professionals. On the other hand, the new name describes exactly what is members are—Young Professionals. "We hope the name will help our members recognize that they belong to a global professional community that can support their career needs from early on," Ford says. "The goal is to make the community more visible as well as support members and prepare them for leadership positions."

The rebranding is successfully spreading around the world, with groups from Toronto to New Zealand taking part in the effort through various events. Additionally, the Young Professionals rebranding was showcased at the IEEE Global Humanitarian Technology Conference (GHTC) late in 2013.

With GOLD, the members could not take full advantage of benefits, as they could only join within the short



period of 10 years after completing their degree. This has now changed, and the criterion has now been extended accordingly to be 15 years after graduation. This change will take effect on August 15, 2014. Following graduation, the young professional's time is very transient, first jobs, marriage, relocations, new homes, they have so much going on during this time. The Society wanted to give them the time to take full advantage of the benefits and support them. To complement this, now we have also added the ability to opt-in after members pass the 15 year mark.

Being part of the community comes with many perks, according to Timothy Wong, 2014 chair of the IEEE Young Professionals Committee. These include meaningful networking opportunities on a local and global scale. It also helps the members to grow their leadership skills. IEEE Young Professionals is about helping members advance in their careers. Many Young Professionals' resources are tailored to help members climb the career ladder. These resources include Mentor Centre, which connects professionals just starting out with mentors who are experienced engineers in similar fields of interest, and live webinars tailored to the needs of job seekers cover such topics as how to have a successful job interview and using social media for the job hunt. There are also social events, such as barbecues, bowling tournaments. Members can find out more about what's going on in their communities by contacting their local affinity group.

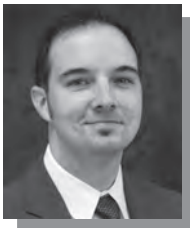
IEEE EDS Young Professionals (YP) group is very active with all the changes happening with YP in IEEE community is being engulfed. This change is also an opportunity to reinvigorate the Society relationship with its younger members. In 2014, we plan to achieve this goal by optimizing our communication and contact with all our members in EDS. In particular, every quarter you will now find a column in EDS Newsletter dedicated to Young Professionals. We will continue organizing technical, and non-technical, webinars with topics tailored to the interest of those who are just embarking in their careers; you should expect more details soon.

In order to get to know you better, we also want to energize the EDS Young Professionals Ambassador program, so hopefully we will get to pay you a visit soon, or we might run into you at an EDS conference. Our Newsletter column will provide with all the information you might need regarding YP activities. For more information about the transition of GOLD to IEEE Young Professionals, contact young-professionals@ieee.org. If you have any questions or suggestions about YP activities in EDS, please feel free to contact eds@ieee.org.

Josheel Pranalal
Vice Chair, Communications
and Marketing
IEEE MGA Young Professionals

Daniel Camacho
EDS BoG Member & YP Chair

2014 PVSC YOUNG PROFESSIONAL AWARD WINNER



Kyle Montgomery
2014 PVSC
Awards Chair

The IEEE Photovoltaics Specialists Conference (PVSC) introduced a new award this year to recognize outstanding young professionals in the photovoltaics (PV) community.

The PVSC Young Professional Award recognizes individuals who have made significant contributions to the science and technology of PV energy conversion, including work on PV materials, devices, modules, and/or systems. The award recipient must also show significant promise as a leader in the field.

On behalf of the organizing and program committees of the 40th IEEE PVSC, I am delighted to announce the recipient of this year's award—**Dr. Oliver Schultz-Wittmann**. He is recognized for his outstanding achievements in the development of silicon solar cells, including the

current world-record multicrystalline cell (20.4%) and high-efficiency, low-cost crystalline cells developed for commercialization by a recently-acquired start-up company.



Dr. Oliver Schultz-Wittmann started his work in the PV field in 1998 helping with rooftop installations while studying Physics at the University of Hamburg, Germany, where he received his diploma in Physics in 2001. His graduate thesis topic was the manufacturing and characterization of selective emitter structures on crystalline silicon solar cells in cooperation with the Fraunhofer Institute for Solar Energy Systems ISE in Freiburg, Germany. In 2002, he began his doctoral thesis on high-efficiency multicrystalline silicon solar cells at Fraunhofer ISE. The highlight of his work was demonstrating

cells made from this material with conversion efficiencies greater than 20%, a record that still stands today. Oliver worked with industrial partners on several high-efficiency concepts, including laser-grooved buried contact cells and interdigitated back contact structures, before leading the high-efficiency cell group from 2007–2008. In 2009, Oliver co-founded the Silicon Valley start-up company TetraSun which was acquired by First Solar in 2013 for their launch of crystalline silicon solar cell production. He has five issued patents and is an active peer reviewer for several journal publications and the IEEE Photovoltaic Specialists Conference. Oliver received the Solar World Junior Einstein Award in 2006 and is a co-awardee of the R&D 100 Award of 2013. Congratulations, Dr. Schultz-Wittmann!

Kyle Montgomery
2014 PVSC Awards Chair
University of California, Davis

RICE UNIVERSITY'S INAUGURAL EDS-ETC EVENT

Volunteers from Rice University, Houston, Texas, held their first EDS-ETC event on April 14, 2014, at Rita Drabek Elementary School in Sugar Land, Texas. This was Rice University's pilot program, organized to introduce fifth grade science students to the world of electrical engineering. IEEE EDS member, Douglas P. Verret and a team of Rice University students, conducted a very successful class of excited and engaged students. The following day the class teacher handed out a survey to the students and the program was given high marks by the students, with 18 out of 20 rating the program as a 10/10, and the remaining students giving the program an 8/10.



The volunteers handed out one kit for every two students and a

pre-determined set of experiments. The teacher of the class, Katherine

Saludis, gave a quick introduction to who we were and what we would be doing, followed by the volunteers giving a quick tutorial on how to use the Snap Circuits® kits. Each group of two students were free to work at their own pace through the experiments. The volunteer team distributed themselves throughout the room and checked in with each group to assist when necessary, as well as ask questions about their current experiment to make them think about the underlying concepts being demonstrated. Most of the groups finished the experiments by the end of the class, and a few began experimenting with the kits on their own. We wrapped up with a quick discussion asking the

students to talk about what they learned. Other fifth grade teachers at Rita Drabek were also present in the classroom to observe so that they could gauge their own interest level in the program. Plans are under way to meet with the school principal to discuss expanding the program at Rita Drabek and also the Elementary School Science Coordinator to fan the program out to other schools. Doug is also helping schools get funding from other organizations and corporations for a large purchase of kits.

The teacher, Katherine Saludis, met with other faculty after our event. Some of the comments that were recorded were: "definitely effective use of class time," liked

the inquiry, discovery approach, "students more engaged than usual," "want to use Snap Circuits on their own." Collectively, Doug, the teachers, and our volunteers agreed it went very well, but we had a few key areas for improvement. The main point was that we needed to have the learning goals and curriculum more planned out. Rather than coming up with questions to ask around the experiments, choose experiments that match a learning goal we are trying to get across. The teachers are excited to have additional events during the next school year.

Thomas Ladd
Rice University

EDS HOSTS FIRST CHAPTER-BASED WEBINAR, BROADCAST LIVE AROUND THE GLOBE



Stewart Rauch
EDS Distinguished
Lecturer

As most of you know, the EDS Webinar program has grown extensively in the past few years, with both the live events and access to the Webinar Archive on the EDS site becoming

vital benefits of membership in the society.

Recently, we expanded our offerings to begin broadcasting in-person, chapter-based events to members around the world. The inaugural chapter webinar took place on April, 23rd at the IBM facilities in

Fishkill, New York, home of the EDS Mid-Hudson Valley Chapter.

The hometown crowd at IBM was treated to an important talk entitled *Terrestrial Radiation Induced Soft Errors in Integrated Circuits*, presented by EDS Distinguished Lecturer, Stewart Rauch. The on-site attendees were joined by over 100 members representing every region of the IEEEWorld.

Dr. Rauch is currently a faculty member at State University of New York, New Paltz. He recently retired as Senior Technical Staff Member at IBM Semiconductor Research and Development Center (NY), specializing in hot carrier, bias temperature instability, and soft error reliability of state of the art CMOS technologies.

He is a Senior Member of IEEE, a Life Member and Distinguished Lecturer of the Electron Devices Society, and frequent journal reviewer for such publications as the *IEEE Transactions on Electron Devices* and the *Microelectronics Reliability* journals, etc.

Our deepest thanks to Dr. Rauch and EDS volunteers Fernando Guarin and Mukta Farooq (Mid-Hudson Chapter Chair) for the time and energy to make this very special event possible.

Look for more live chapter webinars soon, and if you're interested in hosting such an event at your chapter, do not hesitate to contact EDS Executive Director Chris Jannuzzi at c.jannuzzi@ieee.org.

QUESTEDS



Samar Saha
EDS President-Elect

Interested in knowing why it's not possible to measure the built-in voltage of a PN junction using a voltmeter? Do you need to understand the best way to derive an expression for the average thermal velocity of an electron? Or are you curious about what quantum dots and wires are? The answers to these questions and more are available through the QuestEDS Question and Answer page.

To ask a question not already addressed on the Q&A page, visit www.ieee.org/go/questeds. Technical experts answering the questions posed represent academic, government, and industry sectors.

Questions are grouped into nine technical categories and two general ones. Technical categories cover subject areas like semiconductor and device physics, process technology, device characterization, technology CAD, compact modeling, VLSI interconnects, photovoltaics, and quantum electronics. Subject areas addressed are anticipated to expand in the future. Two other categories address questions pertaining to educational activities and general inquiries about society membership. Within a two week time frame from when the question is asked, an answer is posted online. Incoming questions are handled by an editor-in-chief who ensures that they fall within the technical scope of EDS and that they are adequately answered.

Photovoltaics

Question 061-13:

In a solar cell, we want to collect the photo-generated electrons and holes in separate terminals and so we want them not to recombine before collection. In a multijunction solar cell, current flows from one pn junction to another through tunnel junction, where electron makes a tunneling jump from conduction band to valence band and with so many holes in the valence band, the jumping electron should recombine with hole. So, how can the photo-generated electrons and holes make it to the opposite electrode without recombination in a multijunction solar cell?

Answer 061-13:

In any solar cell, one needs to look at how the circuit is completed. That is, how does an incoming photon find exactly the same condition as the previous photon so as to send the next electron out to be collected?

In a single junction, consider what happens in the junction layer (say, p type in a p-n cell). The incoming photon creates an electron-hole pair (EHP). The hole (empty space in the valence band) stays behind in the p-layer, while the electron makes the transit to the n-layer and goes back through the wires to the p side. When it arrives there, the ohmic contact to the p-layer assures that it goes into the valence band (that is, the lowest energy state for it). There it finds the initial hole (vacancy) and settles into that vacant space, i.e. the electron recombines with the hole. The next incoming photon repeats the process since there is an electron in the original space. Thus, what we need is for the hole to remain behind so that the process is complete and reproduced. This is why the current corresponds to the transport of either the electrons or the holes generated in the same layer (p here), but not to the transport of both. This is a different case from that of photo-conductivity, where an external battery supplies both the electrons and holes needed for transport, and therefore, we count both.

Now consider a tandem cell. Both cells are generating the SAME current, i.e. the same number of carriers is being collected from each cell. Let us ignore internal recombination. Then the same number is being generated. Again, consider the p-layer in each cell. Consider that two photons of different energy are incident, one which generates an EHP in the first cell, and one which generates an EHP in the second cell. The electron generated by the first photon in the p-layer of the first cell transits to the interface with the second cell. There it recombines with the hole created by the second photon in the second cell. The external current now comes from the electron generated in the second cell, which travels back to the first cell through the external circuit, and recombines with the hole left behind there by the first photon to complete the cycle.

Thus, it is essential that the electron coming from the first cell recombine with the hole in the second cell. Therefore, an efficient recombination junction is necessary at the interface between the first and the second cell. A tunnel junction allows for the first electron to recombine with the second hole by tunneling into that space.

To view the entire library of questions and answers, visit <http://eds.ieee.org/member-sign-in-form.html?notauth=1>. Your IEEE login is required to view the answer page.

Samar Saha
EDS President-Elect
Ultrasolar Technology
Santa Clara, CA, USA

CHAPTER NEWS

In this issue we are introducing highlights of two established conferences which are important in their area and successfully progressing for years and wholly owned and organized by our Chapters. Also, a professional activity of different nature with social impact by one of our student chapters is presented.

ICSE 2014 of ED Malaysia Chapter

–by Nizar Hamidon and Sushitha Menon

The 11th bi-annual conference ICSE 2014 (IEEE International Conference on Semiconductor Electronics), organized by the IEEE ED Malaysia Chapter, will be held at the Berjaya Times Square Hotel, Kuala Lumpur from August 27–29, 2014. This event is co-organized by the Institute of Microengineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia (UKM). Over the last 22 years, ICSE has become the preeminent international forum on semiconductor electronics embracing all aspects of the semiconductor technology from circuits and devices, modeling and simulation, photonics and sensor technology, MEMS technology, process and fabrication, packaging technology and manufacturing, analysis and reliability, material and devices and nanoelectronics.

ICSE 2014 offers six keynote lectures and regular oral and poster papers with an expected participation of more than 200 professionals from more than 10 countries including USA, UK, India, Thailand, Australia, Taiwan, China, Bangladesh, Japan and Indonesia. The keynote speakers and topics are:

- Dr. Asad M. Madni of UCLA, USA, delivering the talk on “*Convergence of Emerging Technologies to Address the Challenges of the 21st Century*,”

- Dr. Arokia Nathan of Cambridge University, UK on “*Amorphous Oxide Electronics*;”
- Dr. Edward Yi Chang of National Chiao Tung University, Taiwan on “*Realization of GaN-based Technology for Future High Power & High Frequency Applications*;”
- Dr. Young June Park of Seoul National University, Korea, lecturing on “*There is Plenty of Room at the Silicon*;”
- Dr. Abdelkrim Khelif of CNRS, France, on “*Acoustic Metamaterials and Phononic Crystals: Towards the Total Control of the Wave Propagation*,” and
- Dr. Hiroshi Inokawa of Shizuoka University, Japan on “*SOI Photodiode with Surface Plasmon Antenna: from Sensitivity Enhancement to Refractive Index Measurement for Biosensing*.”

Dr. Burhanuddin Yeop Majlis of UKM is the Conference Chair. More information about ICSE 2014 can be obtained at the website: <http://ieeemalaysia-eds.org/icse2014/home.html>.

IPFA 2014 of ED/Rel/CPMT Singapore Chapter

–by Gan Chee Lip and D S Ang

The International Symposium on Physical and Failure Analysis of Integrated Circuits (IPFA) is in its 27th year and will be returning to Singapore after touring other countries in Asia in odd years. IPFA 2014 will be held at Marina Bay Sands Singapore from June 30 to July 4, 2014. Packed with quality technical presentations, including 2 keynote speeches by Michael Pecht of University of Maryland, USA and Raj Nair of GLOBALFOUNDRIES Singapore, and more than 50 invited (inclusive of 2 best paper exchanges with the 2013 ISTFA and ESREF) and contributed talks by researchers from IMEC, IBM, and other leading companies and universities in

Europe, United States, Asia/Asia Pacific, IPFA 2014 promises to bring a rewarding experience to its attendees.

The numerous 2-day tutorial sessions which precede the 3-day conference program will feature comprehensive technical reviews on a wide range of topics – memory reliability (Robin Degraeve, IMEC), IC Design Debug by Optical Probing (Mike Bruce, SEMICAPS), SRAM Failure Analysis (Zhigang Song, IBM), TSV reliability (Rui Huang, UT Austin), FIB Backside Processing (Christian Boit, TU Berlin) and HR-TEM (Tim White, NTU Singapore).

The technical line-up spans seven dedicated streams: 1) Advanced Failure Analysis Techniques; 2) Sample Preparation, Metrology and Material Characterization; 3) Die and Package Level FA Case Studies; 4) Novel Devices and LED Reliability; 5) Transistor Reliability; 6) Advanced Interconnect Reliability; 7) Product Reliability Evaluation.

Highlights in the FA domain include a wafer-level fault isolation approach for debugging IC JTAG failures, characterization of TSVs by 3D electron backscatter diffraction, Raman and FTIR complementary vibrational spectroscopy, a combination of plane-view scanning capacitance microscopy, nanoprob ing and TCAD modeling for MOSFET implant failure analysis.

The session on transistor reliability continues to be dominated by discussion on individual switching oxide defects in small area devices. In the BEOL arena, scientists from IBM will demonstrate the imaging of TSVs using x-ray tomography. As for product reliability, engineers from Hitachi Power Solutions will share a new technique for acquiring dead pixel free and fine inspection image of advanced LSI package using scanning acoustic tomography. Researchers from Freescale will present insights



Volunteers of WIE group of SJCE Chapter with children in need of help

and strategies for the analysis of field data and prediction models for improved customer risk assessment. In the session for Novel Devices and LED Reliability, Presentation from UT Dallas will be on FinFET reliability and researchers from Samsung will elaborate on a quantitative analysis approach for noise generated from shared circuitries in DDR3 DRAM.

STAR Program by SJCE Student Chapter

–by C R Venugopal

The IEEE EDS Student Chapter at SJCE, Mysore, India, with its healthy women member strength has initiated the WIE program called **Student-Teacher and Research Engineer/Scientist (STAR)**. This program was developed to address the growing concern that girls do not get much encouragement at a younger age to learn mathematics, science and engineering and join related careers.

The WIE group of the chapter has initiated a program to train and encourage about 15 girls from a local orphanage in Mysore called “Bapuji Children Home.” Volunteers from the IEEE SJCEWIE group visit the orphanage every week and help them get acquainted with basic tools of computer like MS Office, World Wide Web, etc. They also help them with their academics by solving their doubts in Mathematics and Science. Personality development is given due importance and several supporting activities for the same are conducted. As a part

of this helping program, IEEE-SJCE alumni have donated computers, work books, stationary materials and essential garments for the girls.

“Our long term goal is to encourage these girls to take up engineering as their career. For which, we have been striving to create interest in them for Mathematics and Science alongside acquainting them with computers,” says Rachitha. S, leader of the IEEE-SJCE WIE group.

International Workshop on Future Trend of Nanoelectronics: WIMNACT 39

–by T. Mogmi and Hiroshi Iwai

International Workshop on Future Trend of Nanoelectronics: WIMNACT 39, co-sponsored by the IEEE EDS

Japan Chapter, ECS Japan Section and Tokyo Institute of Technology, was held at Suzukake Hall in Tokyo Institute of Technology, Yokohama, Japan on February 7, 2014.

At the opening session, Dr. T. Mogami, AIST, PRTEA, IEEE ED Japan Chapter Chair, and Prof. H. Iwai, Tokyo Institute of Technology, vice-chair of ECS Japan Section, gave the greetings and introductions of the EDS Japan Chapter and ECS Japan Section, respectively. Technical sessions were chaired by Professors. H. Wakabayashi and K. Kakushima both from Tokyo Institute of Technology, and current status and future possibility of electron and opt devices for various applications including logic and power were presented and



Attendees and presenters of WIMNACT 39

active discussions took place through many questions and comments. The speakers were, Dr. T. Mogami, Prof. M. Liu, of Institute of Microelectronics, Chinese Academy of Sciences, Prof. Y. Shi, Nanjing University, K. Tsutsui, Tokyo Institute of Technology, Prof. Z. Dong, University of Science and Technology of China, Prof. H. Wong, City University of Hong Kong, and Prof. H. Iwai.

Following the speakers were 36 poster presentations given by young researchers and students. The best poster paper awards were evaluated by the award evaluation committee and they were given to Dr. T. Kawanago, Mr. C. Dou, Mr. H. Oomine, and Mr. T. Ohashi. The workshop provided a good opportunity for the young researchers and students to interact with the world's top researchers.

Report on the 38th WIMNACT in Madurai

—by N. Mohankumar and Hiroshi Iwai

The Mini Colloquium WINMACT 38 was organized by the IEEE ED Madras Chapter at Thiayagaraja College of Engineering, Madurai, India, December 27–28, 2013. The MQ had 5 speakers including EDS DLs on the first day which covered the latest trends in device technology. Prof. Hiroshi Iwai from Tokyo Institute of Technology, Japan, Prof. Edward Chung, and Dr. Yuen Yee Wong from NCTU, Taiwan, Prof Chandan Sarkar from Jadavpur University Kolkata, India, and Prof. N. Mohan Kumar, SKP Engineering College, Thiruvannamalai, India. About 200 participants including teaching faculty, researchers, and

graduate students from various engineering institutions attended the event. Prof. Abaikumar and Prof. Sukanesh of Thiayagaraja College welcomed the speakers and the attendees. The sessions included details in the recent trends in MOSFETs, HEMTs, and III-V Semiconductors. There was a lot of interaction between the attendees and the speakers.

The second day had 5 speakers, Prof. S. Rajaram, Prof. N. B. Balamurugan, Prof. D. Gracia Nirmala Rani, Mrs. Vimala, Prof. K. Kalyani of TCE, Madurai and the topics of discussion were on the various VLSI architectures, Fabrication issues and Modelling concepts of different Nano devices. The two day workshop really benefited the student community and research scholars.

IEEE DAY 2014: SAVE THE DATE

The next annual IEEE Day will take place on 7 October 2014. It is never too early to start planning your event. Some suggestions to get you started:

- Recruit Section ambassadors to promote your event/ member engagement
- Raise local funding for event(s)
- Reach out to Industry/Academia to identify guest speakers while promoting IEEE
- Promote your event in Section newsletters, Region/ Section websites, local newspapers

IEEE Day events should focus on a new technology and reflect IEEE's core purpose—to foster technological innovation and excellence for the benefit of humanity.

Post your event, and learn more about IEEE Day at <http://www.ieeeday.org>.



REGIONAL NEWS

USA, CANADA & LATIN AMERICA (REGIONS 1-6, 7 & 9)

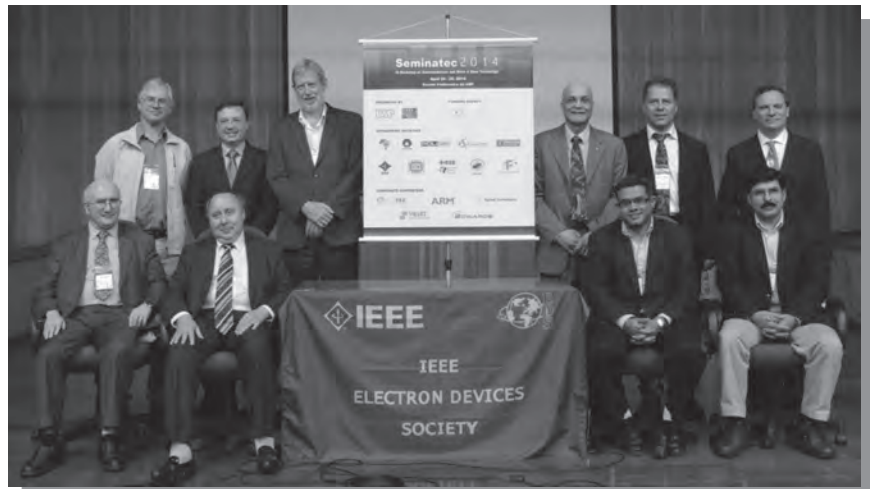
ED South-Brazil

—by Joao Antonio Martino

The ninth Workshop on Semiconductors and Micro & Nano Technology – SEMINATEC 2014—was held April 24–25, 2014, at the University of Sao Paulo (USP), Brazil. The purpose of SEMINATEC is to promote the interaction among industry, academy, research and development centers, government and students, all looking for real opportunities towards improving semiconductor and micro & nano technologies, research, and education. This year SEMINATEC was organized by the University of Sao Paulo (USP) with support and funding from the EDS and SSCS South Brazil chapters, EDS and IEEE UNICAMP's and FEI's student chapters, the Integrated Systems Laboratory (University of São Paulo) and the INCT NAMITEC Science & Technology National Institute.

More than a hundred and thirty participants attended SEMINATEC 2014 from academia, research institutes and industry. Such relatively high attendance reflects the enormous success of its organization, and indicates the substantial and growing interest over the years. This year SEMINATEC's two day intense program was centered around six overview lectures, four of them by EDS Distinguished Lecturers, one by a SSCS Distinguished Lecturer, and one from a research institution:

- 1) "Biosensors – Having Fun with Engineering and the Sciences" by Prof. Jamal Deen, McMaster University, Canada (EDS DL);
- 2) "Non Silicon CMOS Devices: Research Curiosity or Key to Future



SEMINATEC 2014 Lecturers and organizing committee members, from left to right, sitting: Eddy Simoen, Cor Claeys, Suman Datta, Durga Misra. Standing: Wilhelmus Van Noije, Marcelo Pavanello, Jacobus Swart, Jamal Deen, Payam Heydari, Joao Antonio Martino (General Chair)



SEMINATEC 2014 Poster Presentations Authors at University of Sao Paulo, Brazil

- Products?" by Prof. Cor Claeys, K.U. Leuven and Imec, Belgium (EDS DL);
- 3) "High-K Gate Stack and Reliability Requirements for Sub-16 nm CMOS Technology," Prof. Durga Misra, New Jersey Institute of Technology, USA (EDS DL);
- 4) "Beyond Silicon: Transistors for the Future" by Prof. Suman Datta, Pennsylvania State University, USA (EDS DL);
- 5) "Fully Integrated Millimeter-Wave Imaging in Silicon: Challenges and Opportunities" by Prof.

- Payam Heydari, University of California, USA (SSCS DL);
- 6) "Strain characterization and simulation for MOSFETs with embedded source/drain stressors" by Dr. Eddy Simoen, Imec, Belgium.

In addition to the scientific lectures, five semiconductor companies were invited to give half hour presentations describing their activities and demands for research and human resources to academia and industry in the region. The invited speakers from the companies were Dr. Cristiano

Krug from CEITEC federal research center, Eng. Cleber Figueira (Smart Modular Technologies), Msc. Vera Bier (Sansung), Eng. Mauricio Kobayashi (Agilent Technologies) and Dr. Eric Fabris (IC Brazil).

There was also a Poster Session where fourth selected technical papers were presented and discussed. SEMINATEC 2014 included a cocktail reception offered to all the participants, as well as a Panel Discussion Session about the "Interaction between universities and industries." More details are available at <http://www.psi.poli.usp.br/seminatec2014>.

~Francisco J. Garcia Sanchez, Editor



Prof. Enrico Sangiorgi (front row; third from left) and Dr. Werner Weber (back row, third from left) together with Prof. Ali Rezazadeh (front row, middle) and some of the Manchester University delegates

EUROPE, MIDDLE EAST & AFRICA (REGION 8)

ED Manchester University

–by Emerson Sinulingga and Ali Rezazadeh

To celebrate their first anniversary, the ED Manchester University Student Chapter, chaired by Emerson Sinulingga, recently hosted two EDS Distinguished Lectures. Prof. Enrico Sangiorgi of the University of Bologna, Italy, spoke about Micro- and Nano-systems for Energy Harvesting and Dr. Werner Weber of Infineon, Germany, gave an industrial viewpoint of Three-Dimensional Stacking of Silicon Chips. The talks formed part of the Chapter's ongoing activities to update members with the latest technologies in the field of electronic devices. An audience of 35 university students and staff members attended the event and the feedback received from the delegates was universally positive. Following requests from a number of attendees, future events are to be arranged. This event was made possible with the generous support of the IEEE Electron Devices Society and the IEEE UKRI (AP/ED/MTT/PHO) Joint Society Chapter (Prof. Ali Rezazadeh—Chair).

ED Scotland

–by Jonathan Terry

This month sees the end of the term of office of ED Scotland's inaugural chair, Prof. David Cumming. During his tenure, David has administered a busy timetable of social events, lectures, industrial visits and a very successful mini-colloquium on Microsystems, which the Chapter plans to be the first of an annual MQ series. He has also overseen a 20% rise in the Electron Devices Society membership in Scotland since the formation of the Chapter. In one of his last official acts, David recently hosted a Distinguished Lecture at



EDS Distinguished Lecturer, Prof. John Robertson of the University of Cambridge (left). Newly-elected Chapter Chair of ED Scotland, Prof. Anthony Walton of the University of Edinburgh (right)

the University of Glasgow. Professor John Robertson of the University of Cambridge spoke in front of an appreciative audience on the subject of *Interface State Passivation at InGaAs and GaN, high-k CMOS Devices*.

Earlier this year, elections for the Chair-Elect were undertaken by the Chapter's membership, with a unanimous vote seeing Professor Anthony Walton of the University of Edinburgh being elevated to the position. From July 1st, Anthony takes on the role of Chapter Chair and he is looking forward to building on the strong position that David Cumming's time in office has left the Chapter in. Meanwhile, David will continue to play an active part in the growth of the Scottish Chapter as well as carrying on his role as Associate Editor of the *IEEE Transactions on Biomedical Circuits and Systems*.

~Jonathan Terry, Editor

ED Spain

–by Benjamin Iñiguez Nicolau

The NEPHOS (Nanoelectronic and Photonic Systems) Group of the Department of Electronic Electrical and Automatic Control Engineering of

ASIA & PACIFIC (REGION 10)

ED Beijing

—by Ming Liu

On January 14, 2014, Prof. Steve S. Chung from the National Chiao Tung University of Taiwan (NCTU) visited the ED Beijing Chapter. With the Chapter's arrangement, he delivered an EDS Distinguished Lecture entitled *"The Logic CMOS Process-based SONOS Memory"* in the Institute of Microelectronics of Chinese Academy of Sciences (IMECAS). The event was hosted by Prof. Ming Liu from IMECAS, the vice Chapter Chair. There were more than 30 attendees of local professionals and graduate students from the Beijing Chapter.

Prof. Steve first introduced the concept of using SONOS-typed cell in the past will be described. Various developments of the OTP cell in the past will be described. Then, a real example on a CMOS process compatible SONOS-typed cells with 2-bit per cell capability will be demonstrated. Finally, the operation schemes and cell reliabilities will be addressed. The new points of his research on the logic CMOS process-based SONOS memory made a big splash and reached a wide discuss.

After the lecture, a symposium was held with the attendance of researchers from the Laboratory



IEEE EDS Mini-Colloquium Distinguished Lecturers (left to right), Prof. Dimitris Ioannou, Prof. Cor Claeys, Prof. Michael Östling, Prof. Sorin Cristoloveanu, Prof. Benjamin Iñiguez (EDS SRC Vice-Chair—Region 8)

the Universitat Rovira I Virgili (URV, Tarragona, Catalonia, Spain) and the ED Spain Chapter organized two international events in Tarragona related to electron devices:

The 11th Graduate Student Meeting on Electronic Engineering, June 27–28, 2013, an annual event devoted to graduate students, combines plenary talks by prestigious researchers and student presentations. The 2013 edition had six plenary presentations, with one by Dr. Magali Estrada, an EDS Distinguished Lecturer (DL). Dr. Estrada's talk entitled, *"Modeling amorphous metal oxide semiconductor thin film transistors,"* presented her latest work in the novel field of oxide TFTs, which are of great interest for many electronic applications.

10th Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits (EUROSOI 2014), January 27–29, 2014, was organized into a short-course (day 1) and a 2 day conference (days 2 and 3). An IEEE EDS Mini-Colloquium took place on the first day with the participation of four IEEE EDS Distinguished Lecturers, who presented their work on SOI technology:

- Prof. Cor Claeys from IMEC, Belgium, conducted a lecture about *"Process Challenges for Advanced Ge CMOS Technologies;"*
- Prof. Sorin Cristoloveanu, from INPG, France, gave a talk entitled

"From Floating-Body Memory to Unified Memory on SOI;"

- Prof. Michael Östling, from KTH, Sweden, targeted *"Fabrication challenges for sub-10 nm technology nodes;"*
- Prof. Dimitris Ioannou, from George Mason University, USA, addressed *"ESD protection of FD and MuG SOI CMOS chips."*

All presentations will be available for download for free on the conference website, <http://tarragona2014.eurosoi.org/iisstart.htm>.

Apart from the tutorial, Professor Hiroshi Iwai (Tokyo Institute of Technology), an invited speaker from the EUROSOI 2014 workshop, gave an EDS DL *"nNnoCMOS Technology,"* at the Universitat Rovira i Virgili on January 30th.

~Jan Vobecky, Editor



Prof. Steve S. Chung (lecturer, first row, 5th from left), and Prof. Ming Liu (first row, 3rd from left) with student members

of Nanofabrication and Novel Device Integration Technology of IMECAS. Both sides introduced their recent works and had an effective discussion.

ED/SSC Nanjing

—by Zhiqiang Zhang

The IEEE ED/SSC Nanjing Chapter recently sponsored one distinguished lecture at Key Laboratory of MEMS, of the Ministry of Education, Southeast University, Nanjing, China.

On January 8, 2014, Dr. Héctor J. De Los Santos, who serves as the vice president of operation in IntelliSense Software Corporation and is one of the distinguished lectures of the IEEE ED society, was invited to give a lecture entitled “Applications and Trends in RF MEMS.” He explained what RF MEMS is and presented an overview

of RF MEMS development for revolutionizing RF communications. Then he reported the basic theory, packaging, and typical applications of RF MEMS technology, and discussed the challenge to be encountered. In this lecture, he also introduced some typical RF MEMS passive devices which are based on micromachining fabrication techniques and have good RF performances, e.g. capacitors, inductors, transmission lines and switches. These RF MEMS devices showed great potential application opportunities for mobile multimedia communications, e.g. wireless transceivers and routing networks, instead of active and off-chip devices. Finally, Dr. De Los Santos answered some questions from students and shared his research experience with attendees.

ED University of Chinese Academy of Sciences Student Chapter, Beijing

—by Xiaoxin Xu and Wei Wang

The newly formed ED Student Branch Chapter at the University of Chinese Academy of Sciences (UCAS), was inaugurated by EDS Vice-President of Regions and Chapters, Prof. Xing Zhou, of Nanyang Technology University Singapore on April 8, 2014. Prof. Zhou also visited the Institute of Microelectronics, Chinese Academy of Sciences (IMECAS). The Chapter held a short forum to celebrate the formation, with Prof. giving an introduction to the IEEE EDS and its activities. Chapter Advisor Tianchun Ye, Director of IMECAS, encouraged more students to participate in the student chapter and its activities. Prof. Ming Liu, Dr. Jianhui Bu and Gaobo Xu,



Prof. Xing Zhou (9th from left), Director Tianchun Ye (10th from left), and Prof. Ming Liu (11th from left) with the attendees of the DL talk

from IMECAS also talked about their experiences as IEEE Members and gave advice for the new chapter.

Prof. Xing Zhou also gave a Distinguished Lecture entitled of "A Unified Compact Model for GaN-Based HEMTs" for the members of the newly established student chapter, as well as other students from IMECAS.

~Mansun Chan, Editor

ED Kansai

–by Michinori Nishihara

The ED Kansai Chapter held a feedback meeting from the 2013 IEDM with about 20 students and members from academia and industries. The meeting was held at the Osaka Institute of Technology Umekita Knowledge Center, in Osaka, Japan, January 29, 2014. The following two researchers reported: Dr. Yasushi Noda of Panasonic, on Silicon and related sessions and Dr. Munetaka Noguchi of Mitsubishi Electric Corporation, on power and compound semiconductor sessions.

Dr. Noda reported that based on clear market trend toward tablets and smart phones there were more

attention to Low Power technology for mobile SoC. Industry is pushing lithography limit down to 22 nm, 14 nm then less than 10 nm to get not only higher density but also lower power. However, since it is getting harder and harder to push the lithography limit they are looking for Beyond-CMOS technology such as Graphene or Dichalcogenide nanosheet like MoS₂ or WS₂. Dr. Noda also emphasized there were more papers on Tunneling FET using non-Si materials.

Dr. Noguchi reported on increasing number of papers on compound

based CMOS technology including newly reported InGaAs on Si MOS-FET. As for power devices GaN is still dominant compared to SiC or Ga₂O₃. Both speakers covered a wide range of technology and gave us excellent reports of IEDM2013.

After the IEDM 2013 feedback meeting, we held the annual general meeting to review activities of ED Kansai in 2013 and to discuss plans for 2014.

Also discussed were plans for the upcoming 2014 IMFEDK international conference, which is to be cosponsored with the Solid-State Circuits



Dr. Yasushi Noda, speaker



Dr. Munetaka Noguchi, speaker



ED Kansai Chapter members and speakers

Society Kansai Chapter on June 19–20 in Kyoto, Japan. Please check www.imfedk.org for more information.

~Kuniyuki Kakushima, Editor

ED/SSC Bangalore

–by Janakiraman V

The ED/SSC Bangalore Chapter organized two events during the first quarter of 2014. A Distinguished Lecture by Prof. Vijay Arora on “*Nanoelectronics-Quantum Engineering of Low-Dimensional Nanoensemble*,” was held at Indian Institute of Science, Bangalore, February 19, 2014. The talk was attended by professionals from academia IISc, JN-CASR and M S Ramiah School of

Advanced Studies and industry, IBM and CDAC.

The chapter hosted a full day short course on Nanoelectronics on February 20, 2014, jointly with Don Bosco Institute of Technology, Bangalore. The course was attended by 122 participants from academia and industry.

ED NIST Student Chapter, Berhampur

–by Ajit Kumar Panda

The EDS NIST Student Chapter organized a Mini Colloquium February 22, 2014, on advancements in electron devices at NIST Auditorium. More than 110 delegates including faculty

members and graduate students from various institutions and Berhampur University attended the full day program which had four talks given by EDS Distinguished Lecturers.

Prof. M Jagdish Kumar of IIT-Delhi gave the first talk on “*Perspective on the evolution of semiconductor manufacturing: an Innovative Approach*.” Prof. M K Radhakrishnan, of NanoRel gave an introduction to EDS activities and importance of DL programs, followed by his technical talk on “*Challenges in Nano Silicon Devices and Interface Interactions*.” Prof. G N Dash of Sambalpur University talked on “*Trends in Active 2T Microwave Devices*.” The last talk by Prof. C K Sarkar of Jadavpur University was on “*Advanced Hetero-structure based Nano-Scale MOSFETs*.”

On March 22, 2014, the chapter organized a one day seminar on “*Recent Development in Photonic Devices for Communications and Sensor Applications*,” by Prof. T. Srinivas of IISc Bangalore, which attracted 35 participants and included faculty members and M Tech students.

ED Calcutta

–by Soumya Pandit

The ED Calcutta Chapter sponsored the National Workshop on Advanced Nano Device and its Applications,



Attendees of Prof. Arora's short course at DBIT, Bangalore



Participants and Distinguished Lecturers at the NIST DL-MQ program



Speakers at the Nano Device workshop—ED Calcutta Chapter



Prof. Nandita Dasgupta and participants of the seminar held by the ED University of Calcutta Student Chapter

January 17–18, 2014, organized by Silicon Institute of Technology, Bhubaneswar, India. The workshop presented a comprehensive picture of state of the art VLSI devices and its applications in integrated circuit design. There were 3 tutorial sessions, conducted by Dr. Soumya Pandit, Prof. Chandan K. Sarkar and Dr. Angsuman Sarkar. Apart from theoretical lectures, hands-on training on TCAD simulation was provided to the participants. More than 150 participants including graduate students, research scholars and faculty members attended. This was one of the outreach programs of the Chapter.

ED HIT-K Student Chapter, Calcutta

–by Swapnadip De and Soumya Pandit

The ED Heritage Institute of Technology Student Branch Chapter, ED Calcutta Chapter and ED University of Calcutta Student Branch Chapter jointly organized a Technical Talk, December 18, 2013, on “Resistance Random Access Memory (RRAM)—Devices (memory & selection device) to Cross Point Array based Circuits,” by Prof. Udayan Ganguly of IIT Bombay at ECE department, HIT-K. Experimental demonstration of an epitaxial Si vertical diode based selection device for bipolar RRAM was presented. Device

compact modelling and memory array performance modeling were also discussed. The talk was attended by more than 50 participants including graduate and undergraduate students and faculty members.

ED University of Calcutta Student Chapter, Calcutta

–by Sarmista Sengupta and Soumya Pandit

The chapter organized a one day seminar on Microelectronics and MEMS devices on March 25, 2014, in the Institute of Radio Physics and Electronics. The seminar was conducted by Prof. Nandita Dasgupta of IIT Madras. The main emphasis was the fundamental issues related to advanced MOS transistors including leakage current analysis and the various advanced MOS devices. The fabrication of indigenous MEMS structures were

also discussed at length. A total of sixty-two participants attended the program. The session was highly beneficial for the students.

ED Delhi

–by Mridula Gupta and Manoj Saxena

During the first quarter of 2014, the Chapter organized one technical talk, one short course and supported the National Workshop on Optics and Optical Communication. The Technical talk on January 6th, “Analysis of Electromagnetic Fields in Inhomogeneous Media by Fourier Series Expansion Methods—The case of a Dielectric Constant Mixed a Positive and Negative Regions,” by given by Prof. Tsuneki Yamasaki of Nihon University, Tokyo,



Prof. Yamasaki with EDS Delhi Chapter members



Attendees of Prof. Vijay Arora's short course at the ED Delhi Chapter

Japan. More than 60 participants attended his talk held at University of Delhi South Campus. The short course on January 28th was given by Prof. Vijay Arora of Wilkes University at the SP Jain Centre of Delhi University. The topic was "Nanotechnology Journey from Quantum Physics to Nanoengineering," and more than 120 people from various organizations attended.

The workshop on Optical communications supported by the Delhi Chapter was held at Maharaja Agrasen College, Delhi from March 8–10, 2014. It attracted more than 240 participants from 29 different institutions of both academia and industry. The program comprised of 13 invited lecturers and fiber optics software demonstrations.

ED Malaysia Kuala Lumpur

–by P Suthitha Menon

The Annual General Meeting of the ED Malaysia Chapter was held January, 23, 2014, at the Berjaya Times Square Hotel, Kuala Lumpur. Prof. Nizar Hamidon from Universiti Putra Malaysia (UPM) was elected as the Chapter Chair and Prof. Badariah Bais from Universiti Kebangsaan Malaysia (UKM) was elected as Vice-Chair. Prof. P. Suthitha Menon from Institute of Microengineering and Nanoelectronics (IMEN) and Prof. oslina Sidek from Universiti Putra Malaysia (UPM) were elected to be the Secretary and Treasurer respectively. Several members from various universities and industries in

Malaysia were also elected to be part of the committee.

The 11th IEEE International Conference on Semiconductor Electronics (ICSE2014) conference, sponsored by the Chapter will be held in Kuala Lumpur August 27–29, 2014.

ED SJCE Student Chapter, Mysore

–by D Sushamshushekar and C R Venugopal

The IEEE ED SJCE Student Chapter organized its annual mega event, Cyberia-14 from March 14–16 2014. The event was launched on the evening of March 14th where Dr. M K Radhakrishnan, EDS BoG Member and Region 10 SRC Vice-Chair, was the chief guest and Mr. Harish



ED Malaysia Chapter ExCom 2014



Panelists and the moderator during the panel discussion at SJCE Chapter

Mysore, Director of IEEE India Operations was the Guest of Honor. Annual activity reports comprising many events and competitions were presented. Many technical programs were held during the day, with cultural events held in the evening.

A Panel Discussion on *"The rising demands of various facets of industry need an engineer's knowledge domain to be as wide and deep as ever. Is an undergraduate degree in engineering becoming too preliminary?"* was held in which Prof. T K Ramkumar of SJCE was the moderator. Seven panelists from academia and industry include Dr. Syed Shakeeb Ur Rehman, Principal SJCE, Dr. Asok Rao and Dr. M M Nayak of IISc Bangalore,

Mr. Harish Mysore of IEEE India Operations, Ms. Malathi Srinivasan of IBM, Dr. M K Radhakrishnan of NanoRel and Mr. Vijay Koppad of Red Hat. The discussion was highly elucidating which made students realize not to rely just on the curriculum but to work on more practical and application oriented aspects.

ED NIT Student Chapter, Silchar

–by T R Lenka

The Chapter organized a one day Seminar on *"Interdisciplinary Research on Biomedical Engineering"* on August 26, 2013, at Department of Electronics and Communication Engineering, NIT Silchar. Prof. Sneha Anand, Centre for Biomedical Engineering, IIT Delhi,

Prof. Ajit Kumar Banthia, IIT Kharagpur and Dr. Santanu Dhara, Biomaterials and Regenerative Medicine Group, School of Medical Science and Technology, IIT, Kharagpur, delivered lectures on Biomedical Engineering, Biomaterials and Biosensors.

IEEE EDS Distinguished Lectures, organized by the Chapter on September 10, 2013, at NIT Silchar had two speakers. Prof. Ramgopal Rao of IIT Bombay, EDS DL and Region 10 SRC Vice-Chair delivered the talk on *"Nanoelectronics"* and Prof. Richard Pinto of IIT Bombay delivered the talk on *"Pulsed Laser Deposition-25 Years Young."* M.Tech students, PhD scholars and faculty of Department of Electronics and Communication



Professors Richard Pinto and Ramgopal Rao along with participants at NIT Silchar



Official release of the proceedings of ICAEE conference at the VIT Vellore Chapter

Engineering, NIT Silchar, attended the talks.

REL/CPMT/ED Singapore

—by Gan Chee Lip

The Chapter's flagship conference, the 21st International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), was held at Marina Bay Sands Singapore, June 30—July 4, 2014. The conference is technically co-sponsored by the IEEE Electron Devices Society and the IEEE Reliability Society.

IPFA 2014 is devoted to the fundamental understanding of the physical mechanisms of semiconductor device failures and issues related to semiconductor device reliability, yield and performance, especially those related to advanced process technologies. It comprises of 2-day tutorials and 3-day plenary oral sessions with Keynote Addresses and Invited Papers by renowned speakers. Also, the technical program includes Best Paper exchanges from the 39th International Symposium for Testing and Failure Analysis (ISTFA 2013) and 24th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2013).

An equipment exhibition with exhibitors of FA equipment companies will be held in conjunction with IPFA. Also, the "Art of Failure Analysis"



Prof. Simon Delenibous inaugurating the ICAEE conference by lighting the lamp

photo contest which is an integral part of IPFA provides FA enthusiasts a platform to showcase their best FA photos. Voted winners will win prizes and have their photos published in IEEE Spectrum. More details can be obtained at: <http://iee-ipfa.org/>

ED VIT Student Chapter, Vellore

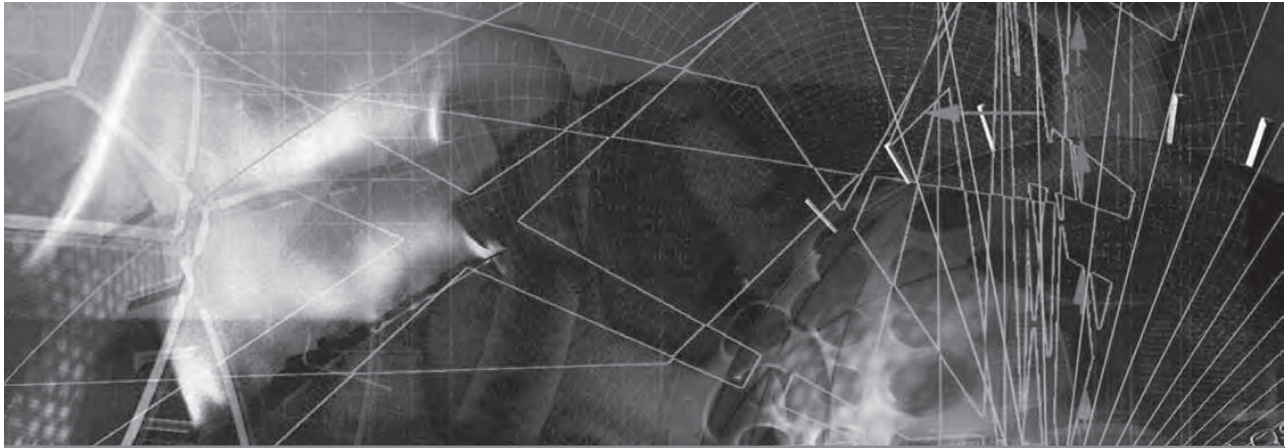
—by Partha Mallick

The Chapter along with VIT University organized the 1st International Conference on Advances in Electrical Engineering (ICAEE) during January 9–11, 2014, at VIT University, Vellore, India, with Dr. Simon Delenibous, IEEE Fellow and EDS Distinguished Lecturer as the Guest of Honor. Two hundred, fifty-five participants from 18 countries attended this conference and heard Dr Simon's

keynote talk on "Future Micro/Nano-Electronics: Towards Full 3D and Zero Variability." Among the other speakers, was also Prof. Devki N. Talwar from Indiana University of Pennsylvania, who spoke on Physics of novel III-nitride based devices. A preconference tutorial was held January 8th. Many eminent researchers from all over the world presented their research studies at the conference. A total of 431 research papers were received with 149 papers accepted for presentation.

Dr. Partha S. Mallick, IEEE EDS Student Chapter Advisor was the General Chair of the Conference and Dr. D. P. Kothari, IEEE Fellow as the Technical Chair.

~M.K. Radhakrishnan, Editor



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EDS MEETINGS CALENDAR

(AS OF 06 JUNE 2014)



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[HTTP://EDS.IEEE.ORG](http://eds.ieee.org). PLEASE VISIT.

2014 20th International Conference on Ion Implantation Technology (IIT)

Abstract submission deadline: 07 Feb 2014
 Final submission deadline: 19 May 2014
 Notification of acceptance date: 24 Apr 2014

26 Jun - 04 Jul 2014

Portland Hilton
 921 SW 6th Ave.
 Portland, OR, USA

2014 IEEE 21st International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)

Abstract submission deadline: 17 Jan 2014
 Final submission deadline: 09 May 2014
 Notification of acceptance date: 14 Mar 2014

30 Jun - 04 Jul 2014

Marina Bay Sands
 10 Bayfront Avenue
 Singapore

2014 21st International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)

Abstract submission deadline: 24 Mar 2014
 Final submission deadline: 12 Mar 2014
 Notification of acceptance date: 30 Apr 2014

02 Jul - 04 Jul 2014

Ryukoku University
 Avanti Kyoto Hall
 31 Nishi Sanno-cho
 Higashi Kujo
 Minami-Ku
 Kyoto, Japan

2014 11th International Workshop on Low Temperature Electronics (WOLTE)

Abstract submission deadline: 28 Mar 2014
 Final submission deadline: 28 Mar 2014
 Notification of acceptance date: 14 Apr 2014

07 Jul - 09 Jul 2014

Phelma-Minatec
 3 Parvis Louis Néel
 Grenoble, France

2014 27th International Vacuum Nanoelectronics Conference (IVNC)

Abstract submission deadline: 17 Mar 2014
 Final submission deadline: 31 May 2014
 Notification of acceptance date: 31 Mar 2014

07 Jul - 10 Jul 2014

RAMADA Hotel
 Regina Titlis
 Dorfstrasse 33
 Engelberg,
 Switzerland

2014 IEEE International Nanoelectronics Conference (INEC)

Abstract submission deadline: 31 Mar 2014
 Final submission deadline: 31 May 2014
 Notification of acceptance date: 30 Apr 2014

28 Jul - 31 Jul 2014

Hokkaido University
 Conference Hall
 Kita 8-Jyo Nishi 5-
 chome
 Kita-Ku
 Sapporo, Japan

2014 Lester Eastman Conference on High Performance Devices (LEC)

Abstract submission deadline: 31 May 2014
 Final submission deadline: 22 Aug 2014
 Notification of acceptance date: 12 Jun 2014

05 Aug - 07 Aug 2014

Atrium Auditorium
 PH101, Philips Hall
 Cornell University
 Ithaca, NY, USA

2014 29th Symposium on Microelectronics Technology and Devices (SBMicro)

Abstract submission deadline: 31 Mar 2014
 Final submission deadline: 01 Jun 2014
 Notification of acceptance date: 18 May 2014

01 Sep - 05 Sep 2014

Mercure Hotel
 Av Santos Dumont
 1500
 Bairro Praia de
 Atalaia, Sergipe
 Aracaju, Brazil

2014 36th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD) Abstract submission deadline: 10 Jan 2014 Final submission deadline: 13 Jun 2014 Notification of acceptance date: 24 Feb 2014	07 Sep - 12 Sep 2014	Westin La Paloma 3800 East Sunrise Drive Tucson, AZ, USA
2014 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) Abstract submission deadline: 07 Apr 2014	09 Sep - 11 Sep 2014	Mielparque Yokohama 16, Yamashita-cho Naka-ku Yokohama, Japan
2014 IEEE Custom Integrated Circuits Conference - CICC 2014	14 Sep - 17 Sep 2014	DoubleTree Hotel San Jose, CA, USA
ESSDERC 2014 - 44th European Solid State Device Research Conference Abstract submission deadline: 10 Apr 2014 Final submission deadline: 30 Jun 2014 Notification of acceptance date: 31 May 2014	22 Sep - 26 Sep 2014	Palazzo del Casino LungomareMarconi, 30 Venice Lido, Italy
2014 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM Abstract submission deadline: 28 Apr 2014 Final submission deadline: 18 Jul 2014 Notification of acceptance date: 16 Jun 2014	28 Sep - 01 Oct 2014	Coronado Island Marriott Resort & Spa 2000 2nd Street Coronado, CA, USA
2014 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)	06 Oct - 09 Oct 2014	Westin San Francisco Airport 1 Old Bayshore Highway Millbrae, CA, USA
2014 International Semiconductor Conference (CAS) Final submission deadline: 02 Jun 2014 Notification of acceptance date: 15 Jul 2014	13 Oct - 15 Oct 2014	Rina Sinaia Hotel 8, Carol I, Str Sinaia, Romania
2014 International Conference on Computer Aided Design for Thin-Film Transistor Technologies (CAD-TFT) Abstract submission deadline: 31 May 2014 Final submission deadline: 10 Aug 2014 Notification of acceptance date: 30 Jun 2014	15 Oct - 17 Oct 2014	Nanjing, China
2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS) Abstract submission deadline: 02 May 2014 Final submission deadline: 25 Jul 2014 Notification of acceptance date: 13 Jun 2014	19 Oct - 22 Oct 2014	Hyatt Regency La Jolla 3777 La Jolla Village Drive La Jolla, CA, USA

TECHNICAL ACTIVITIES AT IEEE SECTIONS CONGRESS 2014



Rakesh Kumar
IEEE Fellow

Every three years IEEE brings together Section Chairs and representatives from around the world at a Sections Congress. The event this year is scheduled for August 22–24, 2014, in Amsterdam at the RAI Exhibition and Convention Center. This event is organized by the Member and Geographic Activities (“MGA”), is the first such event to be held outside the US, and has a theme of “Inspiring our Leaders of Tomorrow.”

IEEE TA (Technical Activities) will be a major contributor to this year’s Sections Congress and will showcase the building of Technical Communities,” said Professor and IEEE Life Fellow, Dr. Jacek Zurada, 2014 IEEE VP-TA. These activities are being coordinated by an AdHoc Committee chaired by IEEE Life Fellow Dr. Rakesh Kumar, a long-time EDS member, and the past President of the Solid-State Circuits Society.

Key technical events at the SC2014 include 15 “Ignite” presentations – a very special, 5-minute, 20-slide presentation – by representatives of various Technical Societies and Councils highlighting Member Engagement and Technical Community Building through Education, Chapters and Conferences. In addition there will be ten presentations by TA leaders providing introductions to topics such as Smart Cities, other Future Directions initiatives, and industry participation. TA will be hosting a technology-centric reception to showcase video images of contributions from various Societies and Councils. Also, a special lounge area is being set up to enable opportunities for attendees to interact with TA leaders.

“Many representatives from various societies and councils, and IEEE staff have come together to help highlight TA’s contributions at this event. It has been my pleasure to lead this effort. While it has been a lot of work, I feel that this will be a key to furthering cooperation between MGA, TA and other parts of IEEE,” said Dr. Rakesh Kumar.

For more information on the 2014 IEEE Sections Congress: https://www.ieee.org/societies_communities/geo_activities/sections_congress/2014/sections_congress_2014.html