A 1.2V Dynamic Bias Latch-type Comparator in 65nm CMOS with 0.4mV input noise

Harijot Singh Bindra, *Student Member, IEEE*, Christiaan E. Lokin, *Student Member, IEEE*, Daniel Schinkel, *Member, IEEE* Anne-Johan Annema, *Member, IEEE* and Bram Nauta, *Fellow, IEEE*

***Abstract*— A latch-type comparator with a dynamic bias pre-amplifier is implemented in a 65nm CMOS process. The dynamic bias with a tail capacitor is simple to implement and ensures that the pre-amplifier output nodes are only partially discharged to reduce the energy consumption. The comparator is analyzed and compared to its prior-art in terms of energy consumption and input referred noise voltage. First-order equations are presented that show how to optimize the pre-amplifier for low noise and high gain. Both the dynamic bias comparator and the prior-art are implemented on the same die and measurements show that the dynamic bias can reduce the average energy consumption by about a factor 2.5 for the same input-equivalent noise at an input common mode level of half the supply voltage.**

***Index Terms* — Dynamic biasing; charge steering; StrongARM; Latch; double-tail latch-type comparator; Noise; SAR; ADC; Comparator**

I. INTRODUCTION

ANALOG-TO-DIGITAL converters (ADCs), are continuously being pushed to their performance limits and have seen tremendous decrease in their power consumption over the last few years. Due to their highly digital architecture, the SAR ADCs scale with both technology and supply voltage. The Walden Figure of Merit for state-of-the-art SAR ADCs is reduced to below 1fJ per conversion-step. However, 50-60% of their total energy consumption comes from the comparator which does not scale in the same order with supply voltage and technology as for the other digital blocks in a SAR ADC like control logic and DAC switches [1,2,3]. The low voltage operation imposes stringent requirements on the quantization noise, thereby making the reduction in energy consumption for each comparator operation even more challenging.

The StrongARM latch was the first in the class of dynamic comparators, and has been widely used over the years as regenerative comparators. This class of comparator has strong positive feedback enabling fast decisions, has no static power consumption and has full swing outputs [5,6]. However since the StrongARM comparator has a single stage architecture, it requires a large voltage headroom as discussed in [4,6].

Harijot Singh Bindra, Christiaan E. Lokin, Anne-Johan Annema and Bram Nauta are with the Integrated Circuit Design group, University of Twente, 7522NB Enschede, The Netherlands. Daniel Schinkel is with Teledyne DALSA Semiconductors, 7521PT Enschede, The Netherlands and also with the IC Design group, University of Twente.

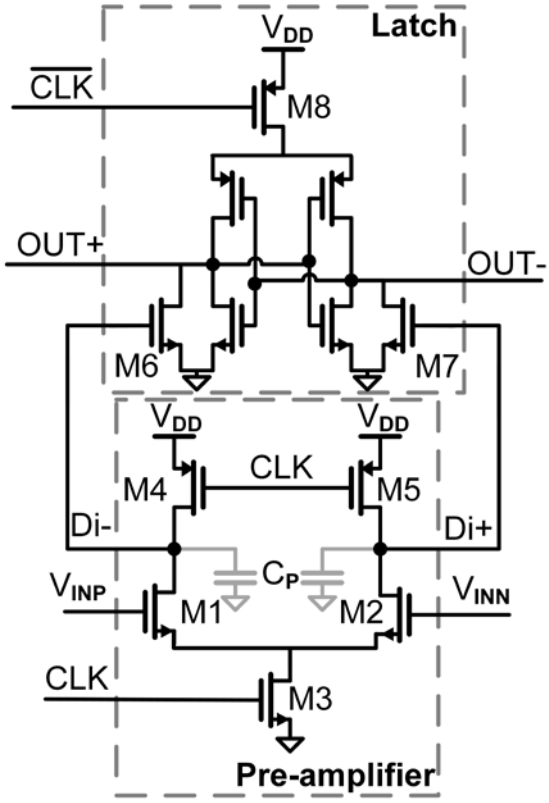

Fig.1 Double-tail latch-type comparator [4]

Furthermore, since there is no isolation between the regeneration latch and the differential input stage, the StrongARM latch suffers from significant kickback as highlighted in [6].

The double-tail latch-type architecture (Fig. 1) presented in [4] mitigated these problems by separating the pre-amplifier stage from the latch. This allows for a greater input common mode range thereby enabling near-V_{DD} operation (for an NMOS input differential pair). In addition, it allows for an extra degree of freedom by providing separate tail transistors: one for the pre-amplifier and one for the latch stage. This provides an independent control of the common mode current for the pre-amplifier and of the regeneration time for the latch stage. The output nodes of the pre-amplifier in the double-tail latch-type comparator discharge completely to ground at the end of comparison. This means that a fixed energy corresponding to a charge packet $2 \cdot C_P \cdot V_{DD}$ is consumed by the pre-amplifier for each comparator operation. The capacitances C_P at each of the pre-amplifier's output nodes (see Fig. 1) also determine the input referred noise [1], so they have to be appropriately sized

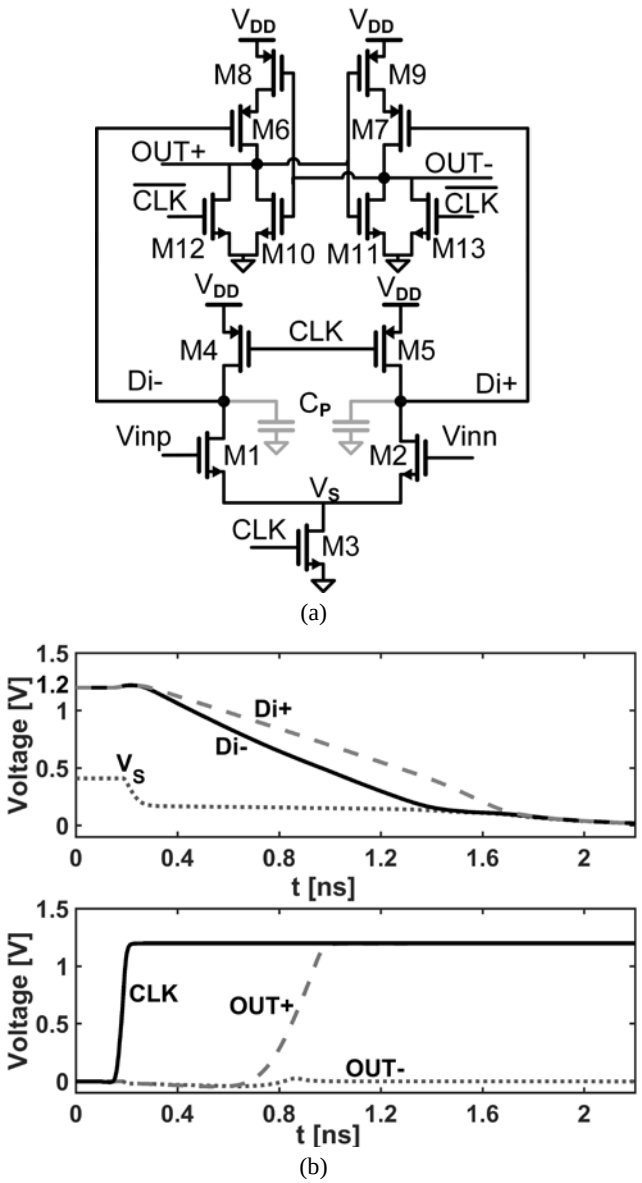

Fig.2 (a) Circuit and (b) Simulated timing waveform of Elzakker's comparator [1] for $|\Delta V_{IN}|$ = 25mV at common mode voltage, V_{CM} equal to 0.6V, V_{DD} = 1.2V.

to attain a certain SNR. As a result, the pre-amplifier constitutes approximately 80% of the total energy consumption of the comparator [1,3,4].

The same holds true for another comparator variant: the Elzakker comparator [1], which is shown in Fig. 2a. The advantage of the circuit in Fig. 2(a) over that in Fig. 1 will be explained in Section II. Based on the circuit of Fig. 2(a), we show that the energy consumption for a given SNR can be reduced through a dynamic bias technique that discharges the output nodes of the pre-amplifier only partially [7]. In this paper we present a detailed analysis of the latch-type comparator with a dynamic bias pre-amplifier (Fig. 3). Also the design methodology and operational details of the dynamic bias pre-amplifier in weak inversion region of operation is compared to the pre-amplifier with switched tail current (Fig. 2) as in the case of Elzakker's comparator. The paper is organized as follows. Section II revisits the double-tail latch-type comparator [4] and its variants (Elzakker comparator [1] and bi-directional comparator [3]), highlighting the various energy reduction techniques for a given SNR requirement. Section III describes the operation of the proposed dynamic bias comparator. Section IV presents the mathematical equation for the input equivalent noise voltage and voltage gain of a pre-amplifier operating in weak inversion and extends it to analysis of the proposed dynamic bias comparator. Section V presents the design methodology and simulation results for both the Elzakker and dynamic bias comparators. Section VI presents the measurement results for both the comparators that were fabricated on the same die for comparing their performance. Section VII summarizes the work with concluding remarks.

II. Prior Art

The double-tail latch-type architecture [4] of Fig. 1 is well suited for low-voltage operation especially for applications like sense amplifier for on-chip data communication, memories etc. which operate at a higher (near V_{DD}) input common mode voltage. However, this architecture suffers from poor optimization of energy consumption for a given SNR due to the fact that the pre-amplifier as well as the regenerative latch start operating at the same time. Since at the start of comparator operation, the differential voltage at the output of pre-amplifier is approximately zero, the latch stage conducts without developing any appreciable SNR. This makes it less attractive for low power applications such as medium to high resolution SAR ADCs. A more optimum solution from the perspective of energy consumption is to delay the conduction of the latch stage, until the time a sufficient voltage gain is developed across the pre-amplifier output nodes.

For use in SAR ADCs, Elzakker et. al, developed a more energy efficient comparator [1] as shown in Fig. 2(a). In it, the pre-amplifier stage is same as in [4], but in contrast to the work in [4], the output of the pre-amplifier is fed to PMOS transistors - M6/M7 which are embedded in the latch stage. Unlike the clocked tail transistor M8 in Fig. 1, there is no explicit tail transistor in the latch stage for the architecture [1] in Fig. 2(a). At the start of comparator operation (Di+/Di- are at V_{DD}), transistors M6/M7 are OFF, which ensures that the latch stage only starts conducting once the output common mode voltage of the pre-amplifier drops below the threshold voltage of the PMOS transistors (M6/M7). Consequently, when the latch stage turns 'ON' it sees a sufficient differential voltage (gain) at its input to perform the regeneration operation.

The energy consumption of the Elzakker comparator can be further reduced by minimizing the pre-charge energy of the pre-amplifier stage. A recently introduced 'bi-directional dynamic comparator' [3] for example splits the pre-amplification in two phases: first charging and then discharging the common-mode. For the bi-directional comparator, two sets of differential pair - one in PMOS and one in NMOS - are used for the pre-amplification, respectively during the charging and the discharging of the output.

The result is that the pre-amplifier nodes are charged to only half the supply instead of the full supply, saving half the energy. However as reported in [3], due to the logic overhead required for reset/latch enable signals and the OR gate to switch from PMOS pair to NMOS pair, the resultant improvement in energy is limited to 33% for the same SNR as in [1].

III. DYNAMIC BIAS COMPARATOR

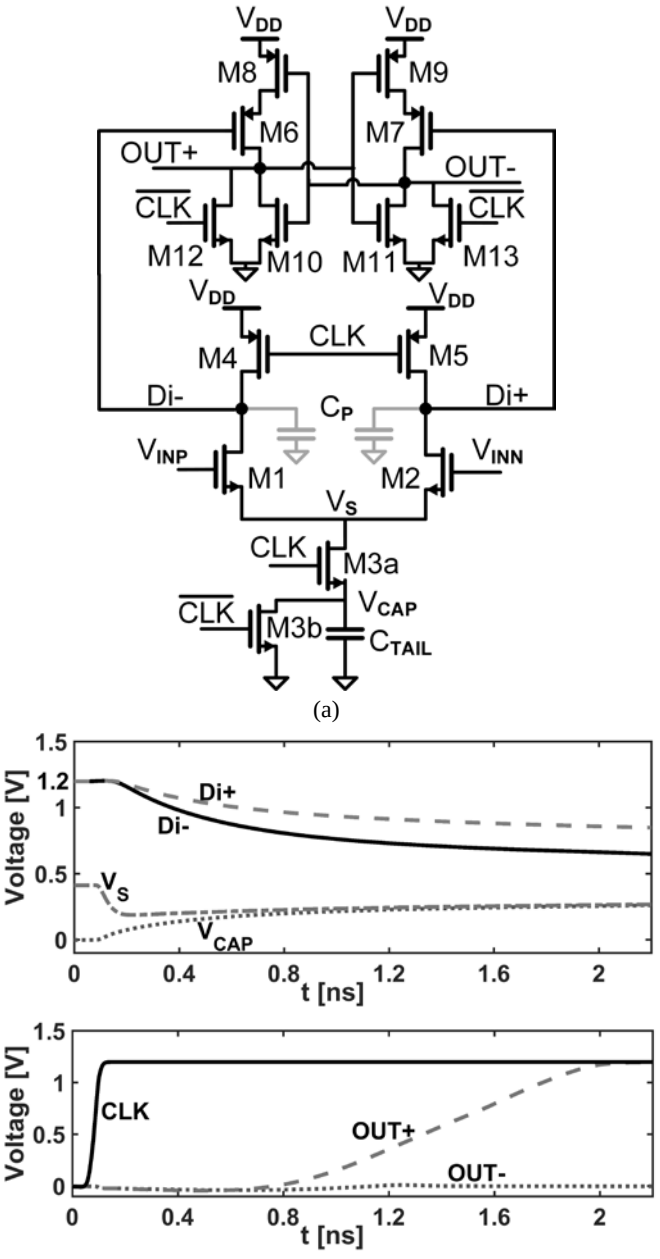

Fig. 3. (a) Circuit and (b) Simulated timing waveforms of the proposed Dynamic Bias Comparator for $|\Delta V_{IN}|$ = 25mV at V_{CM} = 0.6V and V_{DD} = 1.2V

The dynamic bias technique is a relatively simple method to reduce the amount of discharge on the pre-amplifier output nodes (Di+/Di-), with less overhead [7]. It involves the use of a capacitor in the tail of the pre-amplifier, which controls the amount of discharge from the Di+/Di- nodes. The concept of energy bias or dynamic bias was originally proposed by [8] and has been recently used to make low energy charge steering logic [9] for applications in data communication and retiming circuits such as equalizers, clock-data recovery [10].

As shown in [8], dynamic biasing provides an energy efficient biasing mechanism by gradually reducing bias current to operate in the weak inversion region in order to achieve maximum voltage gain for a given charge transfer. Similar to the concept of dynamic biasing, the work done in [11] uses the capacitive degeneration technique to design a linear residue amplifier for pipelined ADCs.

In this paper the concept of dynamic biasing is extended to a double tail latch-type comparator to reduce the energy per bit comparison for a given SNR. The switched-current tail transistor M3 in Fig. 2(a) is replaced by a tail capacitor and a (switch) tail transistor M3a (Fig. 3). The transistor M3b is used to reset the tail capacitor to ground.

The dynamic bias comparator is shown in Fig. 3 along with its timing waveform. During the reset phase, when CLK = 0, the transistors M4 & M5 pre-charge the drain nodes Di+ & Di- to V_{DD}, M12 and M13 reset the latch and the tail capacitor C_{TAIL} is discharged to ground through M3b.

During the comparison phase, when CLK = V_{DD}, all the reset transistors, M3b, M4, M5, M12 and M13 are turned OFF. The tail transistor, M3a turns ON and the capacitances, C_P's on the drain nodes Di+ and Di- start discharging. The common mode current resulting from the discharge of C_P's results in a tail current, I_{TAIL} which charges the tail capacitor C_{TAIL}. This increases the voltage V_{CAP}, which reduces the gate-source voltage, V_{GS} of the differential pair (M1/M2), thereby providing a dynamic bias to the differential pair during the comparison phase.

As the voltage V_{CAP} increases, the gate-source voltage of M1 and M2 reduces until the source voltage reaches the first quenching point, $V_S = \min(V_{INP}-V_T, V_{INN}-V_T)$, where V_T is the threshold voltage of the transistors M1/M2. At this point, one of the input transistors M1/M2 turns off and the drain voltage at that transistor freezes (assuming no sub-threshold conduction). The other transistor continues to discharge its corresponding C_P until the second quenching point, $V_S = \max(V_{INP}-V_T, V_{INN}-V_T)$ is reached. This is in contrast with the Elzakker comparator [1], where both the drain nodes are completely discharged to ground at the end of comparison phase. For the dynamic bias comparator, the voltage V_{D1} and V_{D2} at Di+ and Di- nodes, at the end of comparison phase, depends on the amount of charge transferred to C_{TAIL}. The energy required by the pre-amplifier in the dynamic bias comparator to pre-charge the drain nodes is given as $[2 \cdot C_P \cdot V_{DD}^2 - C_P \cdot V_{DD} \cdot (V_{D1} + V_{D2})]$. This is lower than the conventional pre-charge energy $2 \cdot C_P \cdot V_{DD}^2$ as required in the case of Elzakker's comparator. Since the noise of the first stage (pre-amplifier) dominates [1,12,13], therefore C_P needs to be appropriately sized for a desired SNR and not only consists of the transistor parasitic. The noise power is inversely proportional to C_P as shown in Section IV. The pre-amplifier constitutes around 70-80% of the total energy consumption of the comparator [1,7] and therefore the reduction in comparator's energy consumption by partially discharging pre-amplifier output is quite considerable.

To get the lowest noise at a given current, it is desirable to maximize gm/Id for the input transistors M1 and M2 (elaborated in Section IV), which means that it is desirable to let M1 and M2 operate in the weak inversion region until the latch stage makes a decision. A minimum sized tail transistor M3a is dimensioned, such that its on-resistance ensures that the differential pair is biased near weak inversion at the start of comparator operation. When CLK = V_{DD}, the differential pair starts at a specific tail current, which afterwards decreases

continuously with increasing V_{CAP}. Due to the finite (large) resistance of the tail transistor M3a, the node V_S does not drop to zero instantaneously. The large momentary current also means that the C_{TAIL} initially charges at a fast rate. The gm/Id thus increases with increase in V_{CAP} (decrease in V_{GS}) and achieves its maximum near the second quenching point. In a typical 1.2V supply 10-bit SAR ADC application wherein the differential input voltage to a comparator ranges from near LSB resolution (1mV) to full scale differential (1.2V), the dynamic bias comparator provides an energy efficient charge-biased dynamic pre-amplification mechanism. It operates mostly in the high gain, low input referred noise weak inversion operation region for near LSB input differential voltages and for large input differential voltages it operates with a large overdrive voltage (V_{GS} - V_T) and therefore small propagation delay. However, due to a lower GBW in weak inversion operation, a higher CLK-Q delay is also observed in the case of dynamic bias for small differential input voltages as compared to the Elzakker's comparator [1]. For comparing the performances of the two comparators as depicted in Fig. 2 and Fig. 3, both were fabricated on the same die in a standard 65nm CMOS process. The size of the input differential pair M1 and M2 are the same for both designs to have similar input referred offset. The latch stage is also identical for both the designs.

IV. Mathematical Analysis

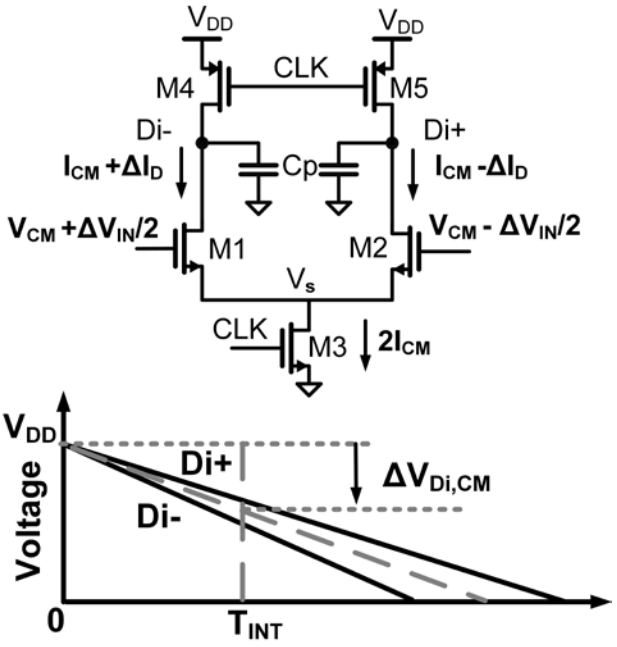

Fig.4. Pre-amplifier and its transient outputs

The work done in [9] presents the voltage gain equations for a "charge-steering latch" wherein the differential pair is operating in strong inversion region. Targeting for applications such as medium to high resolution ADCs, a low input referred noise voltage is desired. According to [1], weak inversion operation is preferred for a low-noise energy-efficient pre-amplifier, although [1] did not provide supporting theory for this statement. Similarly, it is stated in [12] that for the lowest noise, the overdrive voltage of the input transistors should be minimized. First-order approximate relations for voltage gain and noise are given in [9] and [12] respectively using square law transistor models in strong inversion. However, these relations are not valid for V_{GS}-$V_T \leq 0$ for which the strong inversion equations presented in [9,12] predict zero g_m at zero overdrive voltage. In this section, the noise and gain analysis in [1] is extended to weak inversion and quantitatively compared with strong inversion operation. Also the voltage gain and noise equations for the dynamic bias comparator, which has a non-constant tail current, are presented in terms of the capacitor ratio, $\frac{C_{TAIL}}{C_p}$ and output common mode voltage drop $\Delta V_{Di,CM}$.

Voltage gain analysis of constant tail current pre-amplifier

For this analysis, the schematic of Fig. 4 is used. In Fig. 4, T_{INT} is the integration time during which the output common mode voltage of the pre-amplifier discharges by $\Delta V_{Di,CM}$ from the pre-charge voltage V_{DD}, with an average discharge current, I_{CM}. T_{INT} can be written as [1]:

$$\Delta V_{Di,CM}(T_{INT}) = \frac{I_{CM} \cdot T_{INT}}{C_P} \quad (1)$$

The current $\Delta I_D = \frac{g_m \cdot \Delta V_{IN}}{2}$ results in a differential output voltage, ΔV_{Di} across the Di+/Di- nodes during the time T_{INT}. Using $\frac{T_{INT}}{C_P}$ from (1) and neglecting the finite output resistance of M1/M2, this yields

$$\Delta V_{Di}(T_{INT}) = \frac{g_m \cdot \Delta V_{IN} \cdot T_{INT}}{C_P} = \frac{g_m \cdot \Delta V_{IN} \cdot \Delta V_{Di,CM}(T_{INT})}{I_{CM}}$$

where

$$A_V(T_{INT}) = \frac{\Delta V_{Di}(T_{INT})}{\Delta V_{IN}(T_{INT})} = \frac{g_m \cdot \Delta V_{Di,CM}(T_{INT})}{I_{CM}} \quad (2)$$

is the equivalent voltage gain.

Voltage gain analysis of dynamic bias pre-amplifier

For the dynamic bias amplifier, the tail section of the pre-amplifier consists of the switch transistor M3a and capacitor, C_{TAIL} as shown in Fig. 3(a). In addition to ΔI_D, the common mode current, I_{CM} also discharges the capacitor C_P from V_{DD} to an output common mode voltage, $V_{Di,CM}$. Since I_{CM} is not constant for the case of dynamic bias pre-amplifier, (1) cannot be applied directly to obtain A_V as in (2). The output common mode voltage drop can be related to I_{CM} as

$$\Delta V_{Di,CM}(t) = \frac{\int_0^t I_{CM}(\tau) d\tau}{C_P} \quad (3)$$

The current $\Delta I_D = \frac{g_m \cdot \Delta V_{IN}}{2}$ results in a differential output voltage,

$$\Delta V_{Di}(t) = \frac{\int_0^t (g_m(\tau) \cdot \Delta V_{IN}) d\tau}{C_P}$$

The transconductance in weak inversion is [14]

$$g_m(\tau) \simeq \frac{I_{CM}(\tau)}{n \cdot kT/q}$$

Here 'n' is assumed to be relatively constant for small input differential voltage during the integration time in weak inversion [1]. Substituting for $g_m(\tau)$,

$$\Delta V_{Di}(t) = \frac{\Delta V_{IN} \cdot \int_0^t I_{CM}(\tau)\, d\tau}{\left(n \cdot \frac{kT}{q}\right) C_P}$$

Substituting $\frac{\int_0^t I_{CM}(\tau)\, d\tau}{C_P}$ from Eq. (3) and re-arranging yields the voltage gain A_v,

$$A_V(t) = \frac{\Delta V_{Di}}{\Delta V_{IN}} = \frac{\Delta V_{Di,CM}(t)}{n \cdot kT/q} \quad (4)$$

which is the same result as in (2) if one would substitute the value for gm/Id for weak inversion.

The current $I_{TAIL} = 2I_{CM}(t)$ charges the tail capacitor C_{TAIL} in time 't' to a voltage,

$$V_{CAP}(t) = \frac{\int_0^t 2I_{CM}(\tau)\, d\tau}{C_{TAIL}}$$

At the end of integration time, t = T_{INT} and $V_{CAP}(t) = V_s(t)$. Using (3) and re-arranging yields

$$V_s(T_{INT}) = \frac{2 \cdot \Delta V_{Di,CM}(T_{INT}) \cdot C_P}{C_{TAIL}} \quad (5)$$

Substituting for $\Delta V_{Di,CM}$ from (4) in (5) and re-arranging gives the voltage gain, A_V in terms of the ratio, $\frac{C_{TAIL}}{C_P}$

$$A_V(T_{INT}) = \frac{C_{TAIL}}{2n \cdot C_P} \frac{V_s(T_{INT})}{kT/q} \quad (6)$$

Re-arranging (5), the common mode voltage drop at the Di nodes can also be related to the voltage at the tail capacitor V_s through the capacitor ratio, $\frac{C_{TAIL}}{C_P}$:

$$\Delta V_{Di,CM}(T_{INT}) = \frac{C_{TAIL}}{2 \cdot C_P} V_s(T_{INT}) \quad (7)$$

With increase in the input common mode voltage, the gate-source overdrive voltage (V_{GS}-V_T) also increases for the differential pair. It not only leads to a fast speed of operation but also results in pushing the differential pair out of the weak inversion region of operation for at least (initial) part of the integration time. Another effect that can happen for high input common mode voltage is that the differential pair enters into triode region in the later part of the comparison time. Ultimately the voltage at the drain nodes $V_{Di,CM}$ becomes equal to the source voltage: ($V_s = V_{Di,CM} = V_{CAP}$).

Since, $V_{Di,CM} = V_{DD} - \Delta V_{Di,CM}$, the corresponding maximum drop in $\Delta V_{Di,CM}$ is then :

$$\Delta V_{Di,CM,max} = \frac{C_{TAIL}}{C_{TAIL} + 2 \cdot C_P} V_{DD} \quad (8)$$

For the implemented design the Di nodes reach this final settling point for input common mode voltages of 0.9V and above. Even in such non-ideal operating conditions, the Di nodes do not discharge completely to ground and the dynamic bias comparator is more energy-efficient than the Elzakker's comparator.

Strong Inversion Noise Analysis (Elzakker's Comparator)

For the noise analysis, only the thermal noise contribution of the differential pair is considered. Simulations showed thermal noise from the differential pair (M1/M2) to dominate over the flicker noise. The Power Spectral Density (PSD) of the thermal noise current for the diff pair (M1-M2) in strong inversion is [14]

$$S_{i,M1-M2} = 8kT\Upsilon g_m \quad (9)$$

The mean square noise voltage developed across the Di+/Di- nodes at time 'T_{INT}' from [1,12,13] is

$$E[v^2_{n,SI,out}(T_{INT})] = \frac{S_{i,M1-M2} \cdot T_{INT}}{2C_P^2} = \frac{4kT\Upsilon g_m \cdot T_{INT}}{C_P^2} \quad (10)$$

Substituting for $\frac{T_{INT}}{C_P}$ from (1) in (10) results in

$$E[v^2_{n,SI,out}(T_{INT})] = \frac{4kT\Upsilon g_m \cdot \Delta V_{Di,CM}(T_{INT})}{I_{CM} \cdot C_P} \quad (11)$$

The input referred noise for strong inversion operation is,

$$E[v^2_{n,SI,in}(T_{INT})] = E[v^2_{n,SI,out}(T_{INT})] \,/\, A_V^2(T_{INT})$$

Substituting $A_V^2(T_{INT})$ from (2) and assuming as in [1,12,13] that the common mode current is relatively constant for the pre-amplifier in Elzakker's comparator during the time T_{INT},

$$E[v^2_{n,SI,in}(T_{INT})] = \frac{4kT\Upsilon}{C_P \cdot \Delta V_{Di,CM}(T_{INT}) \cdot \left(\frac{g_m}{I_{CM}}\right)_{SI,T_{INT}}} \quad (12)$$

Weak Inversion Noise Analysis (Dynamic Bias Pre-amplifier)

The PSD of the noise current for the differential pair (M1-M2) in weak inversion for the dynamic bias pre-amplifier is given as [14,15]

$$S_{i,M1-M2}(t) = 4qI_{CM}(t) \quad (13)$$

where $I_{CM}(t)$ is the tail current at any given instant of time.

The mean square noise voltage generated across the Di+/Di- nodes for the dynamic bias comparator with continuously decreasing tail current I_{CM} , is derived in the Appendix to be :

$$E[v^2_{n,WI,out}(t)] = \frac{2q \cdot \Delta V_{Di,CM}(t)}{C_P} \quad (14)$$

The input referred noise for weak inversion operation, using (4) at t = T_{INT}

$$E[v^2_{n,WI,in}(T_{INT})] = \frac{2nkT}{C_P \cdot \Delta V_{Di,CM}(T_{INT}) \cdot \left(\frac{g_m}{I_{CM}}\right)_{WI,T_{INT}}} \quad (15)$$

As highlighted in [12,13] the mean square noise voltage in (12) and (15) represents the ensemble average for the non-stationary noise sampled at the end of integration time, T_{INT}. Note that (15) shows that even though the tail current I_{CM} is not constant for the dynamic bias pre-amplifier, the end expression for noise is of similar form as in (12). This is because the charge lost from the drain nodes for a given common mode voltage drop is independent from the shape of the tail current I_{CM}.

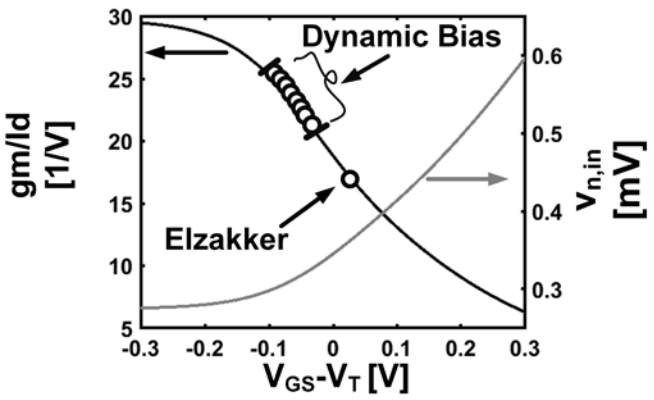

Fig.5. gm/Id and input referred noise voltage (calculated) vs V_{GS} -V_T

Typically in 65nm bulk CMOS processes, n ≈ 1.3 (giving gm/Id ≤ 30 as shown in Fig. 5). For this value of n and $\Upsilon = 2/3$, the numerator terms $4kT\Upsilon$ and $2nkT$ in Eq. (12) and (15) respectively, are approximately equal. It then follows from (12) and (15) that in any region of operation $\overline{v_{n,in}^2}$ scales inversely proportional to gm/Id. A large gm/Id (or small V_{GS}) is therefore desirable for improving the noise performance [12]. Fig. 5 shows the dependence of the input referred noise voltage from Eq. (12) and (15) on V_{GS}-V_T. With decreasing V_{GS}-V_T, the gm/Id increases which reduces the input referred noise voltage. For the differential pair biased in the vicinity of weak inversion region at $t = 0^+$, the continuously increasing V_S in the case of dynamic bias comparator ensures that it achieves a gm/Id higher than that in the Elzakker comparator throughout its integration time.

V. Design and Simulation

In this section the design of the dynamic bias comparator and Elzakker's comparator are discussed and compared. Elzakker's comparator was re-used from a previous design [1]. For the pre-amplifiers in both types of comparators, the differential pair size is kept the same in order to have identical input referred offset. Also the latch stage is identical in the Elzakker's and dynamic bias comparator in order to compare the performance of the two pre-amplifiers in terms of speed.

For the dynamic bias comparator as mentioned in Section III, the V_{GS} constantly decreases from the time CLK goes to V_{DD}. The V_{GS} -V_T for V_{CM} = 0.6V for the dynamic bias pre-amplifier ranges from approximately -25mV to -100mV during the integration time. Fig. 5 shows that the gm/Id varies from $20V^{-1}$ to around $25V^{-1}$ for the dynamic bias comparator.

For the Elzakker's comparator which was re-used without modifications, it turned out that in its new use-case, this led to a higher overdrive voltage than necessary. The V_{GS} -V_T for the Elzakker's comparator at V_{CM} = 0.6V is relatively constant around 30mV throughout the integration time. The gm/Id for the Elzakker's comparator is therefore constant around $16V^{-1}$ which is about 1.4 to 1.5 times smaller than that for the dynamic bias comparator. Equations (12) and (15) indicate that the C_P of the dynamic bias comparator could be reduced by 40-50% to get the same input referred noise as Elzakker's comparator, which is confirmed by the simulations. Therefore, C_P in the design of dynamic bias comparator is reduced by approximately 40% in comparison to that used in the Elzakker's comparator. Fig. 6(a) shows the output common mode voltage drop for both the comparators for 1mV differential input. For the proposed dynamic bias comparator the output common mode voltage drops to approximately 650mV at the end of comparison.

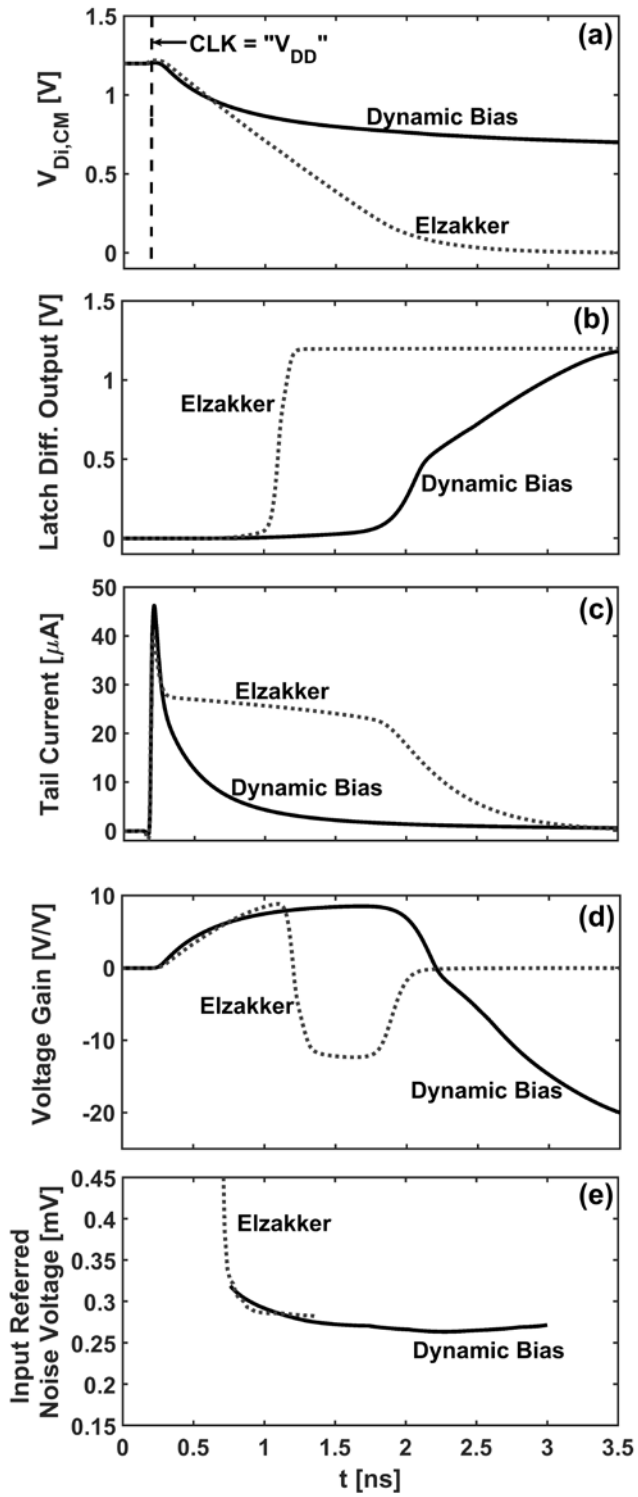

Fig.6. Simulated (a) Output common mode voltage (b) Differential latch output (c) Tail current profile (d) Pre-amplifier differential voltage (gain) of the two comparators and (e) Input referred noise voltage obtained by enabling the noise of only the pre-amplifier stage for the two comparators : Dynamic bias and Elzakker for 1mV differential input at V_{CM} = 0.6V and V_{DD} = 1.2V

Fig. 6(b) shows the differential latch output for both the comparators. Since the output common mode voltage of the pre-amplifier does not discharge to ground, the PMOS transistors M6 and M7 in the latch stage operate at a low overdrive voltage. The latch therefore has a lower regeneration speed than that in the Elzakker's comparator. The tail current profile for both the pre- amplifiers is shown as in Fig. 6(c). Fig. 6(d) shows the voltage gain at the output of the pre-amplifier. The initial tail current in the pre-amplifier is larger in the dynamic bias comparator than in Elzakker's comparator. The initial voltage gain of the pre-amplifier for the dynamic bias comparator is slightly higher than Elzakker's comparator. Additionally, the continuously decreasing V_{GS} (and tail current) in the dynamic bias comparator make sure that it operates deep in weak inversion and achieves maximum gm/Id for the most of the comparison time.

For a V_T of 400mV and C_{TAIL}/C_P = 3.5 (approx. from extraction), the voltage gain, A_V from (4) for $\Delta V_{Di,CM} = 0.5V$ at T_{INT} is approximately 15 for the dynamic bias pre-amplifier. The simulated voltage gain in Fig. 5(d) is approximately 35% lower than its calculated value due to the finite (intrinsic) voltage gain of M1/M2. The ratio $C_{TAIL}/C_P = 3.5$ is chosen so as to achieve an output common mode voltage drop of approx. 0.5V for a source voltage, V_S of around 300mV (Eq. (7)). For this chosen C_{TAIL}/C_P the maximum output common mode voltage drop, for large input common mode voltages, is about $0.6 \cdot V_{DD}$ from Eq. (8).

Fig. 6(e) shows the input referred noise contribution from the pre-amplifier of the two comparators. A pnoise simulation was performed to obtain the noise integrated at the latch output, with noise from all transistors except those in the pre-amplifier disabled. To refer the noise back to the input, the time-strobed noise at the latch output is divided by the corresponding time-strobed small signal gain of the comparator. It is to be noted that the input referred noise only starts to give meaningful results once the comparator develops gain (roughly when the common mode voltage at the Di nodes drop below a threshold voltage from the supply). The simulated input referred noise voltage for the Elzakker and dynamic bias comparators is around 0.29mV and 0.26mV respectively for V_{CM} = 0.6V. This corresponds with the input referred noise of 0.32mV for the pre-amplifier in the dynamic bias comparator as predicted by the analytical model in Eq.(15). The noise from the latch stage was also simulated, with an input-referred contribution of 0.11mV (Elzakker) and 0.09mV (Dynamic Bias). The simulated (post layout extraction) energy consumption for the dynamic bias comparator is 30fJ/comparison for V_{CM} = 0.6V.

C_{TAIL} was designed with a MoM capacitor and C_P also includes approx. 40% of MoM capacitor (in addition to the transistor parasitic) to minimize the effect of process variation. However, due to the process variation in V_T, corner simulations indicate that the input referred noise contribution from the pre-amplifier of the dynamic bias comparator changes from approx. 0.22mV for SS corner to 0.36mV for the FF corner at V_{CM} = 0.6V. The energy consumption per comparison changes from approx. 26fJ/comparison for the SS corner to 40fJ/comparison for the FF corner at V_{CM} = 0.6V.

Note that, if the pre-amplifier is not loaded with the latch, then in the case of dynamic bias, the differential voltage $A_v \cdot \Delta V_{IN}$ would remain on the Di nodes until the reset phase, while in the conventional pre-amplifier, the input transistors enter triode and will short the Di nodes. In the actual comparator, the kickback from the latch changes this behavior and with small inputs, the kickback can actually reverse the Di nodes. However, the kickback has no effect on the latch's final outcome, nor on the input referred noise, as it occurs once the decision has been made and the latch output has crossed the threshold voltage. The tail current for the dynamic bias comparator exponentially decreases with time. On the other hand, the tail current is relatively constant for the pre-amplifier in the case of Elzakker's comparator. Since the average tail current in the pre-amplifier for Elzakker's comparator is higher than the tail current in the dynamic bias comparator, the former has a higher speed of operation (or lower propagation delay). In order to make the propagation delay of the Elzakker comparator equal to that of the Dynamic bias comparator for a given noise performance, both the designs need to have same gm/Id (or same V_{GS}-V_T). For a given differential pair and load capacitance, this can be done by increasing the resistance of the tail switch transistor M3 in Elzakker comparator so that the differential pair operate at similar overdrive voltage, V_{GS}-V_T as in the case of the dynamic bias comparator . This can be done for example, by increasing the length of the transistor M3. Simulations show that in order to achieve this, the length of the tail transistor M3 for the Elzakker comparator should be approximately $9 \cdot L_{MIN}$, wherein the tail switch transistor for the Dynamic bias comparator is L_{MIN}. Further, simulations indicate that the two comparators then have comparable noise performance for the same output capacitance, C_P. The drain nodes of the pre-amplifier for the Elzakker comparator, however will discharge to ground at the end of comparison phase. Therefore, even if the propagation delay is made similar for both the comparators, the energy advantage for the dynamic comparator holds, because its output nodes do not discharge to ground.

VI. MEASUREMENT RESULTS

In order to measure the input referred noise for both the comparators a static differential input voltage, ΔV_{IN} is applied and many comparisons are performed. From that data the ratio of the number of outcomes resulting in "OUTPUT = V_{DD}" to those in "OUTPUT = 0" is computed. This process is repeated for small increments in ΔV_{IN} to generate the cumulative distribution function for the probability of getting "OUTPUT = V_{DD}" as a function of ΔV_{IN}. Fitting the measurements to a Gaussian cumulative distribution function (CDF) as shown in Fig. 7 indicates an RMS input referred noise voltage of 0.4mV for the dynamic bias comparator and 0.45mV for the Elzakker's comparator.

For the dynamic bias comparator for an input common voltage of 0.6V, Eq. (15) estimates an input referred noise contribution of 0.32mV from the pre-amplifier. This is approximately 20% lower than the measurement result of 0.4mV as Eq. (15) does not include the noise contribution from the latch stage. Simulations indicate that the noise contribution from the latch stage for dynamic bias comparator is around 0.09mV.

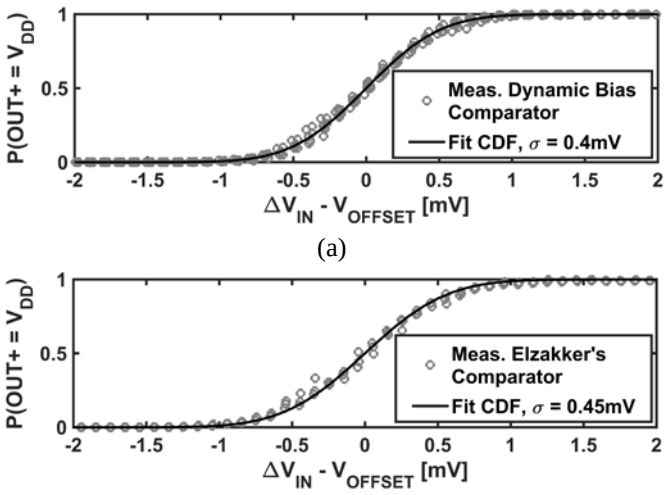

Fig. 7. Measured cumulative probability density distribution and fit to Gaussian distribution for (a) the Dynamic Bias Comparator and (b) the Elzakker's comparator; V_{CM} = 0.6V.

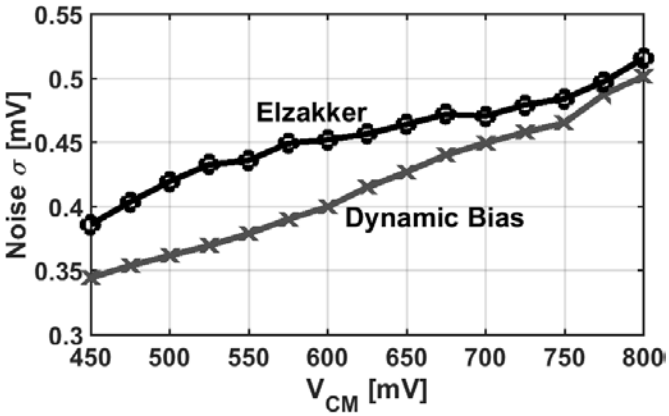

Fig. 8. Input referred noise measured as a function of V_{CM} for the Elzakker's comparator and the Dynamic Bias Comparator.

Assuming that the two noise powers are uncorrelated, the total input referred noise voltage from the analytical model is around 0.34mV. The estimated noise from the equation is 15% less than the measured input referred noise voltage of 0.4 mV for V_{CM} = 0.6V. Simulations indicate that 1/f noise contributes around 10% of the comparator noise. The difference in the estimated noise from the analytical model and the measurement results can be attributed to the exclusion of 1/f noise in the equations in Section IV.

Fig. 8 shows the input referred noise voltage for the two types of comparators as a function of V_{CM} derived from the CDF. It can be seen that the input referred noise voltage decreases with decrease in V_{CM} for both the comparators. This is because the overdrive voltage, (V_{GS}-V_T) of the transistors M1 and M2 for the input differential pair decreases with decrease in V_{CM}. This results in a higher gm/Id at lower input common mode voltage. Since the input referred noise variance is inversely proportional to the gm/Id, according to equations (12) and (15), therefore, this results in a lower input referred noise voltage for decrease in input common mode voltage. The decrease in input referred noise voltage with decreasing V_{CM} as seen from Fig. 8 follows the trend similar to that in Fig. 5 wrt decreasing $V_{GS} - V_T$ (where $V_G = V_{CM}$ and $V_S \approx 0.3$V). Fig. 9 shows the energy consumption versus input differential voltage, highlighting the reduction in overall energy consumption for various input common mode voltages. The energy consumption per comparison for the dynamic bias comparator is approximately 34fJ/comparison whereas it is 88fJ/comparison for the Elzakker comparator for 1mV differential input at V_{CM} = 0.6V. With increase in input common mode voltage, the output common voltage drop at the Di nodes ($\Delta V_{Di,CM}$) also increases until it

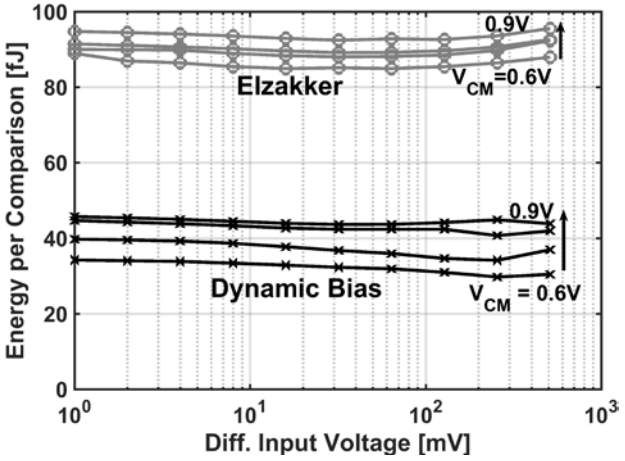

Fig. 9. Energy consumption of Dynamic Bias and Elzakker's latch-type Comparator across differential input voltage range for various V_{CM} = 0.6V to 0.9V in steps of 0.1V for 1.2V supply and 25MHz clock.

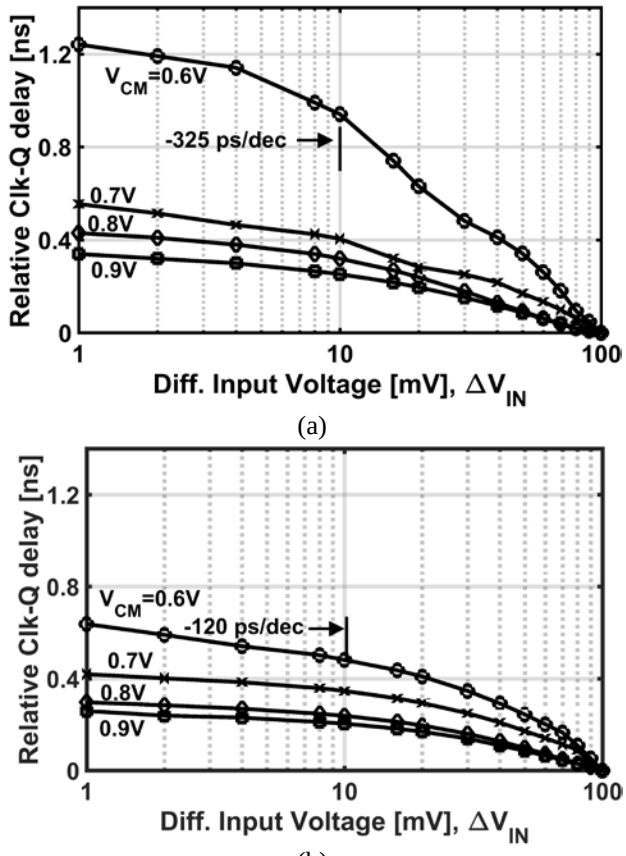

Fig. 10. Relative CLK-Q delay measured for the (a) Dynamic Bias comparator and (b) Elzakker's comparator [2] for various V_{CM} at 1.2V supply.

reaches the maximum value (as was calculated in Eq. (8)). This results in an increase in the energy consumption of the dynamic bias comparator from 34fJ/comparison for V_{CM} = 0.6V to 45fJ/comparison for V_{CM} = 0.9V.

The convergence of the output common mode voltage drop, ($\Delta V_{Di,CM}$) to its maximum value can be seen from the nearly equal energy consumption for V_{CM} = 0.8V and 0.9V. The dynamic bias comparator consumes approximately 2.6 times less energy than the Elzakker comparator at 1mV differential input for V_{CM} = 0.6V and around 2.1 times less energy for V_{CM} = 0.9V. The minima of the energy consumption for the dynamic bias comparator occurs for large differential inputs for which one of the pre-amplifier output nodes does not discharge from its pre-charge value. The dynamic bias comparator consumes approx. 2.7 times less energy than the Elzakker comparator for a differential input voltage of around 100mV for V_{CM} = 0.6V.

The absolute delay of the comparators is not measurable due to additional delay from on-chip output buffers. Alternatively, the relative CLK-Q delay for each input common mode voltage is obtained for both comparators by subtracting the respective delay measured for a large differential input voltage (ΔV_{IN} ≈ 100mV) from the delay measured for smaller differential input voltages. Fig. 10 shows the measured relative CLK-Q delay for the dynamic bias comparator and the Elzakker comparator versus ΔV_{IN} for various input common mode voltages. The logarithmic dependence of the relative CLK-Q delay on ΔV_{IN} is due to the positive feedback of the latch stage. The slope of the CLK-Q delay versus log(ΔV_{IN}) for V_{CM} = 0.6V for the two comparators is: -325ps/decade for the dynamic bias comparator and -120ps/decade for the Elzakker comparator. The dynamic bias comparator has lower regeneration speed than the Elzakker's comparator at the same V_{CM} level. This is due to the quenching of the output of the pre-amplifier near the threshold voltage of the PMOS transistors (M6/M7). Due to this quenching, the latch operates in weak inversion for a longer time for the same differential input voltage. For applications where meta-stability can be of concern (as analyzed e.g. in[19]), the maximum clock frequency for the dynamic bias comparator is consequently lower than that for the Elzakker's comparator. For large differential input signals (>70mV), the CLK-Q delay for the dynamic bias comparator is almost equal to that of the Elzakker's comparator.

The dynamic bias comparator shows a higher sensitivity to the change in input common mode voltage for small differential inputs especially when changing V_{CM} from 0.7V to 0.6V. The relative CLK-Q delay for differential input of 1mV increases by about a factor 2 for the dynamic bias comparator in comparison to a factor 1.5 for the Elzakker comparator when going from V_{CM} = 0.7V to 0.6V. This is because for V_{CM} = 0.6V, the output common mode voltage drop at the Di nodes is close to the threshold voltage for the PMOS input transistors (M6/M7) in the latch stage. This results in the latch operating in weak inversion region of operation for a considerably long time and hence the speed penalty. In SAR applications, this common-mode sensitivity does not have to be a problem as for most of the energy efficient DAC switching algorithms e.g. Split Monotonic switching [16], Swap to rest scheme [17], Merge and Split Switching[18], the common mode voltage is kept constant during a SAR conversion. This also prevents any signal-dependent common mode shift at the comparator inputs. Also it can be seen from the measurements in Fig. 9 and Fig. 10 that for higher common mode voltages, where the relative CLK-Q delay for both the comparators are nearly the same for small differential inputs, the dynamic bias comparator retains its energy advantage. Fig. 11 shows a die micrograph for both the Dynamic Bias and Elzakker's comparators, with the inset showing the sizes. The area overhead for the tail capacitor in the dynamic bias comparator is approximately 20% over that of the Elzakker's comparator.

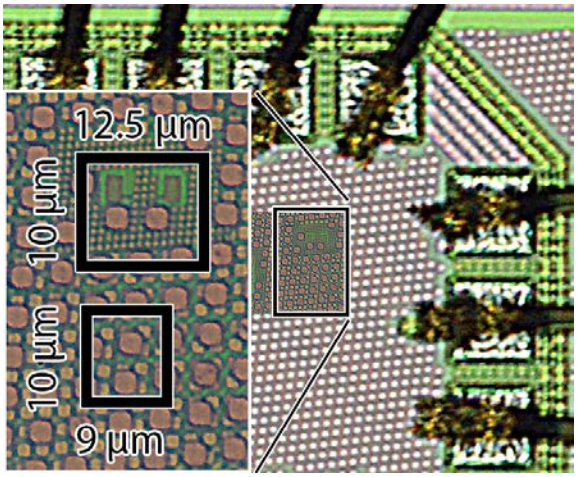

Fig. 11 . Die micrograph : The inset shows the zoomed in region for both the dynamic bias comparator and Elzakker's comparator. The sizes are 12.5µmx10µm for dynamic bias comparator and 10µmx9µm for the Elzakker's comparator.

VII. CONCLUSION

In conclusion the dynamic bias comparator presented here offers a simple, low overhead solution to reduce the energy consumption of the pre-amplifier. The energy saving occurs because of the partial discharge of the pre-amplifier output nodes which are loaded with relatively large capacitors to reduce the noise. The pre-amplifier (dynamic) bias consists of a tail capacitor in combination with a small switch transistor. The mathematical analysis shows that the noise performance of the pre-amplifier is independent of the integration time and can be maximized by increasing gm/Id for a given capacitive load. The dynamic bias keeps the pre-amplifier in the weak inversion regime for most of the integration time in order to obtain minimum achievable noise performance for a given capacitive load. The performance of the dynamic bias comparator can be optimized for a given common-mode voltage by tuning the ratio of the tail capacitor to the load capacitor. The dynamic bias comparator has a higher CLK-Q delay which is due to the longer operation time in the weak inversion regime. The energy per comparison is however independent of the speed of operation. Therefore, for applications where speed of operation is not the bottleneck, such as wireless sensor nodes or IoT devices, the dynamic bias comparator is an interesting choice for reducing energy consumption. For a nominal common-mode voltage, V_{CM} equal to 0.6V (V_{DD}/2), the implemented dynamic bias comparator is about 2.5 times more energy

efficient than its predecessor, which makes it an ideal building block for such low energy applications.

VIII. Acknowledgements

The authors would like to acknowledge Simon M. Louwsma and Paul Geraedts from Teledyne DALSA, Enschede for their valuable inputs and technical discussions.

IX. References

[1] M. van Elzakker et.al, "A 10-bit Charge-Redistribution ADC Consuming 1.9µW at 1MS/s", in *IEEE Journal of Solid-State Circuits*, vol. 45, no. 5, pp. 1007-1015, May 2010.

[2] P. Harpe, E. Cantatore, Arthur van Roermund, "A 2.2/2.7fJ/conversion-step 10/12b 40kS/s SAR ADC with Data-Driven Noise Reduction", *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, 2013, pp. 270-271..

[3] M. Liu et. al "A106nW 10 b 80 kS/s SAR ADC With Duty-Cycled Reference Generation in 65 nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 51, no. 10, pp. 2435-2445, Oct. 2016.

[4] D. Schinkel et. al, "A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time", *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, San Francisco, CA, 2007, pp. 314-605.

[5] T. Kobayashi, K. Nogami, T. Shirotori, and Y. Fujimoto, "A current-mode latch sense amplifier and a static power saving input buffer for low-power architecture", *VLSI Symposium*, June 1992, pp. 28–29.

[6] B. Razavi, "The StrongARM Latch [A Circuit for All Seasons]", in *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12-17, Spring 2015.

[7] H. S. Bindra, C. E. Lokin, A. J. Annema and B. Nauta, "A 30fJ/comparison dynamic bias comparator", *ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*, Leuven, 2017, pp. 71-74.

[8] B. J. Hosticka, "Dynamic CMOS amplifiers", in *IEEE Journal of Solid-State Circuits* 1980 vol. 15, no. 5, pp. 881-886.

[9] J.W. Jung, B. Razavi, "A 25-Gb/s 5-mW CDR/deserializer", in *IEEE Journal of Solid-State Circuits* 2013, pp. 684–69.

[10] S. Saxena *et al*., "A 2.8 mW/Gb/s, 14 Gb/s Serial Link Transceiver", in *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1399-1411, May 2017

[11] M. S. Akter, K. Makinwa and K. Bult, "A capacitively-degenerated 100dB linear 20–150MS/s dynamic amplifier", *2017 Symposium on VLSI Circuits*, Kyoto, 2017.

[12] P. Nuzzo, F. De Bernardinis, P. Terreni and G. Van der Plas, "Noise Analysis of Regenerative Comparators for Reconfigurable ADC Architectures", in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 6, pp. 1441-1454, July 2008

[13] T. Sepke, P. Holloway, C. G. Sodini and H. S. Lee, "Noise Analysis for Comparator-Based Circuits", in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 3, pp. 541-553, March 2009.

[14] Y. Tsvidis, "*Operation and Modeling of the MOS Transistor*", 2nd ed., Oxford University Press, 1999, pp 412-423

[15] A. Papoulis and S. U. Pillai, "*Probability, Random variables and Stochastic Processes*", Boston: McGraw-Hill, 2002, pp 435-494.

[16] B. P. Ginsburg and A. P. Chandrakasan, "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC," *2005 IEEE International Symposium on Circuits and Systems*, 2005, pp. 184-187 Vol. 1.

[17] J. Y. Lin and C. C. Hsieh, "A 0.3 V 10-bit 1.17 f SAR ADC With Merge and Split Switching in 90 nm CMOS", in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 1, pp. 70-79, Jan. 2015.

[18] M. Liu, A. H. M. van Roermund and P. Harpe, "A 7.1-fJ/Conversion-Step 88-dB SFDR SAR ADC With Energy-Free "Swap To Reset", in *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 2979-2990, Nov. 2017.

[19] G. R. Couranz and D. F. Wann, "Theoretical and Experimental Behavior of Synchronizers Operating in the Metastable Region," in *IEEE Transactions on Computers*, vol. C-24, no. 6, pp. 604-616, June 1975.

X. APPENDIX

In this appendix we derive the expression for the mean square output referred noise voltage for the pre-amplifier in the dynamic bias comparator for which the tail current, I_{TAIL} is not constant. It can be approximated as an exponentially decaying function and written as,

$$I_{TAIL}(t) = I_{TAIL}(0^+)e^{-t/\tau 1} \quad (16)$$

where $I_{TAIL}(0^+)$ is the tail current at the instant (t = 0^+) when the switch is closed (CLK = V_{DD}) and τ1 is the time constant for the tail switch-capacitor network (M3a, C_{TAIL}) in Fig. 3(a).

Substituting $I_{CM}(t) \approx I_{TAIL}(t)/2$ for small input differential voltages in Eq. 3 the output common mode voltage drop can be written as

$$\Delta V_{Di,CM}(t) = \frac{I_{TAIL}(0^+) \cdot \tau 1 \cdot [1 - e^{-t/\tau 1}]}{2C_P} \quad (17)$$

As was also analyzed in [12,13], the variance at the output of a filter that is fed with non-stationary white noise can be described with a convolution equation of the magnitude squared impulse response ($|h_n(\tau)|^2$) and the power spectral density $S_i(t)$ of the noise source:

$$\sigma_o^2(t) = \frac{1}{2}\int_0^t S_i(t-\tau) \cdot |h_n(\tau)|^2 d\tau \quad (18)$$

where for the case of the pre-amplifier in the dynamic bias comparator, $S_i(t) = 4qI_{CM}(t)$ is the white noise current PSD for the input differential pair [14] in weak inversion and $h_n(t) = 1/C_P\, e^{-t/\tau 0}$ is the impulse response from the noise current source to the output voltage of the differential pair [12,13].

$\tau 0$ is the time constant for the transconductance amplifier as defined in [12,13].

Substituting for $S_i(t)$ and $h_n(t)$ in Eq.(18) results in the mean square output noise voltage for the pre-amplifier in dynamic bias comparator

$$E[v_{n,WI,out}^2(t)] = \frac{2qI_{TAIL}(0^+)e^{\frac{-t}{\tau 1}}}{2C_P^2}\int_0^t e^{\tau\left(\frac{1}{\tau 1}-\frac{2}{\tau 0}\right)}\, d\tau$$

$$E[v_{n,WI,out}^2(t)] = \left(\frac{2qI_{TAIL}(0^+)e^{\frac{-t}{\tau 1}}}{\left[\frac{1}{\tau 1}-\frac{2}{\tau 0}\right]2C_P^2}\right)\left(e^{\left(\frac{t}{\tau 1}-\frac{2t}{\tau 0}\right)}-1\right)$$

As mentioned in [12,13] for comparator based circuits $\frac{\tau 0}{2} \gg T_{INT}$, since the (integration) time interval in which the circuit is observed is quite small in comparison to the circuit time constant, so the noise approximates to:

$$E[v_{n,WI,out}^2(t)] = \left(\frac{2qI_{TAIL}(0^+)\tau 1}{2C_P^2}\right)(1 - e^{\frac{-t}{\tau 1}})$$

Substituting for $\Delta V_{Di,CM}$ from Eq. (17)

$$E[v_{n,WI,out}^2(t)] = \frac{2q \cdot \Delta V_{Di,CM}(t)}{C_P} \quad (19)$$

This is the same result as would be obtained when the common mode current is assumed to be constant during the integration time.

Harijot Singh Bindra (S'16) received his B.Tech degree in electronics and communication engineering from Punjabi University, Patiala, India in 2008 and M.Tech degree in VLSI design from Indian Institute of Technology, Delhi, India in 2012. He is currently pursuing his Ph.D. degree with the Integrated Circuit Design group at the University of Twente, Enschede, The Netherlands. His current research interests include ADCs, low-voltage low-energy circuit design, equalizers, clocking and data recovery circuits.
He worked as a Scientist with the Indian Space Research Organization from 2008-2010 at the semi-conductor design and fabrication facility in Chandigarh, India. He also worked as Senior Design Engineer at the Cadence Design Systems, Noida, India from 2012-2014 where he worked upon high speed serial links, clock and data recovery circuits and equalizers.
He was awarded with the University Gold Medal for ranking first in the University in B.Tech degree. He received the graduate scholarship for the entire duration of his Master's degree from Cadence Design Systems Inc. He also serves as a Reviewer for the IEEE Journal of Solid-State Circuits (JSSC).

Christiaan E. Lokin (S'16) received the B.Sc. and M.Sc. (cum laude) in electrical engineering from the University of Twente, Enschede, the Netherlands in 2013 and 2015, respectively where he is currently pursuing his Ph.D. degree at the Integrated Circuit Design group. His current research interests include mixed-signal systems and control systems for applications in class-D power amplifiers.

Daniel Schinkel (S'03-M'08) received the M.Sc. degree (cum laude) in Electrical Engineering in 2003 and the Ph.D. degree in 2011, both from the University of Twente, Enschede, The Netherlands.
His Ph.D. research was carried out between 2003 and 2007 at the IC-design group, headed by Bram Nauta. He is one of the founders of Axiom IC, an IC-design company that started in Enschede in 2007 and which focused on the design of data-converters and mixed-signal systems. Axiom IC was acquired in 2013 by Teledyne DALSA. Since 2013, he is active as an independent research consultant, working for various IC companies as well as for the University.
His current research interests include analog, digital, and mixed-signal circuit design, sigma-delta data converters, class-D power amplifiers and high-speed communication circuits. He holds four patents and has authored or co-authored about 25 papers.

Anne-Johan Annema received the M.Sc. degree in electrical engineering and the Ph.D. degree from the University of Twente, Enschede, The Netherlands, in 1990 and 1994, respectively. In 1995, he joined Philips Research in Eindhoven, The Netherlands, where he worked on a number of physics- electronics-related projects, low-power low-voltage circuits, fundamental limits on analog circuits related to with process technologies, high-voltage in baseline CMOS to feasibility research of future CMOS processes for analog circuits. In 2000 he returned to the University of Twente, where he is associate professor with the IC-Design group in the department of Electrical Engineering. His current research interest is in physics, analog and mixed-signal electronics, RF power amplifiers, deep-submicrometer technologies and their joint feasibility aspects. He is also part-time consultant in industry, co-founded ChipDesignWorks and is the recipient of three educational awards at the University of Twente.

Bram Nauta was born in 1964 in Hengelo, The Netherlands. In 1987 he received the M.Sc degree (cum laude) in electrical engineering from the University of Twente, Enschede, The Netherlands. In 1991 he received the Ph.D. degree from the same university on the subject of analog CMOS filters for very high frequencies. In 1991 he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven the Netherlands. In 1998 he returned to the University of Twente, where he is currently a distinguished professor, heading the IC Design group. Since 2016 he also serves as chair of the EE department at this university. His current research interest is high-speed analog CMOS circuits, software defined radio, cognitive radio and beamforming.
He served as the Editor-in-Chief (2007-2010) of the IEEE Journal of Solid-State Circuits (JSSC), and was the 2013 program chair of the International Solid State Circuits Conference (ISSCC). He is currently the President of the IEEE Solid-State Circuits Society (2018-2019 term).
Also, he served as Associate Editor of IEEE Transactions on Circuits and Systems II (1997-1999), and of JSSC (2001-2006). He was in the Technical Program Committee of the Symposium on VLSI circuits (2009-2013) and is in the steering committee and programme committee of the European Solid State Circuit Conference (ESSCIRC). He served as distinguished lecturer of the IEEE, is co-recipient of the ISSCC 2002 and 2009 "Van Vessem Outstanding Paper Award" and in 2014 he received the 'Simon Stevin Meester' award (500.000€), the largest Dutch national prize for achievements in technical sciences. He is fellow of the IEEE and member of the Royal Netherlands Academy of Arts and Sciences (KNAW).