Design Considerations for Integrated High-Frequency p-Channel JFET's

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Abstract—**To achieve high-frequency performance of integrated p-channel JFET's, the large substrate capacitance is decoupled by separating the top gate from the bottom gate. Further optimization of the JFET design, with respect to frequency response, is studied here both theoretically and experimentally using devices produced in a double-implantation BIFET process for analog integrated circuits. Results show that attentuation of the hole mobility due to high doping level effects make it favorable to design with wide lightly doped channels. To avoid undesirable currents from the source to the drain or from the top to the bottom gate, the channel must be uniform. This and the requirements for high-frequency performance put additional demands on the technology. Use of the separated-gate JFET in circuit designs is complicated by the presence of a large bulk effect and the top-gate to bottom-gate reachthrough diode.**

I. INTRODUCTION

UNLIKE vertical p-n-p's, p-channel JFET's can be integrated in a bipolar process in a straightfoward manner. The basic structure resembles that of the vertical n-p-n, since the emitter regions may be used as gates, the base contacting regions as source and drain contacts, and the intrinsic base as the channel. The base, however, is usually too heavily doped to give suitable JFET properties and some extra processing steps become necessary [1]–[3]. Poor reproducibility of the channel is often the result when a region must be made that is thinner and more lightly doped than the original base region. Nevertheless, in modern implantation processes such as the present BIFET process, good reproducibility is ensured and flexible processing schemes often make the inclusion of an extra implantation to form the channel a very simple procedure.

The JFET is a normally-on device and therefore cannot be used with the same versatility as bipolar transistors and MOSFET's. Nevertheless, field-effect transistors as such have some unique properties, and including some sort of FET in a bipolar process gives the analog circuit designer a number of attractive application possibilities. Most important is that significantly improved noise behavior can be realized for certain source impedances. FET's can also be applied as "floating" analog voltage switches, and with the low gate bias of the the FET, it is possible to realize low current offsets. Moreover, in bipolar processes with poor-quality p-n-p's, a high-frequency "p"-type field-effect element can in some situations be a very attractive substitute for the p-n-p. In CMOS processes the integration of JFET's is also interesting because the designer then has access to a transistor with low $1/f$ noise [4]. The use of the JFET usually limits itself to some key positions in the circuit design, but can give considerable simplification of the layout and notable improvement in circuit performance.

The JFET properties that ensure high-frequency performance also promote low-noise behavior. For integrated p-channel JFET's, the former is in the first instance achieved by separating the top gate from the bottom gate and using top-gate-driven configurations, whereby the normally large substrate capacitance is decoupled [2], [3]. Although the idea of separating the gates was launched several years ago, no thorough study of the characteristics of such devices has been given. Compared to the joined-gate case, this separation in fact introduces a number of complications, both on the level of the silicon technology and in the actual circuit design. These problems are treated here, and based on experimental and theoretical evaluations a number of general conclusions are established for the optimal design and application of separated-gate JFET's for high-frequency performance.

II. JFET FREQUENCY RESPONSE

In the saturation region, which is the mode of operation almost always used in analog circuits, the JFET can be represented by the small-signal model shown in Fig. 1. The distributed capacitances and resistances are approximated by the lumped elements illustrated schematically in Fig. 2 for a typical p-channel JFET design. The division of the top- and bottom-gate functions is made at the pinchoff point, which is the point where the depletion layers in the channel meet at the drain end of the channel.

The most popular figure of merit for the JFET frequency response is the cutoff frequency f_T, defined as the frequency for which the short-circuit current gain is unity. High f_T is also an indication of low-noise performance, since the noise of a FET appears primarily at the output as a thermal noise current of the channel. The equivalent noise source at the input is then related to the f_T via the ratio of the transconductance g_m to the gate capacitance C_G. A very simple formula for f_T can be established if the following parasitic resistances are neglected [5]:

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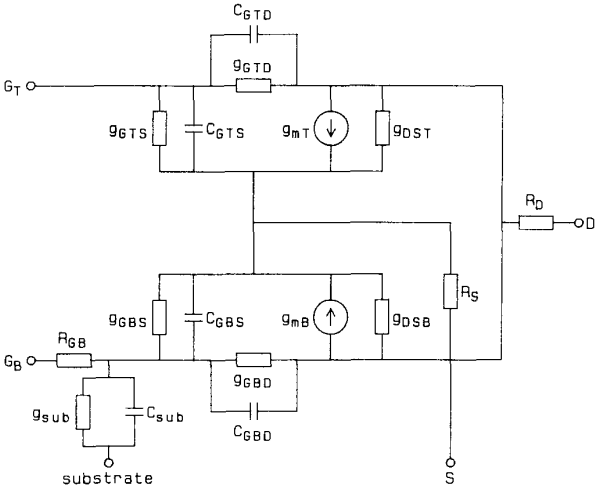

Fig. 1. Linearized small-signal model of a JFET, with emphasis on the role of the top and bottom gates.

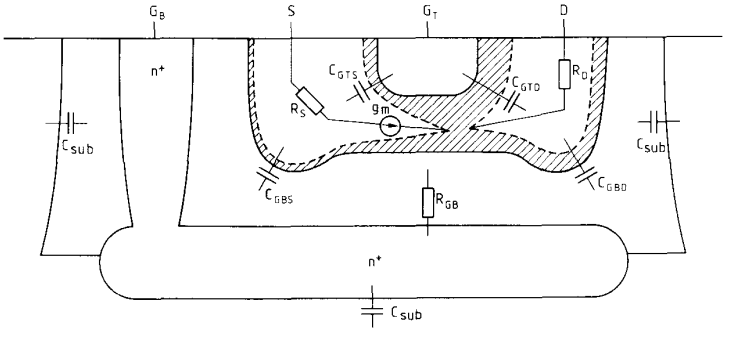

Fig. 2. Distribution of small-signal circuit elements in a JFET.

1) the source series resistance R_S, which is assumed small as compared to the channel resistance (represented by g_m);
2) the conductances of the reverse-biased gates;
3) the top-gate series resistance, which would determine noise and high-frequency performance if the JFET were not designed to make this resistance insignificant; and
4) the bottom-gate series resistance R_{GB}, which is large and, along with the substrate capacitance C_{sub}, limits the frequency response of the bottom gate. Omitting R_{GB} is not of consequence for the general conclusions.

Thus for the joined-gate device

$$f_T = \frac{1}{2\pi} \frac{g_{mT} + g_{mB}}{C_{sub} + C_{GTS} + C_{GTD} + C_{GBS} + C_{GBD}} \quad (1)$$

where

g_{mT} is the transconductance of the top-gate-driven device;
g_{mB} is the transconductance of the bottom-gate-driven device;
C_{GTS} is the top-gate to source capacitance;
C_{GTD} is the top-gate to drain capacitance;
C_{GBS} is the bottom-gate to source capacitance; and
C_{GBD} is the bottom-gate to drain capacitance.

In the top-gate-driven case all capacitances associated with the bottom gate and R_{GB} are eliminated giving

$$f_T = \frac{1}{2\pi} \frac{g_{mT}}{C_{GTS} + C_{GTD}}. \quad (2)$$

The effective transconductance is also reduced by g_{mB}, but with a lightly doped epi-layer this is a relatively small loss, and all in all a much higher f_T can be obtained by separating the gates.

Only the top-gate capacitances are accounted for in the expression for f_T, but the actual performance of the JFET will often be determined by transmission parameters other than the current gain. The bottom-gate capacitance is often dominated by the large junctions between the channel contacting regions and the epi-layer. Under normal functioning of the separated-gate device the source–bottom-gate junction is grounded for small-signal purposes and the bottom-gate–drain junction capacitance becomes by

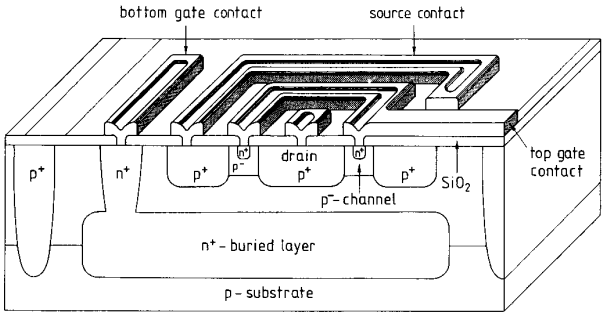

Fig. 3. Cross section of the separated-gate JFET in the BIFET process, without the second metalization layer.

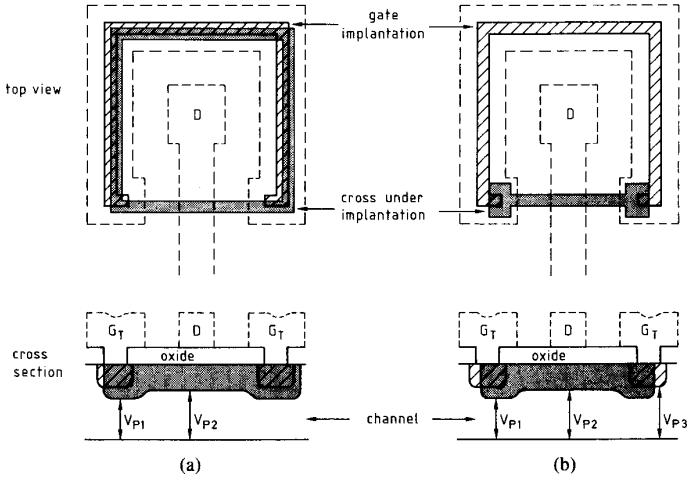

Fig. 4. Two methods of closing the top-gate ring with an extra n^+ implantation under the oxide. The resulting channel depths are indicated, and the corresponding pinchoff voltages are such that (a) $V_{P1} < V_{P2}$ and (b) $V_{P1} \neq V_{P2}$, $V_{P1} < V_{P3}$, and $V_{P2} > V_{P3}$.

far for the most detrimental to the frequency response. The parasitic capacitive coupling from the source to the drain is very small, which can be seen by regarding the junction capacitance C_J at some point J along the source–bottom-gate junction

$$C_J \equiv \frac{\partial Q_J}{\partial V_J} = \frac{\partial Q_J}{\partial I_{DS}} \frac{\partial I_{DS}}{\partial V_{DS}} \frac{\partial V_{DS}}{\partial V_J} \tag{3}$$

where

V_J is the voltage over the junction at position J;
V_{DS} is the drain-to-source voltage; and
I_{DS} is the drain-to-source current.

The second factor on the right side is the output conductance, which in the saturation region is small, and the last factor will be very small because the voltage drop from the source to the drain is practically localized to the high-resistance channel region, which in area is insignificant compared to the channel contacting region.

If R_s is comparable to the intrinsic channel resistance, the effective transconductance, and consequently f_T, will be reduced. This and the above considerations of the bottom-gate capacitances make designs that minimize the drain area preferable.

III. BIFET Process Description

The experimental results quoted here have been measured on p-channel JFET's produced in a high-performance BIFET process, which contains 3-GHz n-p-n's and 450-MHz p-channel JFET's. The process is relatively simple, with standard diffusion techniques being used to form the n^+ buried layer, the n^+ contact to the buried layer, and the p^+ isolation. The active device regions are formed by arsenic and boron implantations. The basic design of the separated-gate JFET is shown in Fig. 3. The gate (emitter) is an n^+ arsenic implantation, the source and drain contacting regions (extrinsic base) are p^+ boron implantations, and, instead of using the intrinsic base implantation, an extra boron implantation is incorporated to form the actual channel region. To obtain high-frequency performance, three basic requirements have been met by this design:

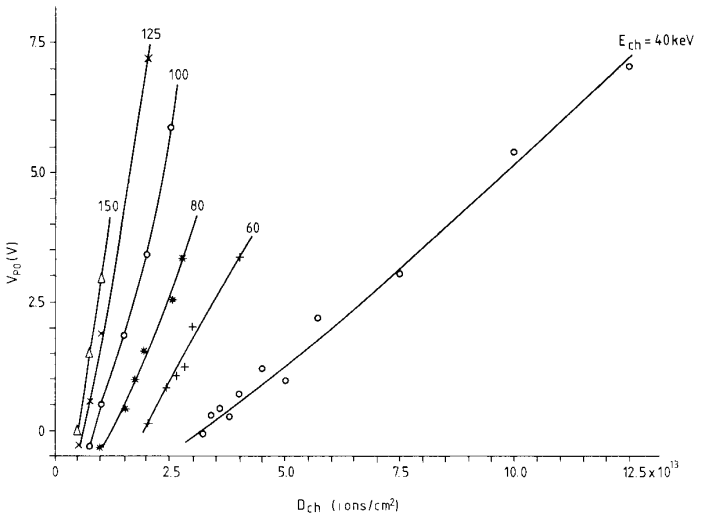

Fig. 5. Pinchoff voltage against channel implantation dose for several implantation energies.

1) the top-gate is made in the self-aligned washed-emitter step to give a narrow (2 μm) gate length L and thus high g_m;
2) the top-gate series resistance is made insignificant by direct metal contact along the whole of the gate; and
3) the influence of the large C_{sub} and R_{GB} is eliminated by using a ring-gate structure with the drain in the center and the top gate totally embedded in the channel region.

The contact to the drain cannot directly cross the washed gate, so a second layer of metal is introduced to cross over the top-gate metallization. Therefore, two extra processing steps are introduced to ensure high-frequency performance. Another possibility was using some sort of cross-under implantation, two variants of which are shown in Fig. 4. An extra n^+ gate implantation is employed before the last oxidation step, either just in the region under the metal track leading to the drain, or as a closed ring running under the whole of the washed gate [3]. In the last case, possible misalignments will increase the effective value of L, and in both cases nonuniformities in the channel depth give either parasitic source-to-drain resistance or premature pinching off in parts of the channel. The latter effect gives undesirable top-gate to bottom-gate currents (see Section VI-A). These problems are also encountered for non-ring-gate structures that attempt to isolate the extremities of the gate via, for example, oxide isolation or a reverse-biased diode. For very long gate JFET's these parasites may be negligible, but, for example, in the smallest device that can be made in the present process, the gate length is 100 μm and any cross under would necessarily be at least 24 μm long, thus a quarter of the total gate length.

The effective pinchoff voltage V_P is here defined as the absolute V_{DS} for which I_{DS} saturates at a given gate biasing V_{GTS} and V_{GBS}. For the standard joined-gate case with biasing $V_{GTS} = V_{GBS} = 0$, the pinchoff voltage is denoted V_{PO}. In the BIFET process the standard JFET is a device with $V_{PO} = 1.5$ V, produced with a channel implantation dose $D_{ch} = 7 \times 10^{12}/\text{cm}^2$ at energy $E_{ch} = 150$ keV. It is designed to be used with a gate biasing such that $V_P = 1$ V. The characteristics of this device are discussed in Section VI.

IV. Optimization of the Channel

In the BIFET process, the extra implantation step, introduced to define the channel region, will be decisive for the characteristics of the JFET's. The actual channel doping profile is determined by the dose and energy of this implantation, subject to the following oxidation and anneal steps, as well as the arsenic gate implantation profile. The relationship found experimentally between the V_{PO} and the implantation parameters is shown in Fig. 5. It is concluded that the higher energy implantations give wider, more lightly doped channels. This has been confirmed by measurements, performed by C–V techniques [6], of the channel doping profile under the highly doped top gate. The intrinsic channel region is decisive for the top-gate transconductance and capacitance, and thus the f_T, whereas it is of little consequence for the bottom-gate capacitances. The relationship between the channel implantation conditions and the top-gate parameters is therefore investigated, and although the V_{PO} results are quite specific to the present BIFET process, generally valid conclusions are established.

A. Theoretical Considerations

A theoretical evaluation of g_m and C_{GT} is given here by limiting the calculations to the intrinsic channel region. The current–voltage relationships are established by basically following the method proposed by Bockemuehl [7], [8]. The procedure is here generalized to include the doping dependence of the mobility. The following assump-

tions are made:

1) the gates may be treated separately by dividing the channel at pinchoff point a (see Fig. 6);
2) the analysis is valid for long-gate JFET's;
3) the depletion approximation is valid;
4) the gates and channel are described by an arbitrary doping distribution $N(y)$; and
5) the channel mobility μ is a function of the doping concentration but field independent; thus, $\mu = \mu(y)$.

Solution of the Poisson equation in the y direction gives the voltage $V(h)$, where $h(x)$ is the boundary of the depletion layer and $V(x)$ is the voltage across the depleted region. It is related to the applied voltage V_a as $V = V_a + \psi_{bi}$, where ψ_{bi} is the built-in voltage. The pinchoff voltage is given by [8]

$$V_p = V(a) = \frac{1}{\epsilon_s}\int_0^a yN(y)\,dy. \tag{4}$$

With $h = y_S$ at $x = 0$ and $h = y_D$ at $x = L$, the drain current I_D governed by the one gate is calculated to be

$$I_D = \frac{Z}{\epsilon_s L}\int_{y_S}^{y_D}\left\{\int_h^a \mu(y)\,N(y)\,dy\right\}hN(h)\,dh \tag{5}$$

giving the corresponding transconductance

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{Z}{L}\int_{y_S}^{y_D}\mu(y)\,N(y)\,dy \tag{6}$$

and the channel conductance

$$g_D = \frac{\partial I_D}{\partial V_D} = \frac{Z}{L}\int_{y_D}^{a}\mu(y)\,N(y)\,dy. \tag{7}$$

To calculate g_m for a given gate and channel doping profile $N(y)$, the doping dependence of ψ_{bi} must be taken into account [8]

$$\psi_{bi} = \frac{kT}{q}\ln\left\{\frac{\left|N(y_G(V))\,N(y_{ch}(V))\right|}{n_i^2}\right\}, \qquad V_a = 0 \tag{8}$$

where $y_G(V)$ and $y_{ch}(V)$ denote the depletion boundary in the gate and channel, respectively. To find the voltage dependence of the depletion boundaries the following equations, found by integrating the Poisson equation, are solved [9]:

$$\int_{y_G(V)}^{y_{ch}(V)} N(y)\,dy = 0 \tag{9}$$

$$\int_{y_G(V)}^{y_{ch}(V)} N(y)\,dy + \frac{\epsilon_s}{q}(V_a + \psi_{bi}) = 0. \tag{10}$$

The hole mobility $\mu(y)$ in the channel is approximated by applying the empirical expression given by Caughey and Thomas [10], which is plotted in Fig. 7(a). The g_m can then be found from (6) with $y_S = y_{ch}(V_{GS})$ and $y_D = y_{ch}(V_{DS})$.

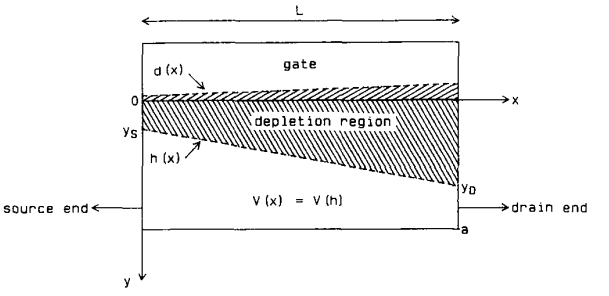

Fig. 6. Nomenclature in the channel region to the pinchoff point a.

The gate junction capacitance per unit area varies along the channel as

$$C_G(x) = \frac{\epsilon_s}{h(x) + d(x)} \tag{11}$$

where $d(x)$ is the width of the depletion into the gate. In the saturation mode of operation the maximum C_G, $C_{G\max}$, is obtained at $x = 0$. Here, $C_{G\max}$ will be used instead of $(C_{GTS} + C_{GTD})$ to evaluate f_T of a top-gate-driven device. If g_{mT} and $C_{G\max}$ are given for a 1×1 μm^2 gate, then from (2)

$$f_T = \frac{1}{2\pi}\frac{g_{mT}}{L^2 C_{G\max}} \tag{12}$$

where L is in micrometers. For the case where the top gate and channel doping levels N_T and N_{ch}, respectively, are uniform, and $N_T >> N_{ch}$, the following simple formulas can be established for a top-gate biasing V_{GTS}:

$$g_{mT} = \frac{Z}{L}\mu\sqrt{\frac{2\epsilon_S N_{ch}}{q}}\left(\sqrt{\psi_{bi} + V_{GTS} + V_P} - \sqrt{\psi_{bi} + V_{GTS}}\right) \tag{13}$$

$$C_{G\max} = ZL\sqrt{\frac{q\epsilon_s N_{ch}}{2(\psi_{bi} + V_{GTS})}} \tag{14}$$

$$f_T = \frac{1}{\pi}\frac{1}{L^2}\frac{\mu}{q}\left\{\sqrt{(\psi_{bi} + V_{GTS})^2 + V_P(\psi_{bi} + V_{GTS})} - (\psi_{bi} + V_{GTS})\right\}. \tag{15}$$

Thus, f_T is only dependent on the doping levels via the quantities μ and ψ_{bi}. Whereas ψ_{bi} increases but slightly with increasing N_{ch}, μ shows a dramatic decrease for N_{ch} of more than $\sim 10^{16}/cm^2$. This gives a correspondingly large reduction in g_m and f_T, as demonstrated in Fig. 7. Normally a JFET will be designed for the highest possible g_m, but here this would be at the expense of the frequency response. Above $N_{ch} \sim 10^{16}/cm^2$, the increase in g_m is minimal, whereas a manifold decrease in f_T is displayed.

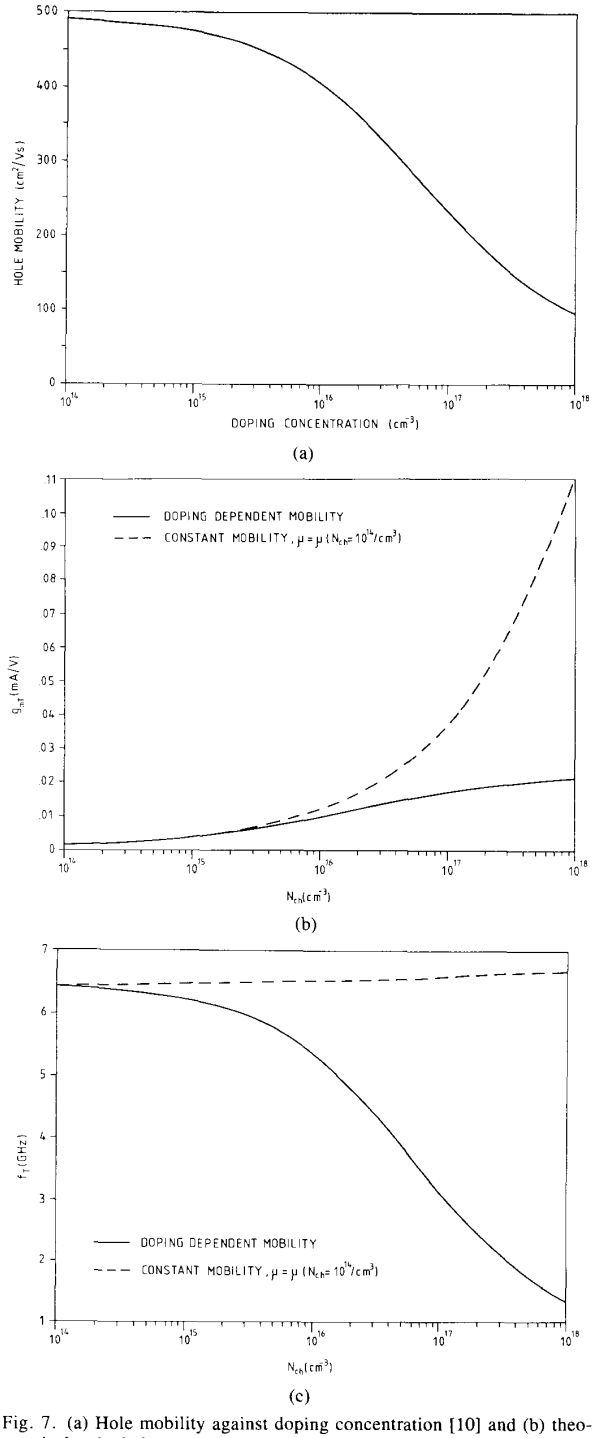

Fig. 7. (a) Hole mobility against doping concentration [10] and (b) theoretical calculations of top-gate transconductance, and (c) cutoff frequency against channel doping concentration for $N_T = 10^{20}/\text{cm}^3$.

B. Experimental Results

In the present BIFET process the dc parameters, when correlated to V_{PO}, are largely independent of the exact implantation conditions. Disregarding the subthreshold region of operation, the correlation can be well represented by the following linear relationships:

$$V_{PT0} = 1.4 \cdot V_{PO} \tag{16}$$

$$V_{PB0} = 5.8 \cdot V_{PO} \tag{17}$$

$$g_{D0} = 19.9\ \text{nA/V}^2 \cdot V_{PO} + 1.3\ \text{nA/V} \tag{18}$$

$$g_{m0} = g_{mT0} + g_{mB0} = 1.06 \cdot g_{D0} \tag{19}$$

$$g_{mT0} = 0.78 \cdot g_{D0} \tag{20}$$

$$g_{mB0} = 0.28 \cdot g_{D0} \tag{21}$$

where all values are normalized to a $1 \times 1\ \mu\text{m}^2$ top gate. The suffix "0" refers to the situation with biasing $V_{GTS} = V_{GBS} = 0$, and V_{PTO} is the top-gate voltage necessary to pinch off the channel, V_{PBO} is the bottom-gate voltage necessary to pinch off the channel, and g_{DO} is the channel conductance with $V_{DS} = 0$. On the other hand, in accordance with the fact that higher implantation energy gives lightly doped, deeper channels, the top-gate capacitance plotted against V_{PO} shows a clear dependence on the implantation conditions. This is illustrated in Fig. 8, where C_{ch0}, the capacitance per unit area of the uniform top-gate–channel junction, is plotted.

A comparison of experimental and theoretical results can in the first instance be made by assuming uniformly doped gates and channel. With such a structure the experimentally observed near-linear relationships between the JFET dc parameters and V_{PO} are not reproduced. Theoretically a spectrum of V_{PO}'s is achieved by varying the channel doping and/or channel of depth. Fig. 9 shows the relationship between transconductance and V_{PO} for a series of channel doping levels. The spread in the corresponding measured values cannot be corelated to the implantation energy. The experimental values of g_{mT0}, however, do lie within the region theoretically covered, which agrees with the fact that the highly doped top gate gives a nearly abrupt transition to the channel and is thus relatively well represented by the simple model. For g_{mB0} the experimental values lie well below those obtained theoretically. In this case the experimental results are theoretically better approximated if the doping profile in the channel is assumed to have a significant implantation tail, which gives a light effective bottom-gate doping at the junction. Thus, the depletion over the bottom-gate junction primarily extends into the then much more lightly doped epitaxial layer, instead of modulating the channel.

The theoretical results showed that although there was some increase in g_{mT0} with increasing N_{ch}, this was forfeited by a large attenuation of f_T. Within the span of the experimental results no clear advantage for g_{mT0} emerges, so in the present process the decision to optimize the channel to maximize f_T instead of g_m is in no way ambiguous. The highest possible implantation energy therefore is used for the channel implantation.

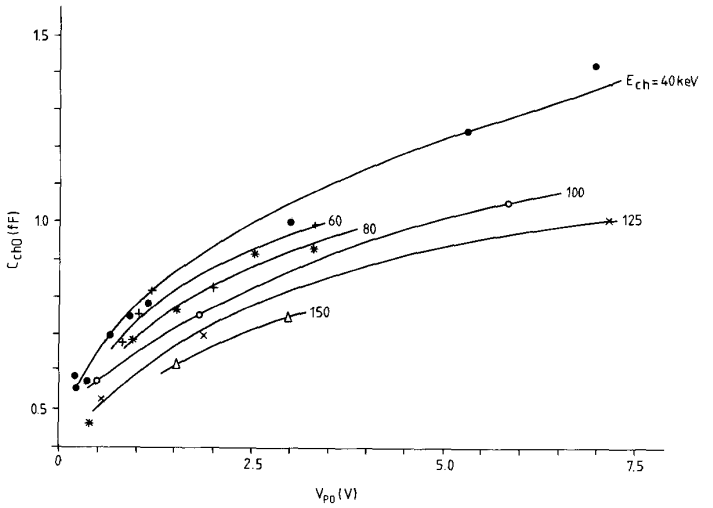

Fig. 8. Intrinsic channel to top-gate junction capacitance against the pinchoff voltage for $V_{GTS} = 0$.

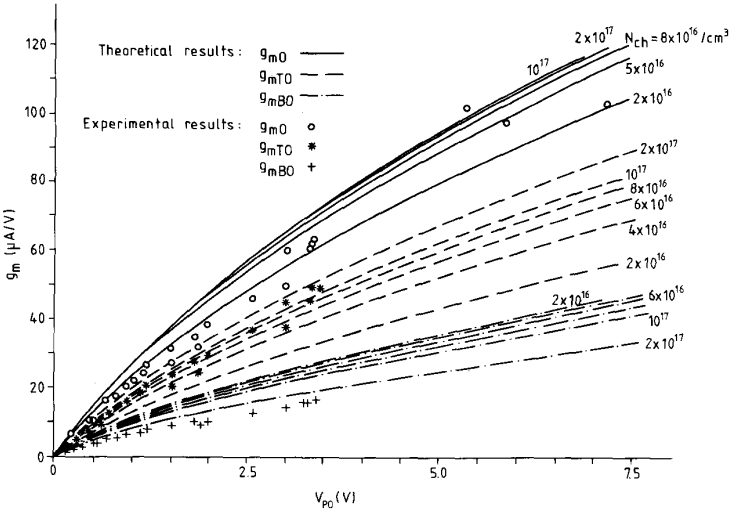

Fig. 9. Experimental and theoretical ($N_T = 10^{20}/\text{cm}^3$) results for the transconductances g_{m0}, g_{mT0}, and g_{mB0} against the pinchoff voltage, normalized to $Z/L = 1$.

V. Parasitic Resistance and Capacitances

A. Top-Gate Sidewall Capacitance

The top-gate capacitance is decisive for the high-frequency performance of the separated-gate JFET's. Examination of Fig. 3 shows that in the present process the parasitic capacitances of the top gate are composed not only of the sidewalls of the gate implantation, but also of the metal that overlaps the channel contacting regions. In particular, the sidewall capacitance may be quite significant because of the high boron concentration at the silicon surface. So, in view of the narrow gate length, it is of great interest to determine the influence of these parasites. The total top-gate capacitance can be expressed as

$$C_{GT} = C_{ch} + C_{sw} + C_m = LZC_{ch0} + 2ZC_{sw0} + 2L_mZC_{m0} \quad (22)$$

where C_{ch} is the intrinsic channel capacitance, C_{sw0} is the sidewall capacitance C_{sw} per micrometer, C_{m0} is the metal overlap capacitance C_m per square micrometer, and L_m is the metal overlap. Thus, the individual parts could be extracted by using a series of structures with different L and L_m. Much more accurate results, however, can be achieved by directly measuring the parasitic capacitances. For JFET's with relatively low V_{PO} (~ 1 V), isolation of these is in fact possible by pinching off the channel by a suitable reverse voltage over the bottom gate. The C_{ch0} can be well determined from test structures with large gate areas. With the measurements of the total parasitic capacitances, the individual values of C_{sw} and C_m can be extracted from some measurements on devices with different L_m.

For a minimum dimension device with $L = 2$ μm, $Z =$

100 μm, and $L_m = 3$ μm the distribution of capacitances is

$$C_{ch} = 0.127 \text{ pF}$$

$$C_{sw} = 0.156 \text{ pF}$$

$$C_m = 0.050 \text{ pF}.$$

Thus, the parasitic capacitances account for 60 percent of the total top-gate capacitance.

B. Source and Drain Contacting Regions

Ring-gate JFET's are by nature asymmetrical. For two reasons the drain is normally placed in the center:

1) to minimize the drain area and thus the drain capacitance, which deteriorates the overall frequency response, and
2) to maximize the source contacting area to the channel, so as to minimize R_S, which reduces g_m.

For the standard JFET in the present BIFET process, with $V_P = 1$ V, the sheet resistance of the intrinsic channel is nearly a factor of 10 higher than that of the extrinsic channel region formed by the channel implantation. The series resistances of the source and drain therefore are practically negligible. For much higher V_P's the two sheet resistances approach each other, and g_m as well as f_T will be attenuated. Here, it may then become advantageous to explicitly design the JFET to obtain a low extrinsic sheet resistance. This would in the present process imply using low-energy, instead of high-energy, channel implantations because this gives a steep implantation profile with a heavily doped surface. A relatively small amount of the total number of implanted channel ions then penetrate the gate implantation to form the intrinsic channel region.

VI. Biasing of the Gates

The effective pinchoff voltage V_P at which a separated-gate JFET will function in a circuit depends on the biasing of the two gates. The desired V_P can be achieved by any number of combinations of channel depth and gate biasing. The top-gate biasing influences the f_T. From (13)–(15) it is seen that increasing V_{GTS} gives some rise in f_T. The corresponding fall in g_m, however, is more marked. So, also in the view of the inconveniences of having high biasing voltages, it is nevertheless preferable to drive the device in the vicinity of $V_{GTS} = 0$. The presence of the built-in voltage already ensures that the depletion over the top-gate junction is so large that the device functions at a point far removed from the region where very high top-gate capacitance would seriously deteriorate the f_T.

In the present process the bottom-gate capacitance is very large and therefore very important for the overall frequency response. For this reason it is advantageous to reverse bias the bottom-gate junction as much as possible. Considerations of the parasitic top-gate to bottom-gate reachthrough diode lead to the same conclusion.

A. Top-to-Bottom-Gate Reachthrough Diode

The top-gate/channel/bottom-gate structure forms a reachthrough diode that will conduct current when the top-gate to bottom-gate voltage V_{GTB} is such that $V_{GTB} > V_{PTO}$ or $V_{GTB} < V_{PB0}$ [8], [11]. The top-gate to bottom-gate current I_{GTB} may furthermore excite electron–hole pairs in the totally depleted channel by impact ionization. This gives a hole current to the source and drain that, for the device with $V_{PO} = 1.5$ V, is quite significant. This is shown in Fig. 10, where I_D and I_{GTB} are plotted as a function of V_{GTS} for several V_{GBS}. For $V_{GBS} = 0$, I_D cannot be completely pinched off. With finite reverse biasing of the bottom gate, more top-gate voltage can be applied before the parasitic currents begin to play a role and I_D can be pinched off in a certain voltage span.

B. The Bulk Effect

As seen in Fig. 10 the bottom-gate biasing has a very large influence on the effective pinchoff voltage of the JFET. This effect is determined by the extension of the depletion width over the bottom-gate junction into the channel. As demonstrated in Section IV-B, the channel implantation tail is decisive for the width of this depletion region, and no attempt is made here to establish a simple relationship between V_P and V_{GBS}. However, attention is drawn to the fact that, to obtain high-frequency performance, the bottom-gate junction must not participate in the signal treatment. It therefore is reasonable to assume that the biasing of the bottom gate is prespecified, and on this basis a relatively simple model can be established. The simple quadratic model of the I–V characteristics, also used in SPICE [12] to simulate joined-gate JFET's, can (when disregarding reachthrough currents) be modified to suit the separated-gate case. A constant k is introduced with

$$k = \frac{V_{PT}}{V_P} \quad \text{at a fixed } V_{GBS} \tag{23}$$

where $V_P(V_{GBS})$ is the absolute of the drain voltage for which I_D saturates when $V_{GTS} = 0$, and $V_{PT}(V_{GBS})$ is the top-gate voltage required to pinch off the channel region. Moreover, $V_P(V_{GBS})$ is equal to the top-gate voltage needed to pinch off the channel region when the bottom-gate voltage follows V_{GTS} so that $V_{GTB} = V_{GBS}$. For a joined-gate device, $V_{PT} = V_P$. The dependence of I_D on V_{DS} and V_{GTS} can then in the forward region be expressed as

$$I_D = \begin{cases} 0, & V_{PT} - V_{GTS} < 0 \qquad (24) \\ \beta(V_{PT} - V_{GTS})^2(1 - \lambda V_{DS}), & \\ \quad 0 < V_{PT} - V_{GTS} < -\dfrac{1}{k} V_{DS} \qquad (25) \\ -\beta V_{DS}\{2(V_{PT} - V_{GTS}) - kV_{DS}\}(1 - \lambda V_{DS}), & \\ \quad 0 < -\dfrac{1}{k} V_{DS} < V_{PT} - V_{GTS}. \qquad (26) \end{cases}$$

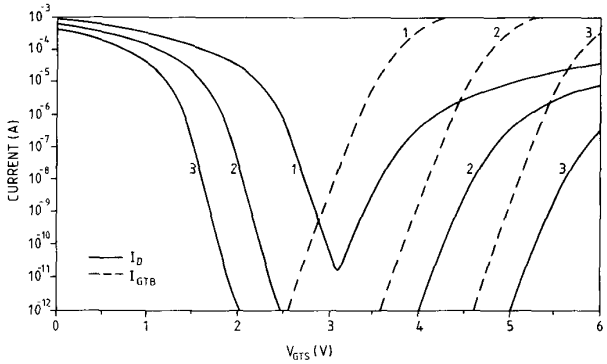

Fig. 10. Measurements of I_D (solid line) and I_{GTB} (dashed line) against (a) V_{GTS} with V_{GBS} = 0 (1), 1 V (2), 2 V (3), for a top-gate driven JFET with V_{P0} = 1.5 V, L = 2 μm, and Z = 100 μm.

The joined-gate JFET can be considered as a special case for which $k = 1$. As an example, a standard JFET (V_{PO} = 1.5 V) with Z = 100 μm is simulated for the bottom-gate biasing V_{GBS} = 0 and 2 V. The simulation parameters are extracted from measurements in the biasing point V_{GTS} = 0 and V_{DS} = −3 V, giving

for V_{GBS} = 0:

$$V_{PT} = 2.30 \text{ V}$$
$$k = 1.53 \ (V_P = 1.50 \text{ V})$$
$$\beta = 135 \ \mu\text{A/V}^2$$
$$\lambda = (25 \text{ V})^{-1} \tag{27}$$

and for V_{GBS} = 2 V:

$$V_{PT} = 1.30 \text{ V}$$
$$k = 1.30 \ (V_P = 1.00 \text{ V})$$
$$\beta = 198 \ \mu\text{A/V}^2$$
$$\lambda = (28 \text{ V})^{-1}. \tag{28}$$

In this manner, quite good fits are obtained, as in the example shown in Fig. 11. Only the effect of channel-length modulation, modeled by the parameter λ, is incorrectly represented. The output conductance in the forward saturation region is $g_{DS} \approx \lambda I_D$. Thus, the saturation conductance is proportional to the drain current but independent of V_{DS}. This relationship is inspired by the similar representation of the output conductance in bipolar junction transistors by the Early voltage. In reality, in a JFET $g_{DS} \to 0$ for increasingly negative V_{DS}, and for more accurate simulation, λ should be dependent on V_{DS}. It is furthermore noted that since ring-gate structures are basically asymmetric, the I–V relationships in the reverse region cannot be directly extracted from the simulation parameters in the forward region.

C. The Cutoff Frequency

The influence of the gate biasing on the cutoff frequency is illustrated by calculations on the above described standard device. The f_T is evaluated in three situations:

1) Joined gates with biasing $V_{GTS} = V_{GBS} = 0$ and $V_{DS} = -3$ V. Then

$$g_m = 974 \ \mu\text{A/V}^2$$
$$C_{GBS} = 0.50 \text{ pF}$$
$$C_{GTB-D} = C_{GTD} + C_{GBD} = 0.21 \text{ pF}$$
$$C_{\text{sub}} = 2.4 \text{ pF}$$

and from (1)

$$f_T = 48 \text{ MHz}.$$

2) Separated gates, top-gate driven, with biasing $V_{GTS} = V_{GBS} = 0$ and $V_{DS} = -3$ V. Then

$$g_{mT} = 608 \ \mu\text{A/V}^2$$
$$C_{GTS} = 0.15 \text{ pF}$$
$$C_{GTD} = 0.06 \text{ pF}$$

and from (2)

$$f_T = 460 \text{ MHz}.$$

3) Separated gates, top-gate driven, with biasing $V_{GTS} = 0$, $V_{GBS} = 2$ V, and $V_{DS} = -3$ V. Then

$$g_{mT} = 552 \ \mu\text{A/V}$$
$$C_{GTD} = 0.06 \text{ pF}$$
$$C_{GTB-B} = 0.19 \text{ pF}$$

and from (2)

$$f_T = 418 \text{ MHz}.$$

As expected, C_{sub} dominates the high-frequency performance of the joined-gate JFET. With separated gates the highest f_T is obtained in situation 2). Positive biasing of

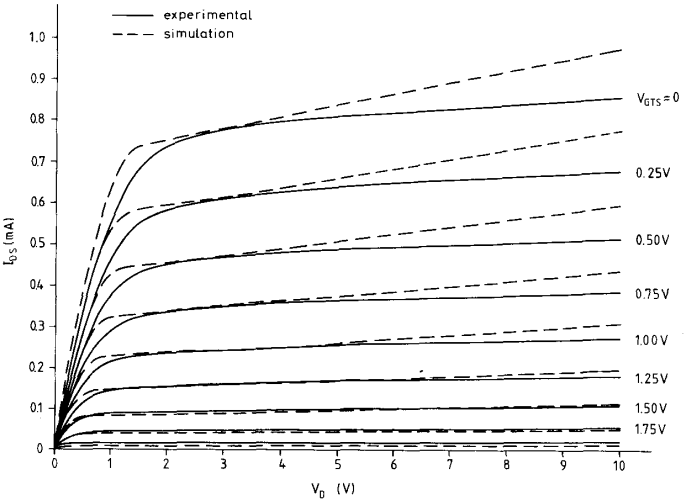

Fig. 11. The I-V characteristics of a top-gate driven JFET with $V_{P0} = 1.5$ V, $L = 2$ μm, $Z = 100$ μm, and $V_{GBS} = 0$.

the bottom-gate reduces f_T as a result of the decrease in g_{mT}, which is not significantly counteracted by the reduction in C_{GTD}. Situation 3) is regarded as the standard biasing scheme of the separated-gate device; hence, the choice of $V_P = 1$ V for this case. Reachthrough current must then be taken into account for $V_{GTB} \geq 4.3$ V instead of 2.3 V ($= V_{PT0}$) as in situation 2).

VII. Conclusions

Whether a p-channel JFET can be integrated in a given bipolar process is often a question of the reproducibility with which the channel region can be fabricated. To also achieve high-frequency performance, basically two requirements must be fulfilled by the technology: Firstly, the top gate must be separated from the bottom gate, and secondly, the top-gate length must be sufficiently narrow. The gate separation will usually also imply that the top-gate/channel/bottom-gate doping profile must be made the same under the whole width of the top gate. Ring-gate structures offer a simple solution, but in cases where the narrow gate length is achieved by self-aligned techniques, it may be necessary to contact the drain via a second metallization layer.

For high f_T, the channel must be lightly doped. The gain in g_m, which may be achieved by designing with a thin channel, is considerably reduced by the decrease in hole mobility caused by high doping effects. If device aspects other than the intrinsic channel are decisive for g_m, preference, however, may be given to a narrow highly doped channel. For example, this is the case when the extrinsic and intrinsic channel resistances become comparable, or when the channel depth is comparable to the channel length so that channel-length modulation becomes very important.

Modeling and application of the separated-gate JFET in circuits is considerably more complicated than for the joined-gate device. The large bulk effect makes it necessary to predetermine the gate biasing both in the technological device design and in the circuit design. Considerations of overall frequency response and the top-gate to bottom-gate reachthrough current make it advantageous to design with a finite reverse biasing of the bottom gate.

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References

[1] G. M. C. Meijer and F. L. J. Verweijen, "JFET's fabricated in a standard IC process for bipolar transistors," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 530–532, 1978.

[2] E. H. Nordholt, P. K. Nauta, and M. V. D. Veen, "A new method for realizing JFET's and super β's in a standard bipolar IC process," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 81–83, 1982.

[3] S. K. Lui and R. G. Meyer, "A high-frequency bipolar JFET I^2L process," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 1319–1323, 1982.

[4] C. J. M. Das, "Realizatie en modelleren van ionen-geimplanteerde junktie-veldeffekttransistoren in kompatibele processen," Ph.D. dissertation, Katholieke Universiteit, Leuven, Belgium, 1984.

[5] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 2nd ed. New York: Wiley, 1984.

[6] L. K. Nanver, "High-performance BIFET process for analog integrated circuits," Ph.D. dissertation, Delft Univ. of Technology, Delft, 1987.

[7] R. R. Bockemuehl, "Analysis of field effect transistors with arbitrary charge distribution," *IEEE Trans. Electron Devices*, pp. 31–34, 1963.

[8] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981.

[9] H. J. J. De Man, "A fast algorithm for the calculation of junction capacitance and its application for impurity profile determination," *Solid-State Electron.*, vol. 15, pp. 177–187, 1972.

[10] D. M. Caughey and R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proc. IEEE*, vol. 55, pp. 2192–2193, 1967.

[11] L. K. Nanver and E. J. G. Goudena, "Characteristics of separated-gate JFET's," *Electron Lett.*, vol. 22, pp. 1244–1246, 1986.

[12] L. W. Nagel, "SPICE 2: A computer program to simulate semiconductor circuits," Memor. ERL-M520, Electron. Res. Lab., Univ. of California, Berkeley, 1975.

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