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I–V CHARACTERISTICS OF INTEGRATED n^+pn^- REACHTHROUGH DIODES

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Abstract—Arsenic and boron implanted n^+pn^- reachthrough diodes have been produced in a high-frequency BIFET (bipolar-JFET) process. The *I–V* characteristics are here measured on structures formed by the top-gate/channel/bottom-gate sandwich of the separated-gate JFET's. A variety of reachthrough voltages have been realized by adjusting the implantation conditoins of the channel. Theoretically the *I–V* characteristics of the diodes are evaluated by solving the Poisson equation in the 1-D case with asymmetric gates. Special attention is paid to the voltage V_{FMRT} necessary to reach the flatband condition after reachthrough. The lowest values, approaching the junction built-in voltage, are achieved if the doping of the reverse biased gate is several times higher than that of the forward biased gate, a situation which is realized in the present n^+pn^- devices if $V_{GT} > V_{GB}$. High impact-ionization currents are measured just after reachthrough for devices with $V_{RT} > 1$ V, which in the JFET's gives undesirable source/drain currents.

NOTATION

E_f	Fermi energy level
k	Boltzmann constant
L	top-gate length
q	elementary charge
T	absolute temperature
Z	top-gate width
ϵ_s	permittivity of silicon
ψ_{bi}	built-in voltage of junction diode
$\psi_{biT(B)}$	built-in voltage of top (bottom) gate/channel junction

1. INTRODUCTION

This study of the *I–V* characteristics of n^+pn^- reachthrough diodes has been made in connection with the development of a high-frequency *p*-channel JFET which could be integrated in a high-performance bipolar process[1,2]. To achieve high-frequency performance of the JFET's, many of the capacitances associated with the bottom gate are eliminated by using top-gate driven configurations with a fixed bias on the bottom gate[3]. The general tendency has been to simulate these devices as a special sort of MOS transistor, but some important physical differences are then overlooked. Among these is the influence of the top-gate/channel/bottom-gate reachthrough diode. This diode is a fundamental part of JFET's operated with separated gates, and it may conduct a large gate current and subsequently parasitic source/drain currents, when the channel is pinched off by one of the gates[4]. For most analog purposes the JFET's operate continuously in the saturation mode far from pinchoff, but even then the parasitic currents can cause problems in start-up situations or in overdrive conditions. For JFET's operating in the subthreshold region, it will generally be compulsory to choose the biasing conditions such that no reachthrough current flows. Modeling of the reachthrough diode *I–V* characteristics in relationship to the normal JFET functions is thus a necessity.

The reachthrough diode itself has been proclaimed to have some interesting properties as an analog device, for example concerning the temperature stability and noise performance[5]. In principle they can be used as a replacement for the conventional Zener diodes, which cannot be designed with the same versatility. They have successfully been used as voltage rectifiers[6], but otherwise few applications have actually been reported. As a microwave device the reachthrough diode has been studied quite extensively as the so-called BARITT diode[7,8]. In all these studies the emphasis is on the optimization of the retarding field formed at the forward biased gate, which for microwave purposes gives the desirable negative resistance characteristics of the diodes. For applications in analog circuits or for voltage limiting, it is desirable to reduce the retarding field as much as possible, and the actual *I–V* characteristics, also when the retarding field is eliminated, are of central importance. These are studied here both experimentally and theoretically, particularly in relationship to the gate and channel doping profiles. On this basis the possibilities of producing reachthrough diodes which are attractive for analog applications are evaluated.

2. EXPERIMENTAL DEVICES

The experimental results quoted here have been measured on *p*-channel ring-gate JFET's produced in a double implantation BIFET process[1]. The basic

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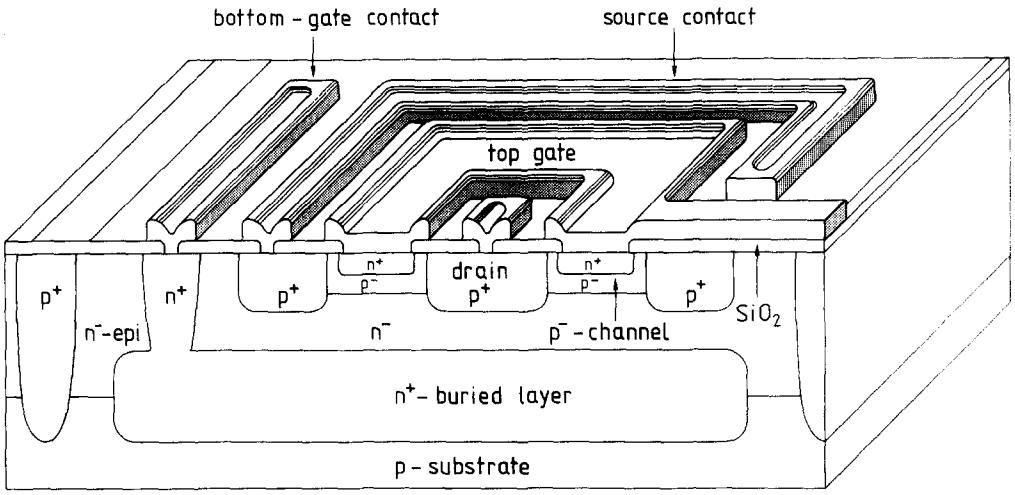

Fig. 1. Basic design of the n^+pn^- reachthrough diode as it is incorporated in the p-channel ring-gate JFET, without the second metallization layer.

design of these devices is shown in Fig. 1. Contact to the bottom gate is made via an n^+ diffusion contacting a n^+ buried layer in the 3.5 μm n^--type epitaxial layer. The n^+ top gate is formed by a $5 \times 10^{15}/cm^2$ arsenic implantation into the contact openings at an energy of 150 keV. This gate is a closed ring surrounding the drain, which is contacted via a second metallization layer. The boron channel implant is performed before the last 3000 Å oxidation step. A series of devices with different reachthrough voltages have been made by varying the channel implantation conditions. The top gate width of all the measured devices is $Z = 431$ μm and the length L varies from 2 to 11 μm.

3. THEORETICAL CONSIDERATIONS

The reachthrough principle is illustrated in Fig. 2 for an n^+pn^- structure. For the equilibrium situation of Fig. 2(a) the difference in the built-in voltages over the gates, originating from the difference in the gate doping levels, is indicated. When the bottom gate and channel are grounded, the top-gate voltage for which the corresponding depletion in the channel just reaches the depletion region over the bottom gate, is called the reachthrough voltage V_{RTT}. The bottom gate is pulled into a forward biasing condition by increasing the top-gate voltage V_{GT} beyond V_{RTT}, and electrons from the bottom gate may be emitted over the potential barrier ψ_B. The potentials V_T and V_B of

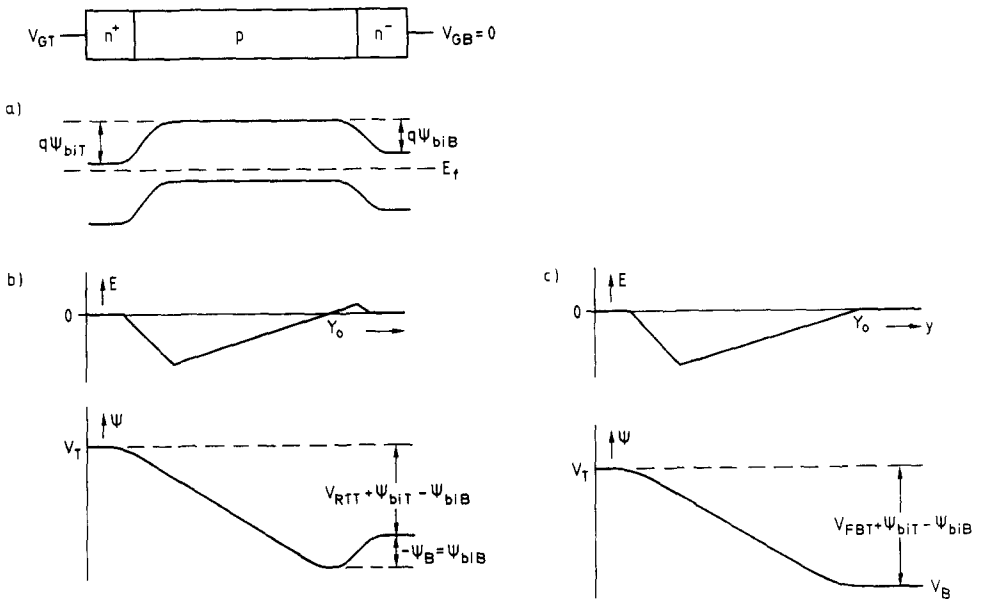

Fig. 2. Schematic illustration of (a) the energy band of a n^+pn^- structure at thermal equilibrium, and (b) the electric field and potential distributions at the reachthrough condition and (c) at the flatband condition.

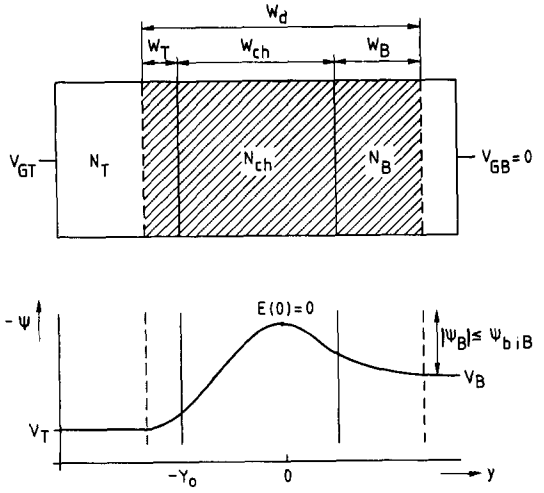

Fig. 3. Nomenclature used to describe the reachthrough diode for $V_{RTT} \leqslant V_{GTB} \leqslant V_{FBT}$.

Fig. 2(b) are related to the gate terminal biasing as:

$$V_T = V_{GT} + \psi_{biT} - \psi_{biB} \tag{1}$$

and

$$V_B = V_{GB} + \psi_{biT} - \psi_{biB} \tag{2}$$

The flatband condition illustrated in Fig. 2(c) is attained when V_{GT} reaches V_{FBT}, the voltage just necessary to make $\psi_B = 0$. With $V_{GT} = 0$ and $V_{GB} > V_{GT}$ the reachthrough and flatband voltages for the bottom gate, V_{RTB} and V_{FBB}, respectively, are defined in the same manner.

For gate voltages between reachthrough and flatband the reachthrough current I_{GTB} will be governed by the thermionic emission of electrons over the potential barrier ψ_B[9] so:

$$I_{GTB} = I_0 \exp\left\{\frac{-q|\psi_B|}{kT}\right\}. \tag{3}$$

Thus the behavior of the reachthrough current in this region can be deduced by establishing the relationship between ψ_B and the gate voltages V_{GT} and V_{GB}. This is done here by solving the Poisson equation in a structure of the type shown in Fig. 3. The doping levels N_T, N_{ch}, N_B of the top gate, channel and bottom gate, respectively, are assumed to be uniform and are defined as positive for p-type and negative for n-type doping. The depletion approximation is furthermore assumed, leading to the following expression for the reachthrough voltage:

$$V_{RTT} = -\psi_{biT} + \left|\frac{N_{ch}}{N_T}\right|(|N_T| + |N_{ch}|) \times (W_{ch} - W_{biB})^2 \cdot \frac{q}{2\epsilon_s} \tag{4}$$

with

$$W_{biB} = \frac{|N_B|}{|N_{ch}| + |N_B|}\sqrt{\frac{2\epsilon_s}{q} \cdot \frac{|N_{ch}| + |N_B|}{|N_{ch} N_B|}\psi_{biB}}, \tag{5}$$

and likewise for the bottom gate. The channel of width W_{ch} is completely depleted and the depletion widths into the top gate and bottom gate are denoted W_T and W_B, respectively, and $W_d \equiv W_T + W_{ch} + W_B$. In addition to the standard boundary conditons, the last constraint necessary to solve the Poisson equation is obtained by noting that a position in the channel exists where $\mathscr{E}(y) = 0$. This condition furthermore implies that W_T and W_B be positive. The potential distribution obtained by integration of the Poisson equation is:

$$\psi(y) = -\frac{qN_T}{2\epsilon_s}y^2 + c_{T1}y + c_{T0} \quad -(Y_0 + W_T) \leqslant y \leqslant -Y_0 \tag{6}$$

$$\psi(y) = -\frac{qN_{ch}}{2\epsilon_s}y^2 + c_{ch1}y + c_{ch0} \quad -Y_0 \leqslant y \leqslant W_{ch} - Y_0 \tag{7}$$

$$\psi(y) = -\frac{qN_B}{2\epsilon_s}y^2 + c_{B1}y + c_{B0} \quad (W_{ch} - Y_0) \leqslant y \leqslant W_B + W_{ch} - Y_0 \tag{8}$$

where c_{T1}, c_{ch1}, c_{B1}, c_{T0}, c_{ch0} and c_{B0} are integration constants, which for $V_{GTB} > 0$ are found to be:

$$c_{T1} = \frac{-q}{\epsilon_s}Y_0(N_T - N_{ch}) \tag{9}$$

$$c_{T0} = V_T - \frac{q}{\epsilon_s}[\tfrac{1}{2}N_T(Y_0 + W_T)^2 + Y_0(Y_0 + W_T)^2 + Y_0(Y_0 + W_T)(N_{ch} - N_T)] \tag{10}$$

$$c_{ch1} = 0 \tag{11}$$

$$c_{ch0} = \frac{3q}{2\epsilon_s}Y_0^2(N_T - N_{ch}) + c_{T0} \tag{12}$$

$$c_{B1} = \frac{q}{\epsilon_s}(W_{ch} - Y_0)(N_{ch} - N_B) \tag{13}$$

$$c_{B0} = V_B - \frac{q}{\epsilon_s}[\tfrac{1}{2}N_B(W_{ch} - Y_0 + W_B)^2 + (W_{ch} - Y_0) \times (W_{ch} - Y_0 + W_B)(N_{ch} - N_B)] \tag{14}$$

where:

$$Y_0 = \frac{W_{ch}}{(N_B - N_T)N_{ch}}\left(N_T(N_B - N_{ch}) - \sqrt{N_T N_B\left[W_{ch}^2(N_{ch} - N_B)(N_{ch} - N_T) - \frac{2\epsilon_s}{q}(N_B - N_T)V_{TB}\right]}\right) \quad \text{for } N_T \neq N_B \tag{15}$$

$$Y_0 = \frac{1/2W_{ch}^2 N_{ch}(N_T - N_{ch}) + (V_{GTB} + \psi_{biT} - \psi_{biB})\epsilon_s/q}{W_{ch}[N_{ch}(N_T - N_{ch})]} \quad \text{for } N_T = N_B \tag{16}$$

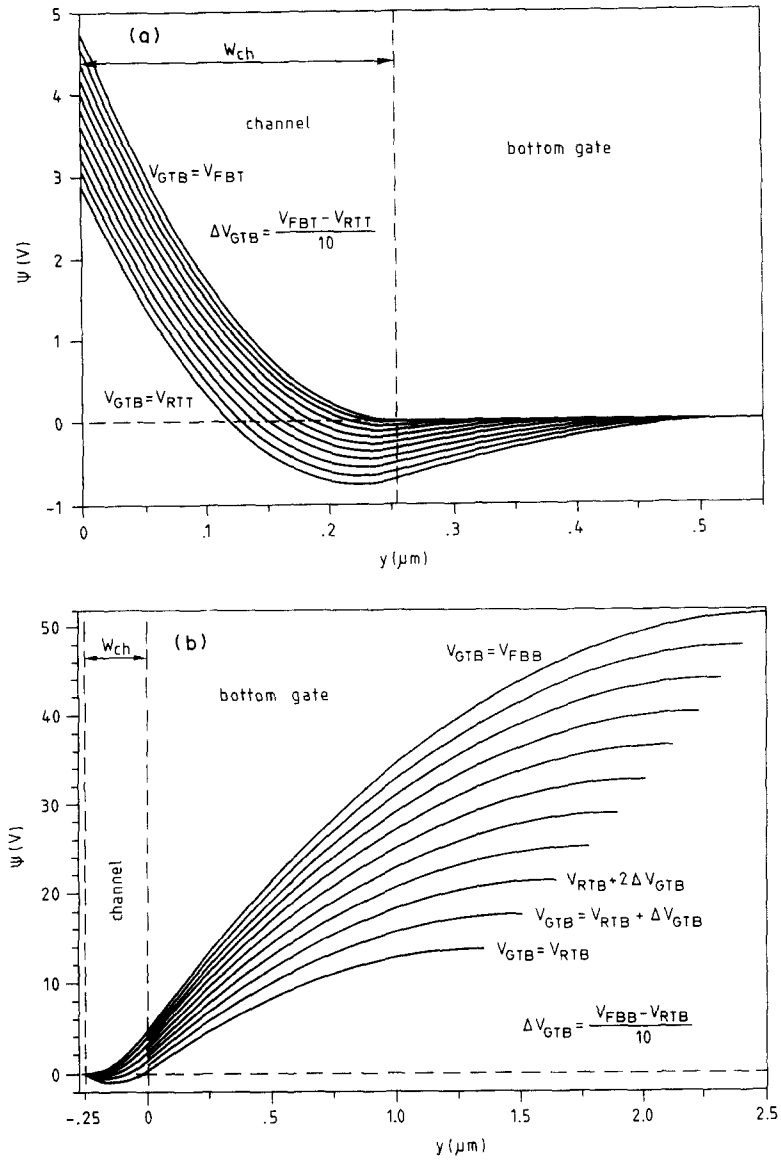

Fig. 4. Simulation of the potential distribution in the depleted region of a n^+pn^- reachthrough diode as a function of V_{GTB}, for (a) $V_{GTB} > 0$, and (b) $V_{GTB} < 0$. The doping levels are $N_T = 10^{20}/cm^3$, $N_{ch} = 10^{17}/cm^3$ and $N_B = 10^{16}/cm^3$, and $W_{ch} = 0.25\ \mu m$.

$$W_T = -Y_0 \frac{N_{ch}}{N_B} \tag{17}$$

$$W_B = -(W_{ch} - Y_0)\frac{N_{ch}}{N_B} \tag{18}$$

$$\psi_B = \frac{q}{2\epsilon_s} Y_0^2 N_{ch}\left\{\frac{N_{ch}}{N_T - 1}\right\} + V_{GTB} + \psi_{biT} - \psi_{biB} \tag{19}$$

$$V_{FB} = \frac{q}{2\epsilon_s} W_{ch}^2 N_{ch}^2\left\{\frac{1}{N_{ch}} - \frac{1}{N_T}\right\} - \psi_{biT} + \psi_{biB} \tag{20}$$

For $V_{GTB} < 0$, the indices T and B are interchanged.

Figure 4 shows an example of the potential distribution in an n^+pn^- reachthrough diode, as calculated by eqn (6)–(8). For $V_{GT} > V_{GB}$ the lowering of ψ_B almost linearly follows the increase in V_{GTB}. On the other hand, for $V_{GB} > V_{GT}$ the bottom-gate voltage is largely used to stretch the depleted region into the gate itself, giving an increasingly inefficient lowering of ψ_B. This is seen directly in Fig. 5, where the behavior of $\psi_B(V_{GTB})$ is shown in the three situations: $N_T \gg N_B$, $N_T = N_B$ and $N_T \ll N_B$. For $N_T \gg N_B$ and $V_{GTB} \to V_{RTT}$, linear behavior is observed and exponential I–V characteristics are expected. A special case results for $N_T = N_B$, where ψ_B is quadratic in V_{GTB}[9].

Beyond V_{FB} the current increases to levels where the injected charge density may exceed the fixed charge. The charge density N_J corresponding to the current density J is given by:

$$N_J = J/v, \quad v = \mu\mathscr{E}. \tag{21}$$

For large enough electric fields the carrier drift

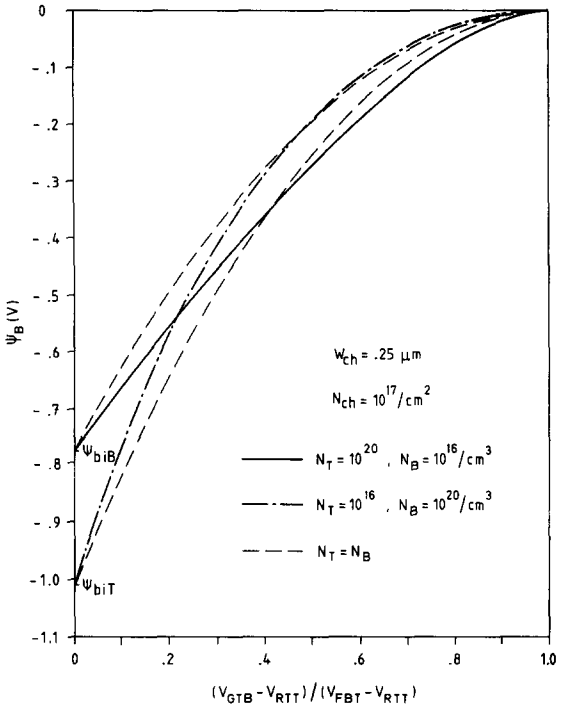

Fig. 5. Simulations of ψ_B against the normalized gate voltage difference.

velocity, v, saturates to v_s and the Poisson equation becomes:

$$\frac{\partial^2\psi}{\partial y^2} = \frac{q}{\epsilon_s}\left\{N + \frac{J}{qv_s}\right\}, \tag{22}$$

For sufficiently high currents the last term becomes dominating and the Poisson equation solves to give

$$V_{GTB} = \frac{J}{\epsilon_s v_s}(W_T + W_{ch} + W_B)^2$$

$$\text{for } V_{GTB} \gg V_{FBT} \text{ or } V_{GTB} \ll -V_{FBB}. \tag{23}$$

For high enough reverse biasing the variations in depletion widths will become insignificant and the reachthrough diode will have a constant differential resistance.

4. RESULTS

A typical example of the experimentally determined I–V characteristics of reachthrough diodes is shown in Fig. 6. As predicted by the theoretical calculations the asymmetry in gate doping gives $V_{RTT} \ll V_{RTB}$. Just after reachthrough I_{GTB} increases exponentially for $V_{GT} > V_{GB}$, but much less rapidly for $V_{GB} < V_{GT}$. For high gate currents the behavior becomes linear with a differential resistance which is dependent on the sign of V_{GTB}. Figure 6 also shows that the gate dimensions in this case are so large that the biasing of the channel contacting regions have no significant influence on I_{GTB}.

A. The flatband to reachthrough voltage

When designing reachthrough diodes for functions similar to those associated with Zener diodes, the voltage:

$$V_{FMR} \equiv V_{FB} - V_{RT} \tag{24}$$

can be compared to the built-in voltage of the junction diodes. Particularly important for the value of V_{FMR} are the relative doping levels of the gates, and we define:

$$V_{FMRT} \equiv V_{FBT} - V_{RTT} \tag{25}$$

$$V_{FMRB} \equiv V_{FBB} - V_{RTB} \tag{26}$$

For given values of N_T, N_B and V_{RTT}, the lowest V_{FMRT} is achieved for narrow, highly doped channels, the lower limits of V_{FMRT} being ψ_{biB}. More influential, however, is the relative doping of the gates. The lowest value of V_{FMRT} is achieved when $N_T \gg N_B$. This is illustrated in the theoretical calculation of Fig. 7, where $N_{ch} = 10^{17}/\text{cm}^3$ and W_{ch} is chosen so as to give

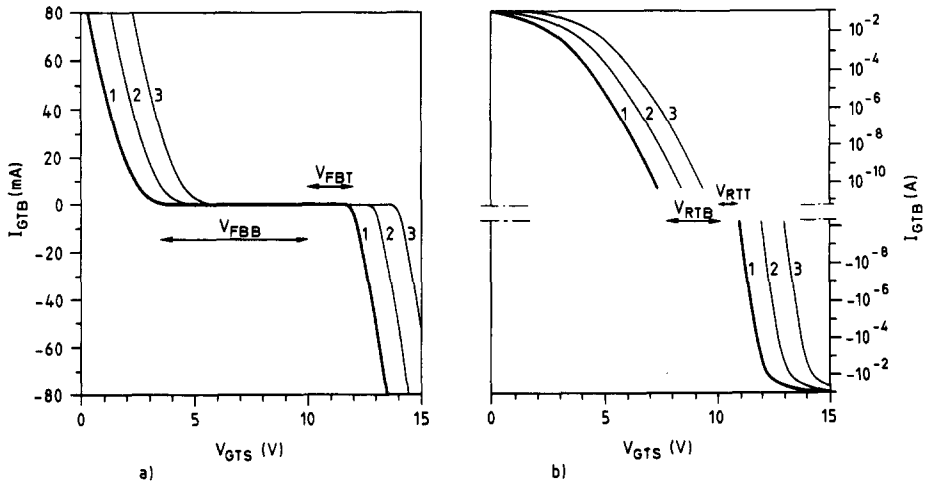

Fig. 6. The linear (a) and logarithmic (b) reachthrough diode characteristics of a device with $L = 8$ μm. I_{GTB} is plotted against V_{GTS} with V_{GBS} fixed at (1) 10 V, (2) 11 V and (3) 12 V. The reachthrough and flatband voltages are indicated for the bold curve (1).

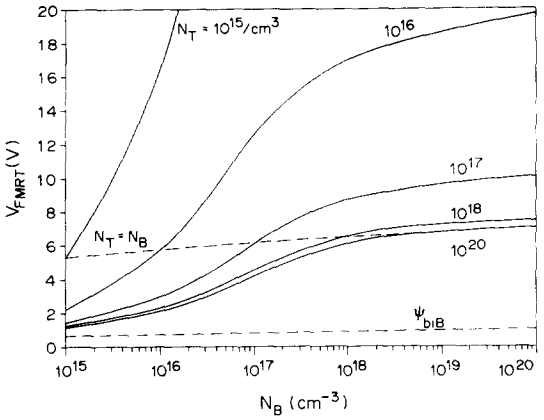

Fig. 7. Simulations of V_{FMRT} against N_B for various values of N_T, with $N_{ch} = 10^{17}/cm^2$ and $V_{RTT} = 5$ V.

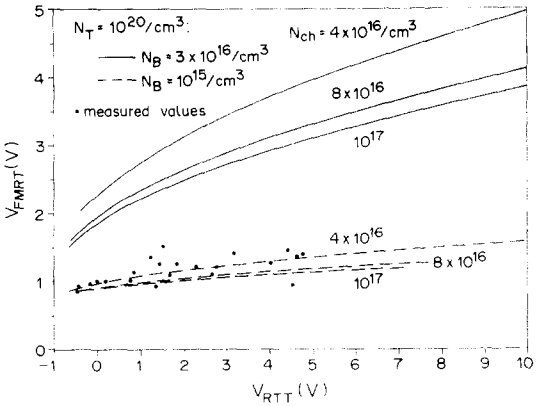

Fig. 9. Simulations of V_{FMRT} against V_{RTT} compared to the values measured for the devices represented in Fig. 8.

$V_{RTT} = 5$ V. Values of V_{FMRT} near ψ_{biB} are achieved for $N_T/N_B > 10^4$.

Figure 8 shows the experimentally determined relationships between the reachthrough and flatband voltages of devices produced under a series of different channel-implantation conditions. No clear correlation to the implantation dose or energy was observed so these parameters are not explicitly indicated. The corresponding V_{FMRT} values are plotted in Fig. 9. Attractively low values from ~1 to 1.5 V are obtained for all devices, with only a slight increase being observed for increasing V_{RTT}. Comparison to the simulated curves also plotted in Fig. 9, shows that such low V_{FMRT} values can be achieved by assuming a very low doping of the epitaxial bottom gate. Here $N_B = 10^{15}/cm^3$ is used instead of the actual $3 \times 10^{16}/cm^3$. A channel implantation tail can account for such an effective lowering of the epi-doping at the junction between the channel and epi-layer.

B. Beyond the flatband condition

Beyond the flatband condition the I–V characteristics become linear. The corresponding differential resistance for a diode with a $1 \times 1\ \mu m^2$ top gate, R_0, can be evaluated from eqn (23) by setting $v_s = 10^7$ cm/s and $(W_T + W_{ch} + W_B) = 0.5\ \mu$m. Thus:

$$R_0 = \frac{(W_T + W_{ch} + W_B)^2}{2\epsilon_s v_s} \approx 10^4\ \Omega\mu m^2. \quad (27)$$

This is of the order of magnitude measured in the experimental devices. The corresponding charge storage effect of the voltage dependent depletion over the channel region is represented by the capacitance

$$C \approx \epsilon_s/(W_T + W_{ch} + W_B) = 1.8 \times 10^{-5}\ pF/\mu m^2 \quad (28)$$

which is about a factor 100 lower than the capacitance over the top-gate junction diode.

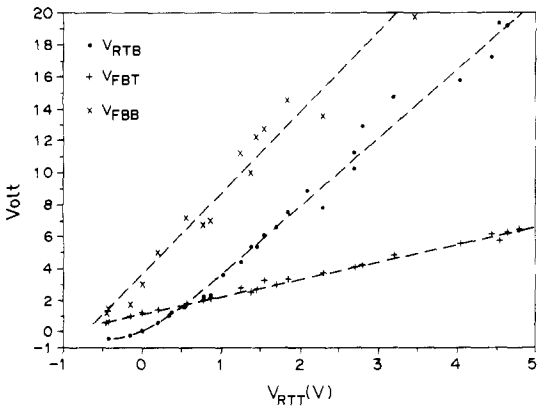

Fig. 8. Experimentally determined relationship between V_{RTT}, V_{RTB}, V_{FBT} and V_{FBB}, for a variety of devices produced with a channel implantation energy between 40 and 150 keV, and a dose between 0.5 and $12.5 \times 10^{13}/cm^2$.

C. Impact-ionization currents

The electric field over the depleted channel can become so large that the electrons injected after reachthrough, gain enough energy to excite electron–hole pairs by impact ionization. The total hole current thus created in the channel may be expressed as:

$$I_p = \int_0^{W_d} \alpha(\mathscr{E}) I_{GTB}\, dy, \quad (29)$$

where $\alpha(\mathscr{E})$, the electron ionization rate, is defined as the number of electron–hole pairs generated per unit distance[9]. Figure 10 shows the three types of current which may flow in a reachthrough diode structure. The electrons created by impact ionization may be collected at the reverse-biased gate and the corresponding holes at the forward-biased gate. If the channel is contacted and reverse biased with respect to the gates, as is the case in JFET's, the holes may also be swept to the channel contacts giving a current I_{ch}. The experimental results of Fig. 11, show I_{ch} relative to I_{GTB} for a number of devices with V_{RTT} up to 4.5 V. For subthreshold devices ($V_{RTT} < 0$) the channel is very thin and I_{ch} is barely significant. On the contrary, for devices with large V_{RTT}, I_{ch} reaches levels which cannot be ignored. The gate junction diode leakage current is normally insignificant compared to I_{ch}.

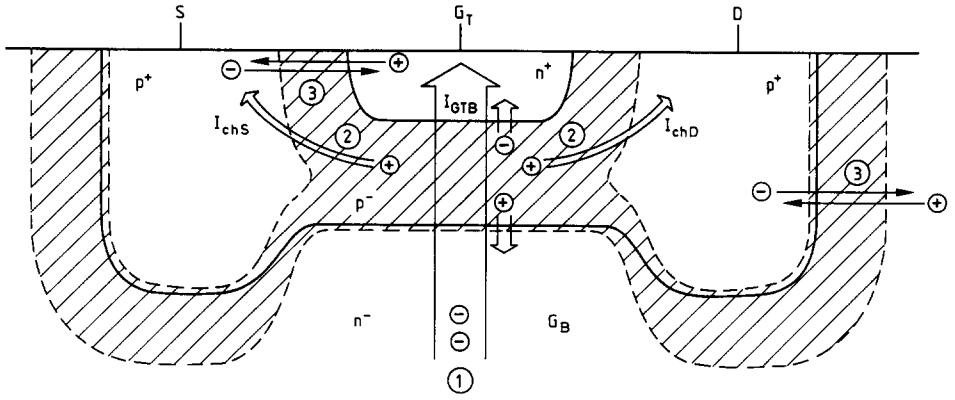

Fig. 10. Currents in a JFET structure with $V_{DS} = 0$ and the reachthrough diode biasing $V_{GTB} > V_{RTT}$. The depleted regions are shaded and the indicated currents are (1) I_{GTB}. (2) Impact-ionization currents, and (3) diode leakage currents.

The measurements displayed in Fig. 11 were for $V_{GT} > V_{GB}$. For $V_{GT} < V_{GB}$ the ratio I_{ch}/I_{GTB} is about an order of two smaller. This can be correlated to a dependence of $\mathscr{E}$ on the total depletion width. In a first order approximation $\mathscr{E}$ is given by

$$\mathscr{E} \approx \frac{V_{GTB}}{W_d}. \tag{30}$$

For $V_{GT} > V_{GB}$ and $V_{GTB} > V_{FBT}$, the depletion widths W_T and W_B are near zero so $W_d \approx W_{ch}$, and for $V_{GB} > V_{GT}$ and $V_{GTB} < V_{FBB}$, $W_T \approx 0$ but $W_B > 0$ so $W_d \approx W_{ch} + W_B$. The number of electron–hole pairs created at a given current level depends more strongly on $\mathscr{E}$ via $\alpha(\mathscr{E})$ than on W_d, so these simple calculations also imply that I_{ch} will be largest for $V_{GT} > V_{GB}$. Direct experimental verification can be made on devices where V_{RTT} and V_{RTB} are not too far apart. This is demonstrated in Fig. 12.

The correlation between I_{ch} and the shape and size of the top gate, will depend on the gate biasing. Before the flatband condition the barrier ψ_B, over which the electrons giving I_{GTB} are emitted, also forms a barrier for the holes created by impact ionization. These are therefore retained in a well between the two gates, and the probability that they will be swept to the channel contacts is large. In this case I_{ch} will increase with L. For $|V_{GTB}| > |V_{FB}|$, I_{ch} becomes independent of L, because holes may then readily recombine at the forward-biased gate.

D. *Influence of reverse biasing of the gates*

The path of the reachthrough current over the channel region is bounded at the channel contacting regions by the potential barriers formed by the built-in voltage plus any reverse biasing. The spatial restriction in I_{GTB} is larger, the higher this reverse biasing. With a floating channel the restraint falls away and the potential over the gates will extend as far as possible into the peripheral channel regions. This gives an effectively larger gate length and I_{GTB} attains a maximum value. For the present devices, the reverse biasing of the channel has little influence on I_{GTB}, even for devices with $L = 2\ \mu$m. To experimentally determine the effective channel length, disturbing effects from impact ionization and parasitic series resistances must be avoided. This is possible for devices with low reachthrough voltage, if measurements are made just after reachthrough. In the example shown in Fig. 13, extrapolation of the curves drawn through the measured values of I_{GTB} against L,

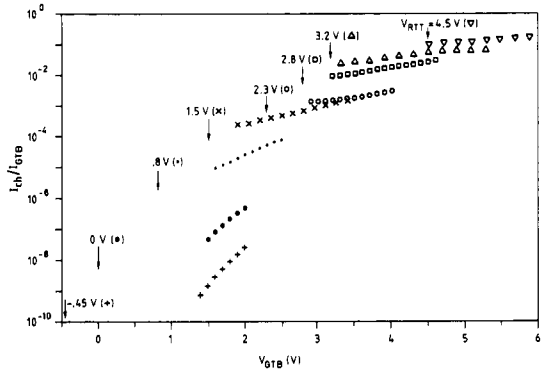

Fig. 11. The ratio of I_{ch} to I_{GTB} against V_{GTB} for devices with $L = 2\ \mu$m. The interval between reachthrough and the onset of measurable I_{ch} is visualized by an arrow indicating V_{RTT}.

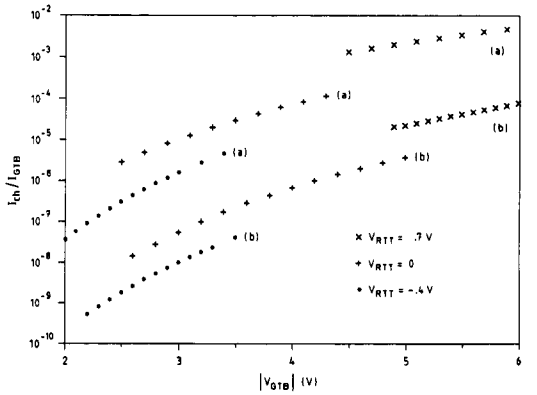

Fig. 12. The ratio of I_{ch} to I_{GTB} against V_{GTB} for three devices with $L = 2\ \mu$m, for (a) $V_{GTB} > 0$, and (b) $V_{GTB} < 0$.

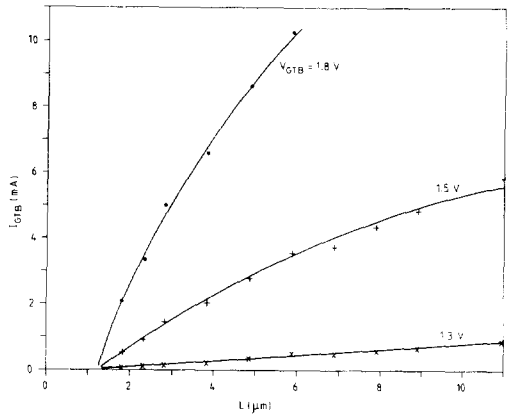

Fig. 13. I_{GTB} against L for a set of devices with $V_{RTT} = 0.7$ V.

indicates that the flow of I_{GTB} would be retained for gate lengths less than about 1 μm. For such gate lengths, large effects of the reverse biasing are thus to be expected.

5. DISCUSSION AND CONCLUSIONS

The asymmetrical gate doping of the n^+pn^- reachthrough diode gives this device I–V characteristics which resemble those of the conventional n^+p junction diode. Wtih V_J representing the voltage over the junction, the characteristics of the latter basically fall into four regions:

(1) $V_j < V_{BV}$, the junction breakdown region, where V_{BV} is the reverse voltage necessary to give breakdown
(2) $V_{BV} < V_J < 0$, the reverse biased region with reverse leakage current
(3) $0 < V_J < \psi_{bi}$, the low-current forward region having exponential I–V characteristics
(4) $\psi_{bi} < V_J$, the high-current forward region where the series resistance of the terminals limits the current

In the reachthrough diode the corresponding ordering is:

(1) $V_{GTB} < V_{FBB}$, high current region, with a nearly constant differential resistance determined by the space-charge-limited current flow over the channel and the series resistance of the bottom-gate terminal
(2) $V_{FBB} < V_{GTB} < V_{RTB}$, low current region, where I_{GTB} increases slowly with V_{GTB}
(3) $V_{RTT} < V_{GTB} < V_{FBT}$, low current region, where the increase in I_{GTB} with V_{GTB} is near exponential
(4) $V_{FBT} < V_{GTB}$, high current region with characteristics such as in region (1)

Furthermore, in the region $V_{RTB} < V_{GTB} < V_{RTT}$ no current flows directly from gate to gate. It is the fact that $N_T \gg N_B$ which assures that $V_{RTT} \ll V_{RTB}$ and $V_{FMRT} \ll V_{FMRB}$. In the present process the boron implantation tail assures an effectively very low N_B, so independent of the channel doping profile the V_{FMRT} is not much higher than 1 V.

With the divisions given above the reachthrough diode could be directly used as a junction diode, with $V_{RTT} + V_{FBT}$ corresponding to the junction built-in voltage and $V_{RTB} + V_{FBB}$ to the breakdown voltage. For most applications however it is most attractive to work in the region $V_{GTB} > 0$, because here the low V_{FMRT} gives a well defined transition to the high current region. In junction diodes the breakdown voltage is determined by the doping levels at the junction, but usually only devices with $V_{BV} = 6.5$ V are produced because away from this point the temperature stability is too poor. For V_{BV} higher than 6.5 V, the breakdown is due to avalanching and below this value tunneling is the most important factor, making it difficult to produce junction diodes with accurate low voltage breakdowns. The underlying principle of the reachthrough mechanism however assures good temperature stability of the reachthrough point, and reproducible manufacture of devices with any reachthrough voltage less than the breakdown voltage of the junction involved, relies only on the reproducibility of the channel.

In the devices produced here the differential resistance in the high current regions is rather high. The contribution made by the series resistance of the bottom-gate terminal could be reduced by using a thinner epitaxial layer. The resistance in the reachthrough diode itself would be decreased by using thinner, more heavily doped channels. The frequency response of the device is then also improved since the decrease in R_0 with W is more rapid than the corresponding increase in the capacitance over the gates. Both a thinner channel (or base) and thinner epi-layer are strived for in high-frequency bipolar processes, so the optimization of such processes also makes possible the integration of low resistance reachthrough diodes. Together with the very low capacitance over the gates such devices may be very attractive for high-frequency purposes.

In the separated-gate JFET's the pinchoff voltages of the top and bottom gates, V_{PT0} and V_{PB0} respectively, are defined such that $V_{RTT} = V_{PT0}$ and $V_{RTB} = V_{PB0}$[2]. This means that in a top-gate driven device a top- to bottom-gate current will flow for $V_{GTB} > V_{PT0}$. Subthreshold JFET's, where the channel is so thin that the built-in voltage over the gates completely depletes the channel, will therefore in normal operation be conducting a reachthrough current. The associated impact-ionization current is in this case only significant for V_{GTB} well beyond reachthrough, so it is nevertheless possible to achieve a true pinchoff of the source–drain current. For the more commonly used JFET's with pinchoff voltages from about 1–3 V, both the currents I_{ch} and I_{GTB} are a problem for $V_{GTB} > V_{RTT}$. With a finite reverse biasing of the bottom gate the effective pinchoff of the top gate is reduced. The top gate then pinches off the channel at a lower voltage than the voltage

$V_{GTS} = V_{RTT} + V_{GBS}$ where I_{GTB} is initiated. Beyond pinchoff there is then a voltage span V_{GBS} in which no current flows from gate to gate and the source–drain current can be pinched off. Designing with a finite reverse biasing of the bottom gate is also advantageous for the frequency response of the JFET's[2] and as a general rule separated-gate JFET's should be designed for use with the maximum V_{GBS} allowed by the voltage capabilities of the process. Due to the large influence of V_{GBS} on the effective pinchoff of the top gate, the top-gate biasing must be considered in the technological design of the JFET's.

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REFERENCES

1. L. K. Nanver, Ph.D. dissertation, Delft University of Technology, Delft (1987).
2. L. K. Nanver and E. J. G. Goudena, *IEEE Trans. Electron Devices* **ED-35,** 1924 (1988).
3. S. K. Lui and R. G. Meyer, *IEEE Trans. Electron Devices* **ED-29,** 1319 (1982).
4. L. K. Nanver and E. J. G. Goudena, *Electron Lett.* **22,** 1244 (1986).
5. D. de Cogan, *Microelectronics* **8,** 20 (1977).
6. P. J. Kannam, *IEEE Trans. Electron Devices* **ED-23,** 879 (1976).
7. S. M. Sze, D. J. Coleman Jr and A. Loya, *Solid-St. Electron.* **14,** 1209 (1971).
8. O. Eknoyan, E. S. Yang and S. M. Sze, *Solid-St. Electron.* **20,** 291 (1977).
9. S. M. Sze, *Physics of Semiconductor Devices*, 2*nd edn*, p. 355. Wiley-Interscience, New York (1981).