

A Switched Capacitor Digital Sine-Wave Mixer for Software Defined Radio

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Abstract—This paper proposes a discrete-time mixer: the sampled RF input is multiplied by digital sinewave-LO samples. The multiplication is implemented by charge sharing between a unary weighted sampling capacitor and an output capacitor. Spurious responses as low as -56dBc are achieved due to the good linearity and matching properties of capacitors. Four 5GS/s time-interleaved samplers are implemented to cover the entire RF range from 0.1GHz to 4.9GHz , while simultaneously providing 50Ω impedance matching. Any radio channel narrower than 20MHz in this RF range can be received at a fixed 20GS/s sample rate. The worst case spurious response, caused by time-errors in the interleaving clock phases, is at -36dBc (uncalibrated). Other measured parameters, of the 28nm CMOS IC occupying an active area of 0.45mm^2 , over the RF band from 1.1 to 4.9GHz are: $\text{NF}=14\text{dB}-16\text{dB}$ (single-side band), $\text{IIP3}>+12\text{dBm}$, $\text{P1dB}>+2\text{dBm}$, and $\text{P}=135\text{mW}$ at a fixed RF sample rate of 20GS/s .

Index Terms—Carrier aggregation, Direct Digital Frequency Synthesis (DDFS), discrete-time mixing, harmonic rejection, multi-band, multi-channel, RF sampling, software-defined radio, switched-capacitor, wideband sampling.

I. INTRODUCTION

System architectures that have a single fixed system clock are emerging [1]–[3]. Continuous coverage of RF channels has been demonstrated at an RF up to 1GHz [2], [3], but higher frequencies are desired. Single clock domain architectures have several advantages as they do not have clock domain coupling while having a much wider tuning range compared to traditional PLLs. As well as the flexibility to choose the clock frequency independent of the receive frequency. Therefore, no fractional-N Phase Locked Loop (PLL) is required and the receiver PLL can even be omitted when using the transmitter PLL in FDD systems. Our architecture comes with a different balance in power dissipation between mixer and frequency synthesizer.

This work does not target a specific application but explores what is feasible in a mainstream 28nm CMOS technology when increasing the input frequency. Capacitor weighting is proposed to lower the spurious responses, since capacitors are expected to have better component matching compared to resistors and transconductors which are used in [2], [3]. The

RF coverage in [2] is limited by internal parasitic capacitances which are eliminated in our proposed architecture since every internal node has an intended capacitance. Moreover, our architecture features a reduced input parasitic, which was limiting the RF coverage in [3]. The proposed architecture is able to receive any RF channel narrower than 20MHz located between 0.1GHz and 4.9GHz at a fixed 20GS/s system sample rate (the channel width and RF are limited by the size of our Look-Up Table (LUT)). The main novelty of this work is the use of switched capacitor weighing to implement RF down-mixing in a digitally controllable way.

II. ARCHITECTURE AND IMPLEMENTATION

A digital mixer is implemented, allowing for a mixer frequency (f_M) independent of the system clock. First the RF input signal is sampled (at frequency f_S). After sampling, the samples are multiplied by a 10-bit value stored in a LUT. Mixer functionality is obtained by storing a sinewave (of frequency f_M) in the LUT. The proposed receiver architecture is shown in Figure 1:

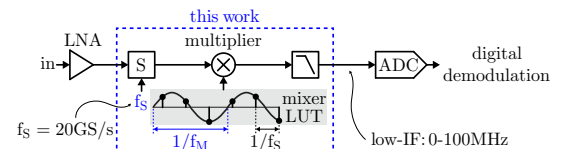


Fig. 1. Proposed receiver with a digital mixer.

The sample capacitor is reset (during ϕ_R) before sampling (during ϕ_S) to provide a switched capacitor load on the RF port for input impedance matching (see Figure 2). Note that this reset isolates the mixer operation from the input matching. The sampler is sliced into multiple samplers with a total sampling capacitance of value C_S . During the mixing clock phase (ϕ_M), the sampled charge is split between the positive and negative outputs. In Figure 2, a fraction α of the sampled charge is sent to the positive output, and a fraction $1 - \alpha$ is sent to the negative output, with α a value between 0 and 1 set by a 10-bit LUT code. As a result of charge sharing between the positive and negative sampling capacitors, a multiplication factor in the voltage domain is obtained. Controlling the multiplication factor α sinusoidally over time provides the desired mixer functionality. Note that, in contrast to mixing by a square wave, multiplication by a sinewave provides harmonic rejection. The signal weighting shows some similarity to the discrete-time harmonic rejection mixer in [4]. However, in [4], the RF channel selection is performed by tuning the LO-

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frequency while we use a fixed sampling frequency and tune the mixer frequency by updating the LUT.

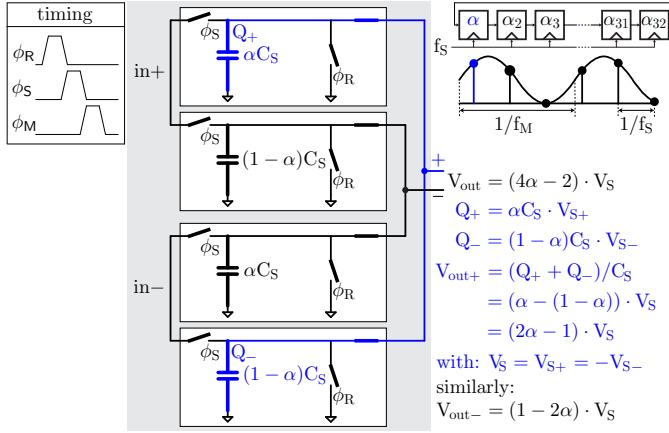


Fig. 2. Equivalent circuit, modelling the charge sharing during the mixer clock phase (ϕ_M) with example multiplication factor α (V_{out} will simultaneously be low-pass filtered, not shown).

It is shown in [5] that clock jitter requirements for RF sampling and mixing are similar, which holds both for charge and voltage sampling [6].

A. Relation between sampling frequency, mixer frequency, and LUT size

A number of k periods can be stored in the LUT of size N to change the mixer frequency: $f_M = f_S \cdot k/N$, where k is an integer ($1 < k < N/2$ to satisfy the Nyquist criterion). For this test chip, a compact LUT size of $N=128$ is chosen; however, a larger LUT size is also possible to obtain a finer f_M resolution. The LUT can even be omitted when implementing the CORDIC algorithm in hardware to generate the sinewave samples.

With the implemented LUT, 323 mixer frequencies can be generated between 0.1GHz and 4.9GHz; by varying the number of periods stored in the LUT and by varying the LUT size from 8 to 128 (in steps of 4 because of 4x interleaving). The largest frequency step is 80MHz and occurs twice around 2.5GHz. The smallest frequency step is 5MHz, and the median and average frequency steps are 12MHz and 15MHz respectively. Instead of increasing the mixer frequency resolution, a low IF architecture that has a variable IF is proposed. If the mixer frequency step is smaller than 80MHz, it is guaranteed that any 20MHz RF channel can be down converted to a low IF frequency between 0Hz and 100MHz ($100\text{MHz} - 80\text{MHz} = 20\text{MHz}$). Moreover, a 100MHz base-band bandwidth is low enough to maintain the A/D conversion at reasonable power level. This 20MHz RF channel bandwidth is dictated by the chosen LUT size together with both the IIR filter cut-off and ADC bandwidth limitations. The RF channel bandwidth can be increased by proportionally increasing the LUT size until the bandwidth is limited by the IIR-filter. The mixer core itself can handle more wideband signals without requiring additional power consumption.

B. Circuit sizing

The sampler is sliced into 256 unary weighted slices. Each unit slice has an almost minimum sized NMOS switch

($W/L=150\text{nm}/30\text{nm}$) and a 5fF MOM sample capacitance. The small switch size minimizes the parasitic at the RF node, resulting in a high RF bandwidth. The simulated MOM capacitance matching is at a 10bit level, therefore two samplers are added with a binary weighted sampling capacitance value of 2.5fF and 1.3fF. Hence a 10-bit multiplier is realized. The total sampling capacitor is $256 \cdot 5\text{fF} = 1.3\text{pF}$. The switches are driven by inverters and the input signal DC level is set at 0 Volts to increase the switch overdrive voltage. All sampling switches are driven by one single inverter to eliminate timing mismatch between the sampler slices.

At a 20GS/s sampling speed, the switched capacitor input impedance is roughly equal to 50Ω . Hence, the settling constant normalized to $T_{on}(=1/f_S)$ equals $T_{on}/(R_S \cdot C_S) = 1/(20\text{GHz} \cdot 50\Omega \cdot 1.3\text{pF}) = 0.7$ where R_S equals the 50Ω source impedance and neglecting the switch resistance. Incomplete settling means that the sampling pulse is widened compared to the ideal delta pulse resulting in a first-order sinc-shaped response in the frequency domain which suppresses the aliases before sampling. Two times oversampling leaves some frequency space for more anti-alias filtering. Moreover, the sinc filter does not affect the RF signal much at $f_S/4$. This technique offers flexibility in RX-frequency but does not provide narrow channel filtering at RF.

To increase the sampling speed to 20GS/s and allow for various clock-phases — reset, sampling, and mixing — four time-interleaved samplers running at 5GS/s are implemented. As a side effect of interleaving, the readout of the LUT can also be clocked at 5GHz. Figure 3 shows the schematic of the implemented digital mixer.

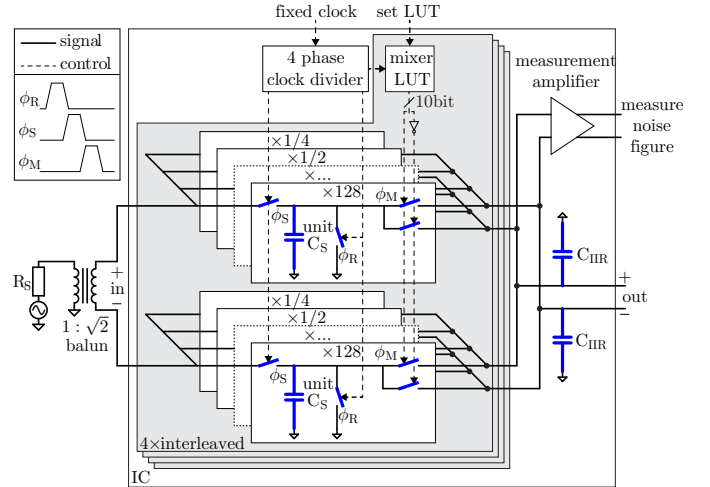


Fig. 3. Implementation of the switched capacitor discrete time mixer.

The output voltage created during the mixing clock phase (ϕ_M) is filtered by charge-sharing between the sampling capacitor and a large capacitor ($C_{IIR}=30\text{pF}$, Figure 3), creating a first order IIR filter. Additional filtering may be added.

All internal parasitic capacitances will add to either the sample capacitor (C_S) or to the baseband filter capacitor (C_{IIR}). Hence the input frequency of this architecture is only limited by the parasitic capacitance at the RF node and the used CMOS technology node will limit the clock speed. All signals can be considered “in-band” because of the broadband

sampler and hence a highly linear passive switched capacitor implementation is desirable.

The linearity and the noise figure are both determined by the sampler. Since the sampler has to provide a 50Ω input impedance, the noise figure after sampling is 3dB. Due to the passive nature of the mixer, the mixer loss will be equal to the mixer noise figure. The mixer conversion gain will be -6dB for a passive implementation: $A_{in} \cdot \sin(2\pi f_{in}t) \cdot \sin(2\pi f_M t) = 0.5 \cdot A_{in} \cdot \sin(2\pi [f_{in} \pm f_M]t)$. Hence a Double Side-Band (DSB) noise figure of 9dB is expected. According to simulations, the kT/C noise added by the IIR filter adds roughly 1dB to the noise figure. Note that the mixer noise figure is not a fundamental limit inherent to this architecture since a gain stage can be added between the sampler and the mixer.

The proposed receiver can be implemented twice to generate I and Q signals for image rejection at the cost of doubling the power consumption. However, we decided to leverage the flexibility of the receiver to shift to another IF and hence another image channel once a strong image occurs. In this way, an image avoiding rather than an image rejection strategy is used while simplifying the hardware (no I/Q needed).

III. MEASUREMENT RESULTS

A 28nm CMOS IC is designed and fabricated (see Figure 4). All measurements are performed at 20GS/s.

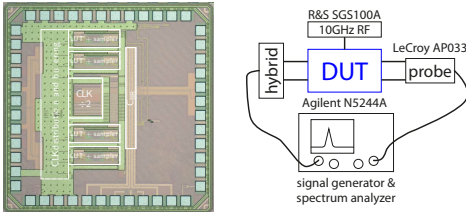


Fig. 4. Photo of the $1\text{mm} \times 1\text{mm}$ IC with 0.45mm^2 active area (left) and measurement setup for measuring spurious responses (right).

A. Spurious responses

To measure the spurious responses, a -30dBm (well below compression) input tone is swept from 0 to 10GHz ($f_S/2$). See the measurement setup in Figure 4. The conversion gain to a constant 25MHz IF is measured. Note that this is similar to measuring the harmonic rejection of a harmonic rejection mixer except that in our case the responses are not harmonics of the LO frequency hence the term *spurious responses* is used. The mixer frequency is set to $f_M = f_S \cdot 7/128 \approx 1\text{GHz}$, meaning that exactly seven sinusoidal periods are written to the mixer LUT of size 128. Figure 5 shows the measured relative spurious responses. All measurement results are obtained without calibration of the capacitor weighting.

Two kind of spurious responses are distinguished: those caused by quantization and those caused by interleaving. Quantization errors are repeated every 128 (LUT size) clock periods hence creating spurious responses at $f_{in} = f_S \cdot n/128$ (where n is an integer). Due to the four interleaved samplers, interleaving errors are repeated every four clock periods hence creating spurious responses at $f_{in} = f_S \cdot n/4 \pm f_M$ (where n is an integer). The sampler is followed by a discrete time

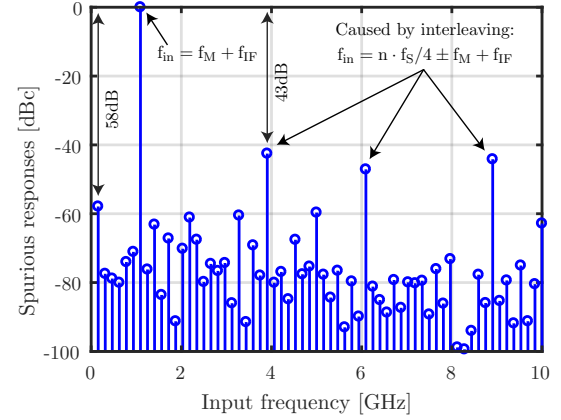


Fig. 5. Measured normalized spurious responses by sweeping the input frequency from 0 to 10GHz at a fixed $f_M \approx 1\text{GHz}$ and at a constant 25MHz IF.

mixer; therefore, the spurious responses caused by interleaving are shifted by f_M . The highest measured spurious response is at -43dBc and is caused by interleaving errors, while the highest spurious response caused by quantization is at -58dBc. The quantization level of -58dBc is expected from a 10-bit quantizer.

The interleaving error could both be caused by gain errors between the interleaved samplers and timing errors between the sampling moments. The gain errors are measured and used in simulation, resulting in spurious responses $> 9\text{dB}$ less than the measured spurious responses caused by interleaving. It is concluded that the spurious responses due to interleaving are not caused by gain errors but are caused by timing errors.

Simulations show that timing errors in the sampling moments of 1ps already cause spurious responses at roughly -40dBc. The timing errors have been minimized as much as possible by careful layout. A timing error will translate into a frequency dependent gain error. Gain errors can be compensated for by changing the LO-samples (α) in the LUT. Hence it is possible to reduce one spurious response caused by interleaving by adding gain compensation to the LO-samples stored in the LUT. This has been verified through simulations, showing that the spurious response caused by interleaving reduces to below -60dBc.

The spurious responses are measured for 25 mixer frequencies between 1.1GHz and 4.9GHz for eight ICs. The mixer frequencies are set to: $f_M = f_S \cdot k/128$ where k is an integer between 7 and 31. Figure 6 shows the measured strongest spurious response (caused by interleaving) and strongest spurious response caused by quantization versus mixer frequency f_M .

The spurious responses show larger deviations at exactly 2.5GHz, since only three sine coefficients are used. Therefore the quantization errors are far from random resulting in larger deviations across samples. Also, at $f_M = f_S \cdot 24/128 = f_S \cdot 3/16$, slightly higher deviations across the ICs are visible because there are fewer sine-coefficients. The ICs need a certain minimum supply voltage to deliver functionally correct behavior at the full 20GS/s sampling rate; two of the eight measured ICs required a 30mV higher than nominal supply voltage (higher supply voltage increases the speed of digital

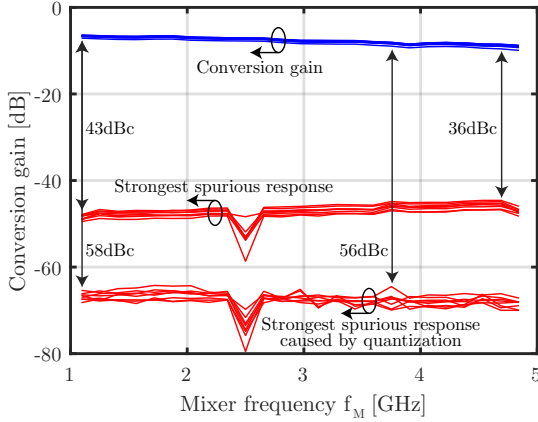


Fig. 6. Strongest spurious response (caused by interleaving) and strongest spurious response caused by quantization versus mixer frequency (f_M) measured at a constant 25MHz IF (measured for 8 ICs).

circuits). Decreasing the supply voltage increased the spur levels significantly. However, increasing the power supply voltage further does not reduce the spurious responses.

B. General receiver performance

Conversion gain (including impedance matching imperfections), noise figure (single sideband), IIP3 (in-band), and P1dB are measured versus mixer frequency f_M and are all shown in Figure 7. The S11 is measured versus input frequency f_{in} and shown in the same figure (the increase of S11 at 2.5GHz is most likely caused by packaging parasitics). All measurements are performed at $f_s = 20\text{GS/s}$ and the SC21, NF, IM3 ($\Delta f = 1\text{MHz}$), and P1dB are measured at a constant 25MHz IF. The single-side-band noise figure is reported since there are no I and Q channels implemented. An on-chip measurement amplifier is used to be able to measure the noise figure (which is not included in the power consumption). Both the measured noise figure and conversion loss are 1dB worse than calculated in Section II-B.

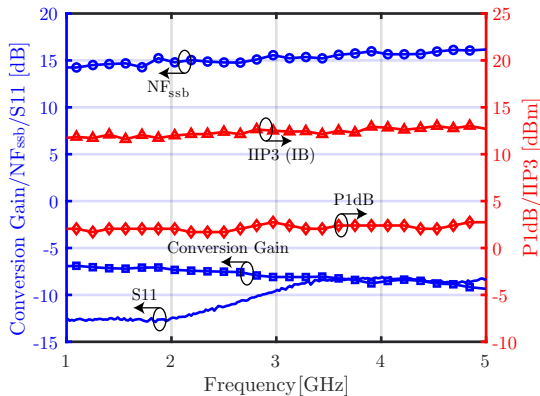


Fig. 7. Receiver performance for various mixer frequencies measured at a constant 25MHz IF. And the S11 measured versus input frequency.

The measured power consumption is 135mW for a 0.9V power supply ($f_s = 20\text{GS/s}$) and is independent of the mixer frequency f_M . Only dynamic power is dissipated (drivers to switches, clock divider and readout of LUT) which is proportional to the sampling frequency and reduces by technology scaling.

IV. CONCLUSIONS

Comparing the proposed receiver to those proposed in other papers that use one single clock frequency shows that a 5x greater RF input range is achieved. Moreover, spurious responses (caused by quantization) as low as -56dBc are achieved due to the good linearity and matching properties of capacitors. This is 13dB better than in previous work benchmarked in Table I. Timing errors in the clock signal result in interleaving spurious responses at -36dBc at 20GS/s (see Table I). Note that other publications [2], [3] already show a 10dB gain drop at 1GHz whereas our design shows only 2dB drop in gain at a frequency as high as 4.9GHz.

TABLE I
COMPARISON TABLE WITH OTHER ARCHITECTURES USING ONE SINGLE FIXED SYSTEM CLOCK.

	[2]	[3]	This work
Category	Trans conductor	Resistor	Switch capacitor
Technology	28nm FDSOI	65nm bulk	28nm bulk
Clock/sample freq. [GHz]	2	2	20
RF [GHz]	0.1 – 1	0 – 1	0.1 – 4.9
Worst case spur [dBc]	-41	-24	-43 – -36¹ -58 – -56²
Control bits	8bit	10bit	10bit
IIP3 [dBm]	+2 (IB) +16 (OOB)	>+31 (OOB)	+12 (IB)
P1dB [dBm]	-	-	+2
Conversion gain [dB]	33 – 23	-2 – -12	-7 – -9
NF [dB]	7 – 13	26	14 – 16³
Power [mW]	19	8	135 (@20GS/s)

¹Worst case spur caused by interleaving ($4 \times 5\text{GS/s}$) across 8 samples

²Worst case spur caused by quantization across 8 samples

³Single side-band NF since I/Q is not implemented

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REFERENCES

- [1] J. van Sinderen *et al.*, "A wideband single-PLL RF receiver for simultaneous multi-band and multi-channel digital car Radio reception," *IEEE Radio Frequency Integrated Circuits Symp.*, May 2016, pp. 330-333.
- [2] R. Kasri, E. Klumperink, P. Cathelin, E. Toumier and B. Nauta, "A digital sine-weighted switched-Gm mixer for single-clock power-scalable parallel receivers," *IEEE CICC*, April 2017, pp. 1-4.
- [3] N. Sinha, M. Rachid, S. Pavan and S. Pamarti, "Design and Analysis of an 8 mW, 1 GHz Span, Passive Spectrum Scanner With >+31 dBm Out-of-Band IIP3 Using Periodically Time-Varying Circuit Components," *IEEE JSSC*, Aug 2017, pp. 2009-2025.
- [4] Z. Ru, E. A. M. Klumperink and B. Nauta, "Discrete-Time Mixing Receiver Architecture for RF-Sampling Software-Defined Radio," *IEEE JSSC*, Sept 2010, pp. 1732-1745.
- [5] V. J. Arkesteijn, E. A. M. Klumperink and B. Nauta, "Jitter requirements of the sampling clock in software radio receivers," *IEEE TCAS II*, Feb 2006, pp. 90-94.
- [6] V. Syrjälä, V. Lehtinen and M. Valkama, "Sampling jitter in charge sampling radio," *IEEE WCNCW*, April 2012, pp. 59-63.