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Low temperature silicidation of Pd layers on crystalline silicon monitored via *in situ* resistance measurements

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ABSTRACT

Metal-silicon contacts may degrade during (SOI) wafer processing at unknown, high temperature conditions such as caused by sputtering or etching. We observed this phenomenon for Pd contacts on SOI wafers. Silicide formation of Pd contacts on crystalline silicon has therefore been investigated for low temperatures (57 – 135° C). We present an elegant measurement technique for monitoring the silicide formation process using *in situ* four point resistance measurements. From this the Pd₂Si thickness was determined via a resistance model. The results obtained via this simple measurement technique showed that silicide formation of Pd contacts on Si occurs already at 57° C, which is a temperature easily reached during metal sputtering onto thin SOI wafers. Furthermore, below approximately 100° C our results indicated that apart from Pd₂Si formation also mixed layers of Pd in Si and vice versa exist whereas at higher temperatures these mixed layers are absent or not significantly present.

In addition, we consider this measurement technique as an elegant, universally applicable method for monitoring silicide formation of metal-silicon contacts.

INTRODUCTION

Palladium is of interest as a high work function (5.12eV [1]) metal to form good contacts to p-type silicon. Pd on Si, however, is known to form Pd₂Si at temperatures even below 200° C [2,3]. Silicide formation at such low temperatures should be taken into account when devices are processed under conditions with unknown temperature, such as sputtering. As long as good thermal conducting bulk materials are used (such as silicon wafers of several hundred micrometer thickness), the heat transport to the bulk is sufficient to prevent excessive heating at the interface of Si and the deposited Pd. Silicon On Insulator (SOI) technology [4], has opened the way to new experimental silicon devices with nanoscale dimensions such as Multi-gate transistors and FinFETs [5]. During the sputter deposition of Pd layers on SOI wafers, however, the actual temperature at the Si-Pd interface can easily lead to silicide formation due to poor heat transport through the thin Si and the underlying poor thermal conducting SiO₂ layer. This effect is illustrated in Figure 1.

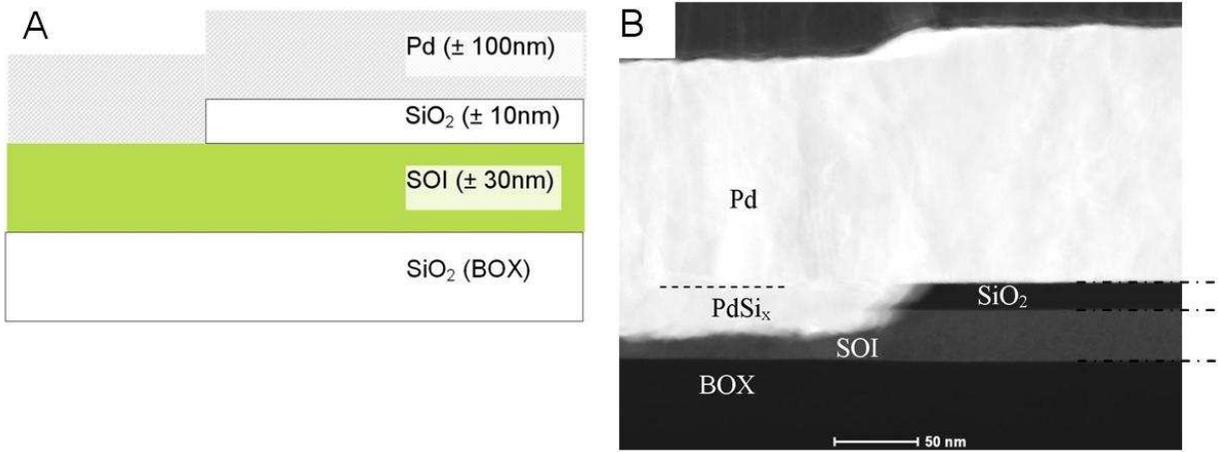


Figure 1. Schematic drawing of a SOI device with Pd contact (A) and High Angle Annular Dark Field (HAADF) Transmission Electron Microscopy (TEM) picture of the resulting device (B). The device consisted of a 100nm of Pd layer sputtered on a SOI wafer with 30nm of silicon.

In Figure 1B it can be seen that palladium has reacted with a large part of the silicon (SOI) into either a mixture of Pd and Si or Pd₂Si as was determined using an Energy Dispersive X-ray (EDX) detector.

Above findings resulted in this study in which we have focused on the low temperature (< 150° C) reactions of Pd layers on Si. This was done via *in situ* four point resistance measurements. From this the Pd₂Si thickness was determined via a simple resistance model as outlined below.

THEORY

The reaction of metallic Pd layers with bulk Si has been extensively studied. Below approximately 800° C only one stable phase is formed, namely Pd₂Si. The formation of this silicide follows diffusion limited kinetics [6]. The formed layer thickness of the silicide d_{Pd_2Si} grows according to the Arrhenius equation (1):

$$d_{Pd_2Si}^2 = D_0 t e^{-E_A/kT} \quad (1)$$

where D_0 [m^2s^{-1}] is the diffusivity pre-exponential term, t [s] is the time, E_A [eV] is the activation energy, k [$eV \cdot K^{-1}$] is Boltzmann constant and T [K] the temperature. Values for the activation energy vary between 0.9 – 1.5 eV [3,7]. Most studies in literature calculated the Pd₂Si thickness via backscattering techniques [7-9] or X-ray Diffraction [2,3]. In this study we determined the Pd₂Si thickness via in-situ resistance measurements. The basis for the calculation of d_{Pd_2Si} is a three layer resistive model of the samples in the form of a stack of Pd, Pd₂Si and Si. The resistances of these individual layers are in parallel and this gives for the total measured sheet resistance:

$$\frac{1}{R_{sheet,meas}} = \frac{d_{Pd}}{\rho_{Pd}} + \frac{d_{Pd_2Si}}{\rho_{Pd_2Si}} + \frac{d_{Si}}{\rho_{Si}} \quad (2)$$

Where d is the thickness of the layer and ρ the resistivity of the layer. d_{Si} and ρ_{Si} are considered constant and insensitive to temperature in the investigated temperature range (50 – 225° C). The initial Pd layer thickness $d_{Pd,0}$ and the resulting Pd₂Si thickness $d_{Pd_2Si,\infty}$ after all Pd has been consumed have been determined using Rutherford Backscattering Spectroscopy (RBS). Subsequently, we have applied a simple linear relation between d_{Pd} and d_{Pd_2Si} according to:

$$d_{Pd} = d_{Pd,0} - \frac{d_{Pd,0}d_{Pd_2Si}}{d_{Pd_2Si,\infty}} \quad (3)$$

Finally, substituting equation (3) in (2) gives for d_{Pd_2Si} :

$$d_{Pd_2Si} = \frac{\frac{1}{R_{sheet,meas}} - \frac{d_{Pd,0}}{\rho_{Pd}(T)} - \frac{d_{Si}}{\rho_{Si}(T)}}{\frac{1}{\rho_{Pd_2Si}(T)} - \frac{d_{Pd,0}}{d_{Pd_2Si,\infty}\rho_{Pd}(T)}} \quad (4)$$

Here the resistivities have been compensated for temperature. The procedure used for temperature compensation is illustrated in Figure 2.

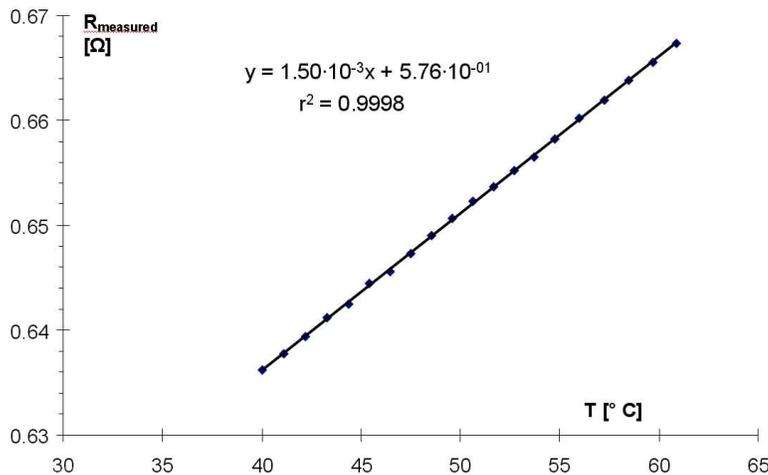


Figure 2. Measured resistance versus temperature for the heating up phase in the temperature range 40° - 60° C. The solid line shows the best linear fit ($r^2 = 0.9998$).

During the heating up phase the measured resistance increased linearly with temperature. It is assumed that during the relatively fast heating up no intermixing of Pd in Si or vice versa or the formation of silicide occurs. The resistance change is then solely due to the heating up of the

(unaffected) Pd layer and thus reflects the Temperature Coefficient of Resistance (TCR). The r^2 values for the linear fits were near unity for all samples and this supports our assumption. The parameters of the best linear fit have been used for calculating the resistivity of ρ_{Pd} as a function of temperature. A similar procedure was used for obtaining ρ_{Pd_2Si} as a function of temperature. This was derived using the resistance vs temperature data during the cooling down phase of completely silicidized samples.

EXPERIMENT

Silicon substrates (100 mm, p-type, $\langle 100 \rangle$, resistivity 5-10 Ωcm) were cleaned using standard cleaning. After a 1% HF dip, a layer of nominal 45 nm of Pd was sputter deposited at 500W at room temperature. Hereafter, samples were put in a vacuum oven and annealed at constant temperatures in the range of 57° - 135° C. In situ 4-point probe resistance measurements were performed during these thermal treatments. Additionally, samples were analyzed using X-ray Diffraction (XRD) and RBS.

DISCUSSION

The normalized resistance measurements at constant temperature are shown in Figure 3.

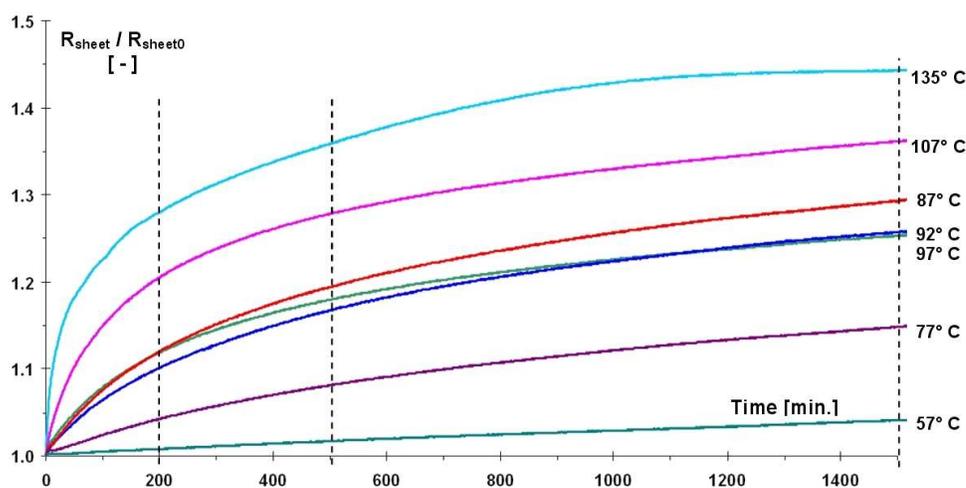


Figure 3. Relative resistance change (R_{sheet} / R_{sheet0} at $t = 0$) vs time for temperatures in the range 57° - 135° C.

The measured resistance increases in time, even at a temperature as low as 57° C. This is attributed to the formation of a higher resistance Pd_2Si layer at the cost of the lower resistance Pd layer. We also evaluated the room temperature resistance change during a measurement of 20,000 minutes (app. 14 days). Although we observed a change over time it was hardly visible on this timescale. After 20,000 minutes the change was 2.3% and after 1500 minutes it was less than 0.2% as compared to R_{sheet0} , respectively. The latter would not be visible in Figure 3. Therefore the error due to a room temperature resistance change was neglected and the samples were regarded to be stable during storage prior to measurements.

The trend in Figure 3 shows a discrepancy between 80 – 100° C. In general an increase in resistance change is observed with increasing temperature. For the measurements at 87, 92 and 97° C, however, we see a decrease in resistance change with increasing temperature. This effect is clearly observed in Figure 4, where the resistance increase as a function of temperature is shown after 200, 500, and 1500 minutes. This deviation at 87° and 92° C is still under investigation in our group.

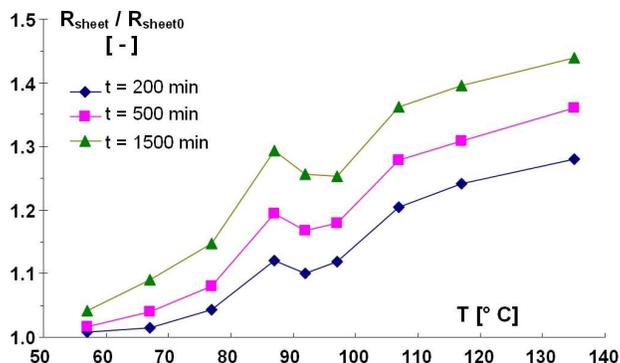


Figure 4. Relative resistance change ($R_{\text{sheet}} / R_{\text{sheet}}$ at $t = 0$) vs isothermal temperature for three different times.

Apart from the anomaly mentioned above, a trend towards higher resistance for higher temperature/ longer time is observed: At first approximation there is a transition towards a smaller derivative for temperatures higher than 100° C: The change in resistance seems to level off or increases not as severe as a function of temperature as compared to the lower temperatures.

Both Pd and Si are assumed to be diffusion species during the Pd₂Si formation [10]. An explanation for the observed phenomenon is that for lower temperatures mixed layers of Pd and Si may exist via diffusion of Pd into Si and vice versa without the formation (or next to partial formation) of Pd₂Si. This process would also result in a resistance change just like the sole formation of Pd₂Si from Pd and Si. Our simple model so far is not capable of distinguishing between the two processes (mixing and silicide formation). The data is therefore further investigated and complemented with XRD and RBS.

XRD and RBS analysis

Figure 5 shows the XRD diagram from samples isothermally heated at temperatures from 57° - 107° C. Also shown is a reference sample with an as deposited Pd layer.

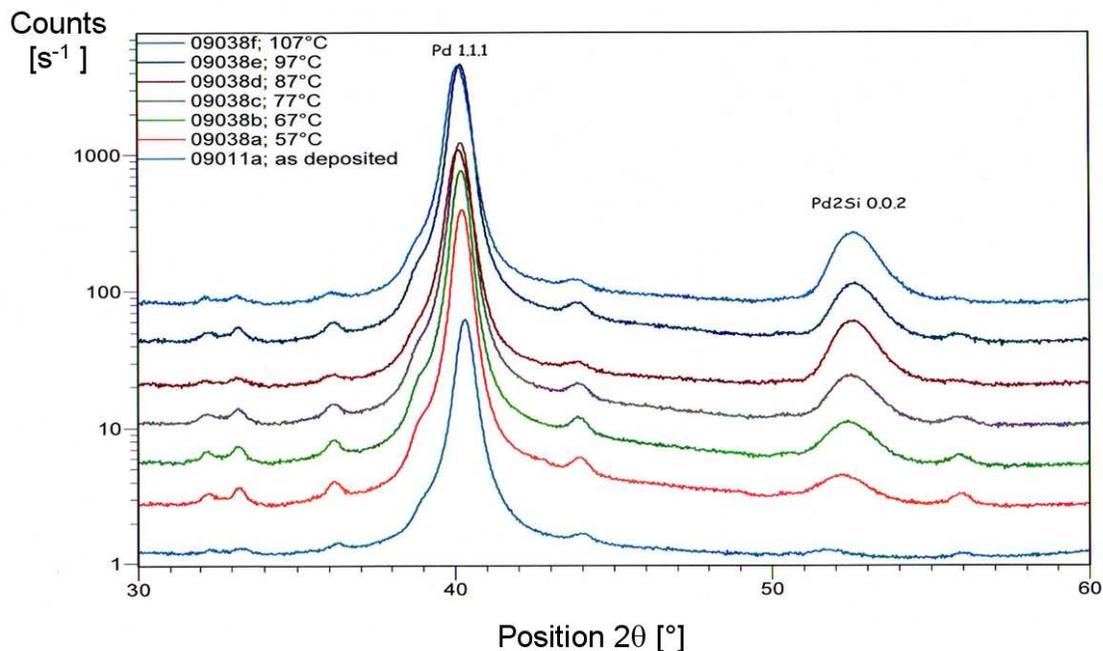


Figure 5. XRD diagram of a reference “as deposited” sample and six samples with isothermal anneal at temperatures between 57 – 107° C. Scans have been shifted vertically to make comparison easier. The other peaks next to Pd(111) and Pd₂Si(002) are all caused by spectral impurities because no monochromator was used.

For the reference samples the Pd peak was clearly visible but the Pd₂Si peak was hardly visible as compared to the annealed samples. For the other six annealed samples both Pd and Pd₂Si are present. Therefore, we conclude that the appearance of the Pd₂Si peak was due to the annealing step and was not present prior to measurement. In general the Pd peak becomes smaller and the Pd₂Si peak becomes larger at higher temperatures. In addition, the Pd₂Si peak shifts to the right because the unit cell becomes smaller. This is probably caused by a slight decrease in the Si content of this phase. XRD indicates that even at 57° C Pd₂Si is formed. However, XRD analysis does not provide information on the presence of mixed layers of Pd in Si.

RBS analyses of the samples (not shown here) reveal a gradient in the Pd and the Si profile over several nanometers, ranging from PdSi_{0.3} (at the Pd side) up to PdSi₄ (at the Si side). This indicates that for these samples besides Pd₂Si also mixed layers are present.

Arrhenius plots

From the resistance measurements and using equation 4 the formed Pd₂Si layer thickness was calculated. The activation energy was determined using equation 1. Figure 6 shows the Arrhenius plot for the temperature range of 57-135° C.

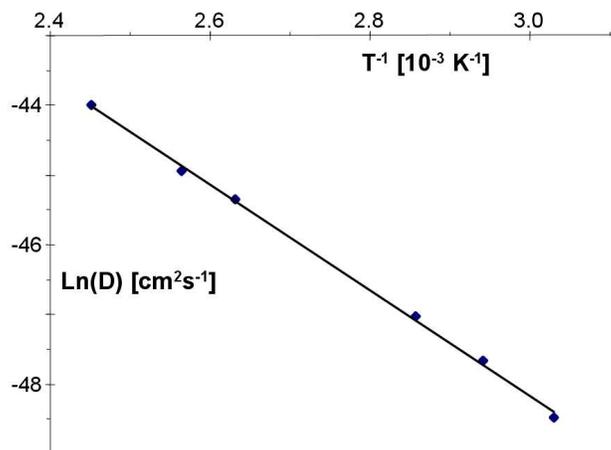


Figure 6. Arrhenius plot of the data for 45 nm Pd samples for temperatures in the range 57 – 135° C. Data points for 87, 92, and 97° C have been omitted. The solid line shows the best linear fit.

A good linear fit was obtained using our resistive model. The resulting activation energy E_A of the data of figure 6 is 0.7 ± 0.1 eV. This is somewhat lower than the data in literature that vary between 0.9 – 1.5 eV [7]. Those data, however, were in most cases determined at temperatures above 150° C. Therefore, in order to compare our model with literature data, we also determined the activation energy from samples with approximately 150nm Pd on Si in the temperature range of 150-225° C. The Arrhenius plot hereof is depicted in figure 7.

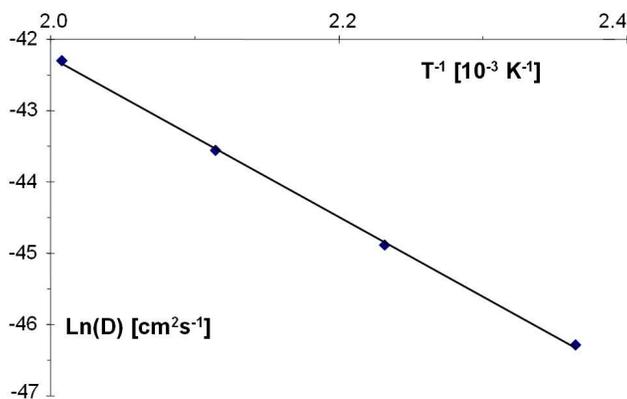


Figure 7. Arrhenius plot of the data from 150 nm Pd on Si for temperatures in the range 150 – 225° C. The solid line shows the best linear fit.

Again a good, linear fit was obtained. From this data an activation energy was derived of $E_A = 1.0 \pm 0.1$ eV, which is in good agreement with literature [7]. To explain the observed discrepancy in found values for E_A for the high and the low temperature range we propose a difference in layer structures of the samples for high ($> 150^\circ C$) and low ($< 150^\circ C$) temperatures. At high temperatures the diffusing Pd and Si species react instantaneously to Pd_2Si without substantial formation of intermixed layers of Pd and Si. For low temperatures besides Pd_2Si (as shown via XRD) a substantial amount of intermixed (but no silicide) layers may be formed which also result in an increase in measured resistance. In our resistive model these mixed layers are not taken into account. They are assumed to behave like Pd_2Si . This can eventually lead to an error

in the derived activation energy. Currently, we try to extend our electrical model to fit the resistance measurements not only to Pd₂Si formation, but also to include the Pd rich and Si rich regions at the Si and Pd side.

CONCLUSIONS

Sputtered Pd layers on bare Si wafers have been examined on isothermal behavior in the low temperature range of 57° - 135° C. We used simple *in situ* four point probe resistance measurements during the thermal treatment (and silicide formation). The resistance data was analyzed using a simple three layer resistive model for deriving the silicide thickness. The silicide growth rate and the activation energy were determined. This method is relatively simple compared to commonly used XRD and RBS measurements.

So far this study has shown that Pd layers on Si are not stable even at temperatures as low as 57° C. XRD analysis revealed the formation of a Pd₂Si phase, whereas RBS indicated that intermixed layers of Pd and Si exist in the temperature range below 100° C. The above findings are of crucial importance for metallic Pd contacts to Si on SOI wafers. During sputter deposition of Pd the heat transport is limited through the thin Si/SiO₂ stack. Significant heating and substantial Pd₂Si formation was observed, resulting in Pd-Si interfaces of ill-defined composition.

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