A Sub-mW All-Passive RF Front End with Implicit Capacitive Stacking Achieving 13 dB Gain, 5 dB NF and +25 dBm OOB-IIP3

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***Abstract*— This paper presents a sub-mW mixer-first RF front-end that exploits a novel capacitive stacking technique in an altered bottom-plate N-path filter/mixer to achieve passive voltage gain and high-linearity at low noise figure. Capacitive stacking is realized implicitly by reading out the voltage from the bottom-plate of N-path capacitors instead of their top-plate, which provides a 2x gain at the read-out capacitors. Additional passive voltage gain is achieved using impedance upconversion while improving the out-of-band linearity performance of small switches. With no other active circuitry, only clock generation circuits determine the total power consumption of this RF front-end. A prototype is fabricated in GF22 nm FDSOI technology. Operating at f_{LO}= 1 GHz, the prototype achieves a voltage gain of 13 dB, 5 dB Noise Figure and +25/+66 dBm Out-of-band IIP3/IIP2 at 160 MHz offset while consuming only 600 μW of power from a 0.8 V supply.**

***Keywords*— Passive mixer, N-path filter, mixer-first receiver, bottom-plate mixing, capacitive stacking, high linearity, low-power, RF front-ends.**

I. Introduction

Massive deployment of wireless sensor nodes and scarce available radio spectrum make the receivers in the sensor networks susceptible to interference problems. On top of the strict limits on cost and power consumption, the interference robustness is becoming a major concern for these radios. RF front-ends adopt techniques such as N-path filters/mixers, in which large switches and capacitors are used, to achieve high out-of-band linearity ($>$ 30 dBm) at the cost of power in the clock drivers [1]–[2]. Such front-ends exhibit low conversion loss and high input impedance at tunable switching frequency. Often, the N-path filters/mixers are cascaded with active blocks to provide impedance matching at RF input and IF gain at the desired operating frequency [1],[3]. These active blocks consume a lot of power to achieve low noise figure and high linearity [3],[2].

In this paper, we present a low power and highly linear all-passive RF front-end employing an altered bottom-plate N-path mixer and a passive matching network. The architecture, implementation and performance of the novel RF front-end is discussed in detail in the rest of the paper.

II. Architecture

Bottom-plate N-path filters achieve higher linearity compared to conventional top-plate N-path filters [2]. As shown in Fig.1a and Fig.1b, modulation of switch resistance due to input-dependent V_{GS} is reduced in the bottom-plate configuration by grounding the V_S node of the switch. Hence, it results in higher linearity. However, when the switch is

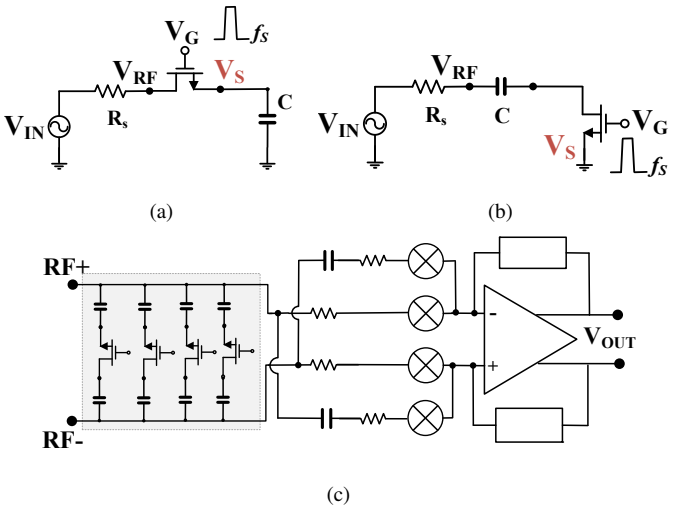

Fig. 1. (a) Top-plate N-path filter, (b) Bottom-plate N-path filter and, (c) Differential bottom-plate N-path and cross-coupled switch-RC front-end [2]

open, the capacitor becomes floating and stores the down-converted baseband voltage across its terminals (without being referenced to ground). As such, it complicates the possibility of extracting the baseband signal from the capacitor. Hence in [2], the bottom-plate configuration is simply used as bandpass filter and the RF voltage from the top-plate of the N-path capacitors is down-converted using a cross-coupled switch-RC network (Fig.1c). It achieves an out-of-band IIP3 of 44 dBm, which is 15-20 dB higher than the top-plate configuration.

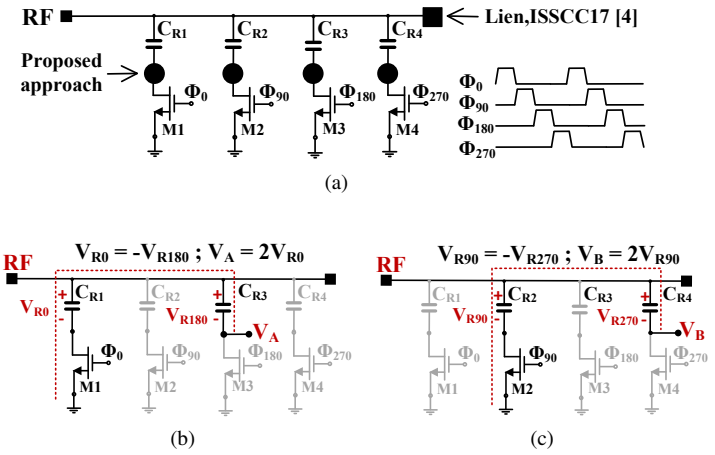

Fig. 2. (a) Proposed down-conversion technique in bottom-plate N-path filtering; Capacitive stacking (b) when M1 is conducting and (c) when M2 is conducting

Unlike [2], we propose to sense the voltage from the bottom-plate of the N-path capacitors in this work (Fig.2a). The resultant behavior can be explained as follows.

Consider a 4-path single-ended bottom-plate N-path filter in Fig.2a. Suppose that RF sinusoidal input f_{in}, is down-converted to baseband by clocks, ϕ_{0-270}, switching at frequency f_{LO}. Let the resulting down-converted baseband voltage across the mixing capacitors C_{R1}-C_{R4} be V_{R0}, V_{R90}, V_{R180} and V_{R270} respectively. For $f_{in} \approx f_{LO}$, the baseband voltages V_{R0} and V_{R180} are in anti-phase since the clock phases (ϕ_0, ϕ_{180}) driving their corresponding switches (M1,M3) are 180 degrees phase-shifted. Similarly V_{R90} and V_{R270} are in anti-phase. In simpler terms, the in-band instantaneous voltages can be expressed as,

$$\begin{aligned} V_{R0} &= -V_{R180} \\ V_{R90} &= -V_{R270} \end{aligned} \tag{1}$$

When switch M1 is conducting, the bottom-plate of the capacitor C_{R1} is connected to ground and other capacitors remain floating. When observed from node A in Fig. 2b, the capacitors C_{R3} and C_{R1} are connected in series to ground. In other words, capacitor C_{R1} and C_{R3} appears to be stacked upon each other. Therefore the resultant voltage at node A,

$$V_A = -V_{R180} + V_{R0} = 2 \times V_{R0} \tag{2}$$

Note that from node A the bottom-plate of the Capacitor C_{R3}, V_{R180} is seen inverted and hence the negative sign. Thus, a voltage gain of 2 is achieved for baseband signals by simply tapping them from the node A. Likewise, when switch M2 is closed, $V_B = 2 \times V_{R90}$ can be achieved by tapping the signal from node B, at the bottom-plate of the Capacitor C_{R4}, as shown in Fig. 2c. Similar voltage gain can be achieved by reading out the signal from the bottom-plate of capacitors C_{R2} and C_{R4} when switches M2 and M4 are closed respectively.

In a fully-differential implementation of the bottom-plate N-path filters, the balanced RF inputs RF+ and RF- are in anti-phase. Therefore, when a switch is closed, a zero voltage point occurs in the middle of the inversion region in the channel of the switching transistor. The zero-voltage point behaves similar to ground in the single-ended implementation and can be used for differential capacitor stacking. The implicit capacitor stacking in differential bottom-plate N-path filters can be realized as shown in Fig. 3. Here, the additional read-out capacitors C_{B1} and C_{B2} are used to read-out the 2×BB signal from the bottom-plate of capacitors C_{R3} and C_{R7} when M1 is closed (Fig.3a). Additionally, they can be re-used to read-out the signal from the bottom-plate of capacitors C_{R5} and C_{R1} when M3 is closed (Fig.3b). Such capacitor re-use is possible due to differential RF inputs and 180 degrees phase shifted clocks driving the switches. Since the read-out capacitors share the charges with two N-path capacitors at different time instants, an additional order of infinite impulse response filtering is achieved in this scenario.

Further, to achieve the desired input matching and more voltage gain, we propose to use passive matching network instead of power-hungry active blocks [4],[5],[6]. The loss

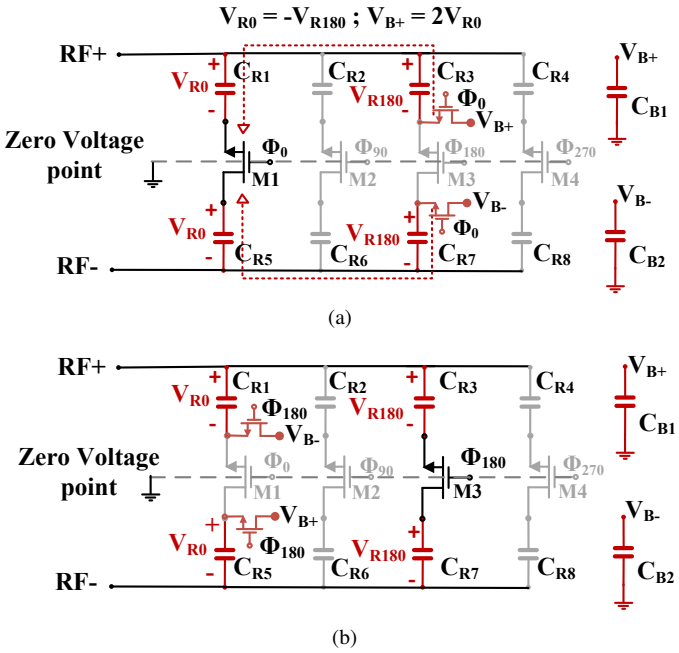

Fig. 3. (a) Capacitive stacking in the fully-differential proposed RF front-end and (b) read-out capacitors reuse.

due to the parasitic substrate capacitance of N-path capacitors and charge sharing behavior of read-out capacitors together determine the impedance to be matched and the achievable voltage gain and bandwidth.

III. Circuit Implementation

The circuit schematic of the proposed RF front-end is shown in Fig. 4. The core of the RF front-end is composed of fully differential bottom-plate N-path filters implemented together with the proposed read-out technique. RF mixing and IF read-out capacitors are chosen to be 6.4 pF and 4 pF respectively to achieve an IF bandwidth of 15 MHz and desired impedance matching at 1 GHz.

Passive mixer switches are sized to provide a differential resistance of 30 Ω. This is a trade-off between power consumption of the clock drivers and maximum achievable linearity. As shown in Fig. 4, additional switches are used to set the common-mode bias voltage, V_C of the mixer and sampling switches via an external supply.

All the switches are driven by 4-phase non-overlapping 25% duty-cycle clocks provided by divide-by-2 circuit. GF22 nm FDSOI CMOS process uses SiGe channel in PMOS transistors to achieve a driving capability similar to that of NMOS transistors. Hence the input capacitance of the digital circuits are significantly reduced. When compared to other CMOS processes with Si channel in MOSFETs, where PMOS transistors are often 2-3x larger than NMOS for similar driving capability, almost 2x higher speed and lower power consumption is achieved in the digital implementation.

IV. Measurement Results

An experimental prototype is fabricated in 22 nm FDSOI CMOS process and a QFN40 package is used. The chip photo

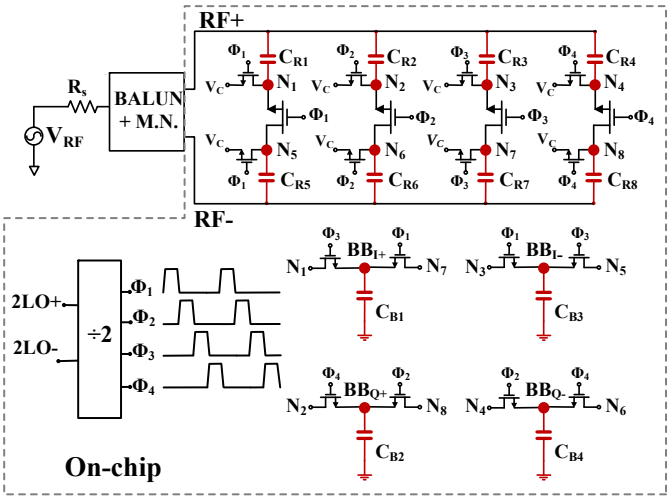

Fig. 4. Complete architecture of the implemented RF front-end

is shown in Fig. 5a and the active area is $0.65 \times 0.35\,\text{mm}^2$. To be able to experiment with multiple impedance up-conversion ratios, off-chip transformers are used as matching network and as balun simultaneously. For all the reported measurements below, a Minicircuits TC4-14X+ transformer with an impedance up-conversion ratio of 1 : 4 is used. The prototype operates in the frequency range of 0.6 - 1.3 GHz (Fig. 5b). At a switching frequency of 1 GHz, the dividers and clock drivers in the front-end consume 600 μW of power from a 0.8 V supply.

Figure 5b and Figure 5c show that the front-end achieves a small-signal conversion gain of 13 - 14 dB, an IF bandwidth of 16 MHz, and a minimum double-sided NF of 5 - 6 dB. The parasitic substrate capacitance of the RF capacitors provides low-pass filtering at the RF terminals. Such passive filtering limits the bandwidth and attenuates the input signal. Together with limited transformer bandwidth, it degrades the NF of the front-end by $\sim$3 dB at higher RF frequency [2]. It also shifts the S11 minima to left in accordance with the LPF phase response [1].

The measured IIP3 and IIP2 performance versus frequency offset of the interferers from the f_{LO} is shown in Fig. 6a. The offset frequency of the two-tone interferers are swept while keeping the resulting IM3 or IM2 product at a baseband frequency of 5 MHz. With no active circuit elements, the proposed RF front-end achieves an in-band IIP3 of +10 dBm. As the frequency offset increases, IIP3/IIP2 increases due to N-path filtering. The front-end achieves a maximum out-of-band IIP3 of +25 dBm and IIP2 of +66 dBm at an offset of 160 MHz (10x BW).

Large signal performance of the RF front-end is evaluated by measuring the in-band 1 dB compression point (CP1dB) and out-of-band blocker 1 dB compression point (B1dB). Figure 6a shows the B1dB compression point versus blocker frequency offset normalized to bandwidth. For a blocker located at 80 MHz offset (5x BW), the proposed work achieves -1 dBm B1dB compression point. As shown in Fig. 6b, the front-end achieves a large in-band compression point (CP1dB) of -7.5 dBm thanks to no active circuitry.

As shown in Fig. 6c, LO leakage at the RF port was measured for 4 different samples. We see that the proposed RF front-end achieves < -70 dBm LO leakage across the operating LO frequency range. At $f_{LO} = 1$ GHz, it exhibits < -80 dBm LO leakage.

The performance summary of the proposed RF front-end and the comparison with other state-of-the-art mixer-first front-ends is shown in Table 1. From the table, it is evident that this work achieves comparable out-of-band linearity performance while consuming 10x - 20x lower power than several high-performance mixer-first front-ends.

Strikingly, when compared to other sub-mW RF front-ends in Table 2, the proposed work shows $\sim$ 20 dB improvement in the out-of-band IIP3 performance while exhibiting low noise figure. Additional baseband amplification is necessary to adopt this architecture in low-power RX. And, it would degrade the linearity performance of the proposed front-end. However, it should be noted that at out-of-band frequencies, this RF front-end provides more than 20 dB attenuation. Such attenuation minimizes the linearity degradation of the RX and facilitates competitive performance. Finally, additional attenuation can be achieved by using high-Q LC matching network instead of transformers.

V. Conclusion

This paper reports a proof of concept of implicit capacitive stacking in a bottom-plate N-path filter. Such capacitive stacking is achieved by reading-out the down-converted signal from the bottom-plate of N-path capacitors. It results in an inherent passive voltage conversion gain of 6 dB and facilitates low noise figure at the cost of additional capacitor area. Further, a passive matching network is employed to realise impedance matching, to achieve more voltage gain and high linearity with small mixer switches.

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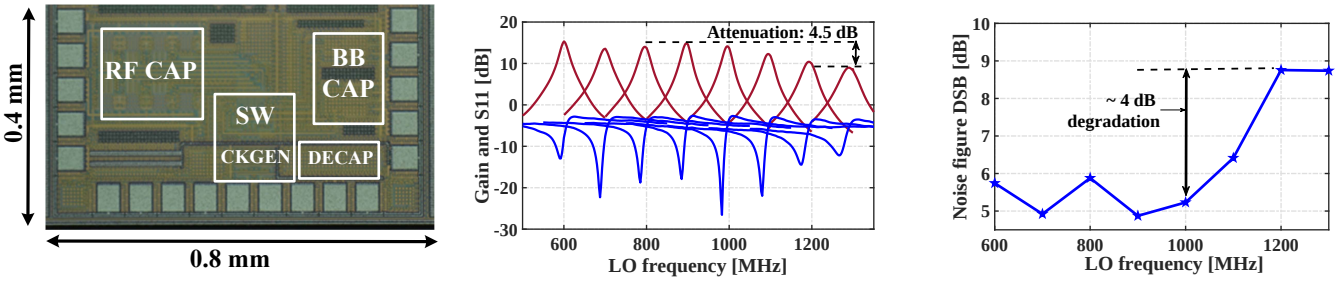
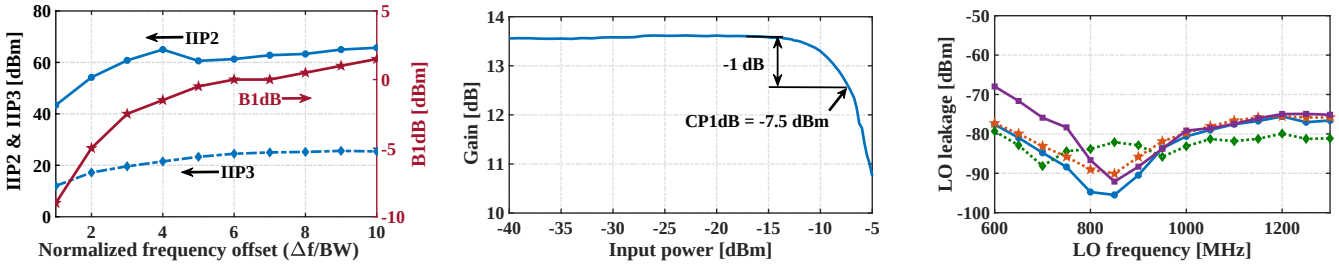


(a) (b) (c)

Fig. 5. (a) Die Micrograph and Small signal performance: (b) Conversion gain and S11 vs LO frequency; (c) DSB Noise figure vs LO frequency



(a) (b) (c)

Fig. 6. (a) Linearity performance: IIP3, IIP2 and B1dB (IF BW = 16 MHz); (b) Inband 1 dB Compression point and (c) LO leakage at RF port (measured for 4 different samples)

Table 1. Result summary and comparison with high-performance mixer-first receivers.

Features	**Andrews JSSC10**	**Nejdel RFIC15**	**Lin ISSCC15**	**Westerveld RFIC16**	**Lien RFIC17**	**This Work**
Technology	65 nm	65 nm	65 nm	65 nm	45 nm SOI	22 nm FDSOI
Frequency [GHz]	0.1 - 2.4	2 - 3	0.1 - 1.5	0.03 - 0.3	0.2 - 8	0.6 - 1.3
Power [mW]	37 - 70	27 - 75	11@1.5 GHz	46.1	50 + 30 mW/ GHz	0.6@1 GHz
Gain [dB]	40 - 70	7.5	38	21-36	21	13 - 14
IF BW [MHz]	10	10	2	2 - 40	10	16
DSB-NF [dB]	3 - 5	2.5 - 4.5	2.9	6	2.3 - 5.4	5 - 6 ($\leq$1 GHz)
OOB IIP3[dBm @ Δf/BW]	25 @ 10	26 @ 10	13 @ 15	41 @ 20	39 @ 8	25 @ 10
OOB IIP2[dBm @ Δf/BW]	56 @ 10	65 @ 10	47 @ 15	90 @ 20	88 @ 8	66 @ 10
LO leakage [dBm]	-65	-60	N.A.	N.A.	-65	$<$-70
Supply [V]	1.2/2.5	1.2	0.7/1.2	1.2	1.2	0.8
Active Area [mm^2]	0.75	0.23	0.028	0.8	0.8	0.23

Table 2. Comparison with low-power RF front-ends.

Features	**Bryant RFIC12**	**Lin ISSCC14**	**Selvakumar JSSC15**	**Lee TMTT18**	**Krishnamurthy ESSCIRC18**	**This Work**
Technology	65 nm	65 nm	130 nm	28 nm	28 nm	22 nm FDSOI
Frequency [GHz]	2.45	0.43 - 0.96	2.4	2.4	2.4	0.6 - 1.3
Power [mW]	0.4	1.15	0.6	0.64	0.58	0.6@1 GHz
Gain [dB]	27.5	50	55.5	50	19	13 - 14
BW [MHz]	N.A.	N.A.	2	1	3.6	16
DSB-NF [dB]	9	8.1	15.1	6.5	11.9	5 - 6 ($\leq$1 GHz)
OOB IIP3[dBm @ Δf/BW]	-21 @ N.A.	-20.5 @ N.A.	-15.8 @ 2.5	0.9 @ 10	3.3 @ 13.9	25 @ 10
Supply [V]	0.8	0.5	0.8	0.8	1	0.8
Active Area [mm^2]	0.24	0.2	0.25	0.25	N.A.	0.23