

A 4MS/s 10b SAR ADC with integrated Class-A buffers in 65nm CMOS with near rail-to-rail input using a single 1.2V supply

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Abstract— We present a 10b differential SAR ADC integrated with unity gain (Class-A) voltage buffers, operating from a single supply voltage 1.2V and handling near rail-to-rail inputs. The two differential inputs are first compared and depending on the comparison result, the inputs are either swapped or not, after which these signals are buffered, sampled and converted. This way each of the two buffers needs to handle only half of the full-scale range which enables operation of the Class-A buffers at the ADC supply voltage while providing an overall near rail-to-rail (full-scale) input range for conversion. The buffered ADC can handle $2V_{P-P}$ differential input and consumes $149\mu\text{W}$ at 4MS/s to achieve a state-of-the-art Walden FoM of 87fJ/conversion-step including buffers. The buffered ADC was designed in a 65nm CMOS process and occupies an active area of 0.04mm^2 .

Keywords—SAR ADC; input buffer; Class-A driver; Nyquist sampling; SFDR; INL; DNL

I. INTRODUCTION

Most energy efficient SAR ADCs find application in low power IoT nodes, wherein the sensors usually have low output power drive capability and cannot drive the (relatively) large sample capacitor (C_S) of the ADC. SAR ADCs have a large (rail-to-rail) input range and thus a buffer circuit is required that can

handle near rail-to-rail signal swing for near Nyquist input frequencies [1]. As highlighted in [1-3], the energy consumption to drive an ADC is not represented in the Walden FoM used for benchmarking ADCs, it is seldom addressed and it presents a bottleneck in achieving an overall low energy consumption data acquisition system for interfacing with low power sensor nodes. The work in [1] addresses the problem of driving a SAR ADC and shields the large sample capacitor by driving it with a Class-A buffer that has a (relatively) small input capacitance. This came at the cost of both operating the buffer at a supply voltage which is 2x that of the ADC itself and using thick oxide current sources to alleviate reliability issues. Other techniques to handle rail-to-rail signal swings include charge-pumps [4] to extend the supply voltage beyond nominal rails and using a dual, complimentary input pair buffers (both PMOS and NMOS) [5]. The former has device reliability concerns because of exceeding the supply rail; the latter has signal dependent offset modulation leading to distortion.

We present a differential-input SAR ADC integrated with voltage buffers, powered at a single supply voltage level. Before buffering and sampling, the differential inputs (V_{INP}/V_{INN}) are compared with each other. Based on this

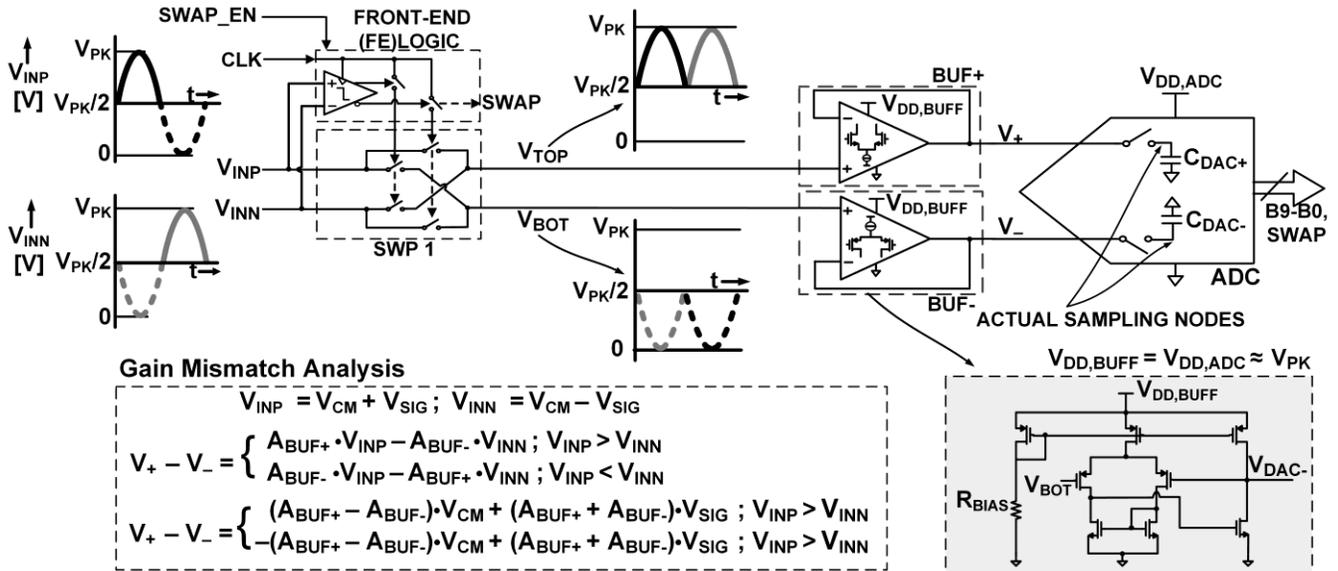


Fig.1 Block diagram of the SAR ADC integrated with unity gain buffers. All blocks operate at the same supply voltage. A_{BUF+} and A_{BUF-} (approximately equal to unity) represent respectively the gain of the buffers BUF+ and BUF-.

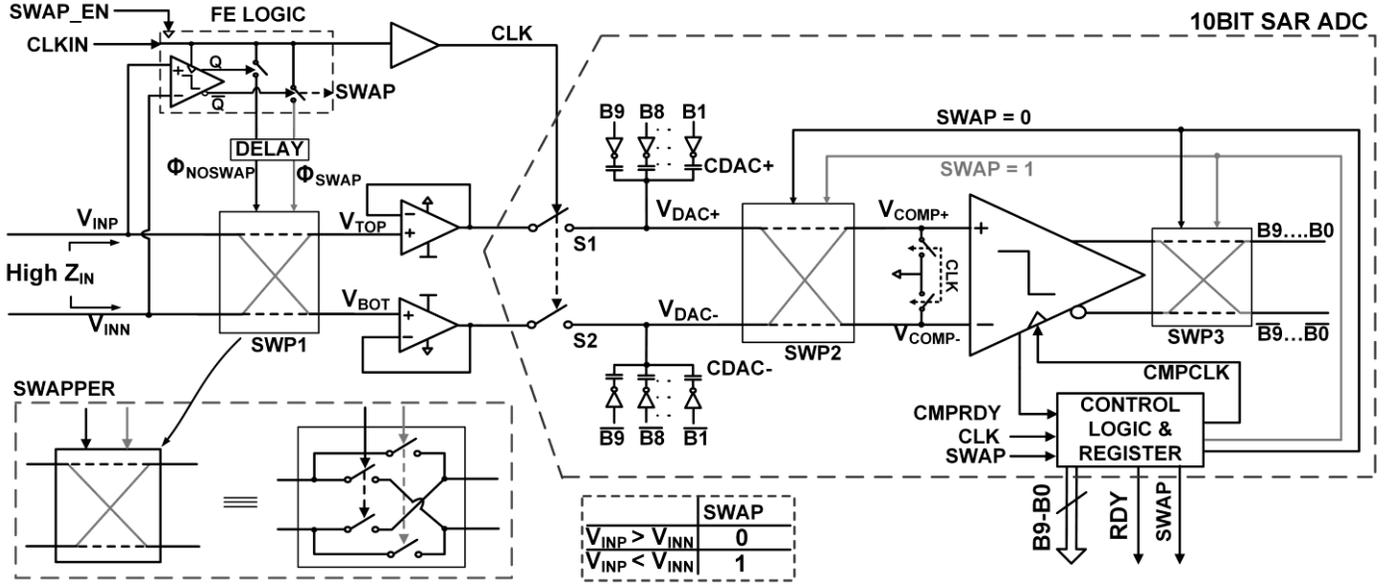


Fig. 2. Buffered SAR ADC architecture. Swappers SWP1, SWP2 and SWP3 route the signal paths depending on the sign of $(V_{INP} - V_{INN})$. SWP2 is disabled during sampling to isolate the main comparator from CDAC. Additional swapping by SWP2 brings the sampled V_{INP} and V_{INN} to always appear respectively at V_{COMP+} and V_{COMP-} for SAR conversion. Swap action performed by SWP3 keeps the SAR loop convergent.

comparison, the inputs are either routed straight or cross-connected to the two voltage buffers. This way, both buffers and respective DACs operate on only (about) one half of the full-scale input range (FSIR), without compromising the FSIR of the ADC. Conceptually, it has similarities with [3] where $2/3^{\text{rd}}$ and $1/3^{\text{rd}}$ of either differential input range was sampled on a specific differential DAC to reduce the maximum voltage change at the sampling capacitor throughout the Nyquist band by a factor 1.5x. The innovation presented in this paper is that the ADC includes (Class-A) buffers that operate either on the upper or on the lower half of the FSIR, enabling operation of both buffers at the ADC supply voltage while effectively buffering rail-to-rail input signals.

II. ARCHITECTURE

Fig.1 shows the block diagram of the SAR ADC with unity gain (voltage) buffers, BUF+ and BUF-. Noise and offset of the front-end (FE) comparator are of no concern, since its output is not used for the ADC conversion. Depending on the FE comparator output, SWP1 which consists of NMOS bootstrapped switches, either connects V_{INP}/V_{INN} straight to V_{TOP}/V_{BOT} or swap the signal paths to connect vice versa during sampling. The BUF+ and BUF- inputs receive signals that are respectively in the upper and lower half of the FSIR. Therefore, instead of conventionally having 2 single-ended buffers both handling the FSIR of the ADC, BUF+ and BUF- in this work only have to handle half the FSIR. BUF- consists of a PMOS differential pair first stage and an NMOS common-source second stage in unity gain arrangement. BUF+ is complementary to BUF- and uses an NMOS input differential pair. This is different from [5] where each of V_{INP} and V_{INN} is always connected to both PMOS and NMOS input stages thereby modulating the gain and offset with the signal amplitude, leading to distortion. As shown in Fig.1, gain

mismatch between BUF+ and BUF- results in the addition (or subtraction) of a small (\sim LSB level) voltage at the ADC input. The output of the FE comparator (SWAP bit) indicates whether this (offset) voltage is added or subtracted due to input swapping. Offset mismatch between the buffers also results in a similar addition (or subtraction). A straightforward correction can be applied to remove the effect of gain and offset mismatch from the output code using the SWAP bit data. The corrected output code is then identical to that of a conventional unbuffered differential SAR ADC.

Fig.2 shows the complete architecture of the proposed buffered SAR ADC. The actual sampling action is performed on CDAC+/- by NMOS bootstrapped switches (S1/S2) that are controlled by CLK. Note that SWP1 is disabled after the sampling phase. However its clock (Φ_{SWAP} or Φ_{NOSWAP}) is delayed wrt CLK to make sure that V_{INP}/V_{INN} are connected to the buffer inputs when CLK goes LOW at the end of sampling period. This prevents kT/C noise of the buffer's (small) input capacitance to be added to the sampled signal (V_{DAC+}/V_{DAC-}). The SAR ADC contains 2 swappers SWP2 and SWP3 which are turned OFF during tracking. SWP2 isolates CDAC+/- from the main comparator's inputs during sampling; these inputs are reset to ground to prevent ISI. Depending on whether SWAP = 0 or 1, SWP2 connects V_{DAC+}/V_{DAC-} respectively to V_{COMP+}/V_{COMP-} or vice versa for the SAR conversion. This additional swapping of the signal path cancels the comparator offset voltage inside the SAR loop (unlike in [3]) and avoids distortion caused by this. All timing signals for the swappers and the internal SAR conversion are generated asynchronously from a single external CLKIN. Both the FE comparator and the main comparator inside the SAR loop use a latch-type architecture similar to in [7]. The demands on noise performance and drive capabilities of the FE comparator are

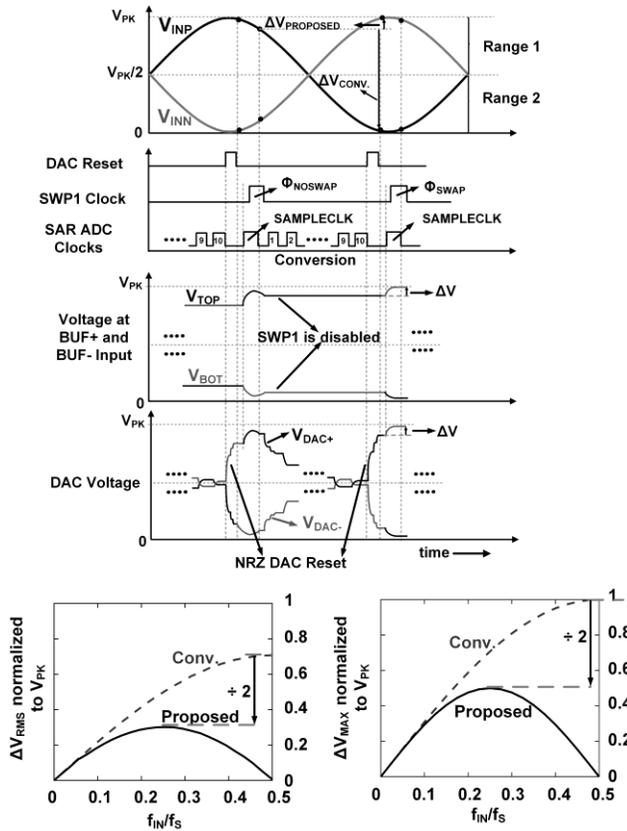


Fig. 3. Timing information along with change in voltage at the DAC nodes and input of the buffers for the buffered SAR ADC. Also shown are the (MATLAB) simulated RMS and maximum change in voltage at the input of the voltage buffers (and corresponding CDAC) for sample and hold operation, for the proposed and conventional sampling scheme.

much lower than those for the low noise main comparator. In our design this results in a faster regeneration (compared to the main comparator) and a much lower power consumption. Simulations show that the slope of the regeneration time constant of the FE comparator and the main comparator wrt change in input differential voltage is -40ps/decade and -200ps/decade respectively. The rate of metastability of the ADC for a given comparison time is therefore dominated by the main comparator's regeneration time constant. The FE comparator resolves a 1mV differential input in 0.5ns of clock to output delay. With a slope of -40ps/decade , an input differential voltage (1fV) can thus be regenerated within 1ns of comparison time.

The input capacitance of the buffer is $50\text{fF}/20\text{fF}$ respectively for $\text{BUF-}/\text{BUF+}$. This is $5\times$ lower than the single-ended DAC capacitance of 250fF (including parasitics). Fig.3 shows the timing information for near Nyquist inputs and change in voltage at the buffers input and at $C_{\text{DAC+}}/C_{\text{DAC-}}$. SWP1 is disabled during conversion and the buffer inputs ($V_{\text{TOP}}/V_{\text{BOT}}$) as well as its outputs hold the sampled signal. The non-return to zero DAC reset brings back the voltage to the previously sampled input voltage at the end of conversion. This reduces the maximum voltage change at the output of the buffers, thereby reducing the initial slewing for full-scale inputs. Fig.3 also

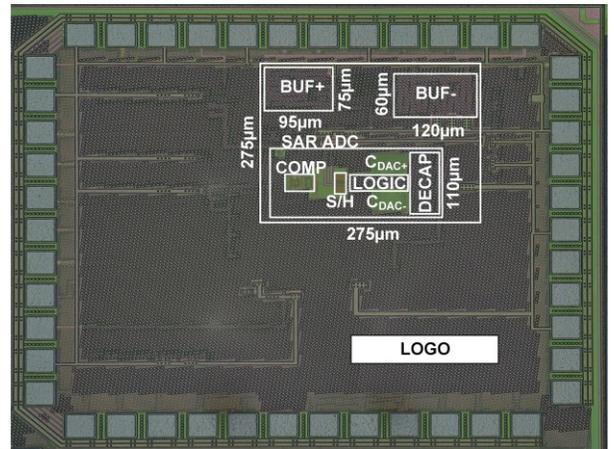


Fig. 4 Die micrograph of the SAR ADC along with two unity gain buffers BUF+ and BUF- . Total area is 0.075mm^2 with an active area of 0.04mm^2

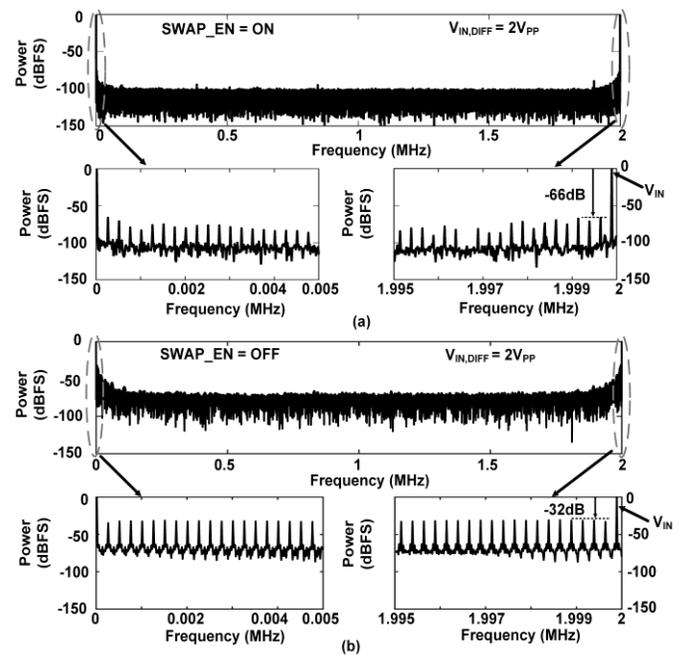


Fig. 5 Measured output spectrum of the buffered SAR ADC, normalized to the power level of the input tone at 1.99375MHz for $f_s = 4\text{MS/s}$ for (a) $\text{SWAP_EN} = \text{'ON'}$ and (b) $\text{SWAP_EN} = \text{'OFF'}$

shows the maximum and RMS voltage change that can occur at the input of the buffers as a function of input frequency (f_{IN}). Due to the swapping at buffer inputs, ΔV_{MAX} for the proposed architecture is $V_{\text{PK}}/2$ at half the Nyquist input frequency, i.e. at $f_s/4$. This means that for a given FSIR (V_{PK}), the maximum charge delivered by the signal source to the buffer's input capacitance (C_{IN}) is $Q_{\text{IN,MAX}} = C_{\text{IN}} \cdot V_{\text{PK}}/2$ at $f_{\text{IN}} = f_s/4$ and decreases on either side (of $f_{\text{IN}} = f_s/4$). The energy delivered by the signal source is therefore an order of magnitude less than that delivered to $C_{\text{DAC+}}/C_{\text{DAC-}}$ for conventional sampling without buffering and without swapping. Simulations show that $Q_{\text{IN,MAX}}$ is 30fC per sample operation for each channel, of which 18fC is delivered to the input of the buffer, 7fC to the FE comparator and 5fC to the switches in SWP1 .

III. MEASUREMENT RESULTS

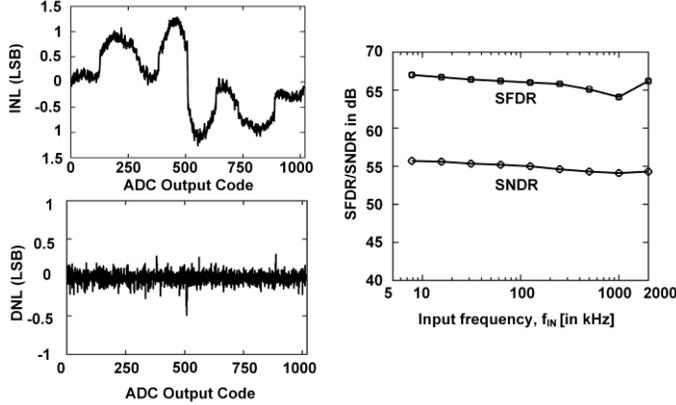


Fig. 6 Measured Static and Dynamic performance of the buffered SAR ADC at 4MS/s.

	This work	[1]	[6]
Technology	65nm	40nm	28nm
Supply Voltage [V]	1.2	1.2	1.1
ADC Buffer		2.5	1.2
Max. Sampling rate [MS/s]	4	35	104
ENOB_{Nyq}	8.73	12.1	7.2
Diff. Input Swing (pk to pk) [V]	2 V_{PP}	1.8 V _{PP}	1.2 V _{PP}
Power Consumption (ADC + Buffer)	0.149 mW	54.5 mW	3.1 mW
Max. Input Charge required per channel (Q_{IN,MAX})[†]	30 fC	180 fC	Not Reported
Walden FoM[‡] [fJ/conversion]	87	355	200 [#]
Area [in mm²]	0.075 (including decaps)	0.24 (including decaps)	0.024 (Core only)
Calibration	Yes, off-chip offset correction	Yes, off-chip DAC Calibration	Yes, DAC calibration, comparator offset trimming

[†]For [1] Q_{IN,MAX} calculated for their reported C_{IN} = 200fF and V_{PK} = 0.9V.

[‡]Walden FoM = $\frac{\text{Power (ADC+Buffer)}}{\min[2 \cdot \text{ERBW}, f_s] \cdot 2^{\text{ENOB}}}$

[#]Calculated for the ENOB near Nyquist B/W as per the measurement data in [6] instead of at low frequency as reported in [6].

Table 1: Comparison of SAR ADCs with integrated buffers

The chip was fabricated in a 65nm CMOS process. Fig. 4 shows the 10b SAR ADC including input buffers and decaps that occupy an area of 0.075mm² (active: 0.04mm²). Fig. 5a and Fig. 5b show the FFT of the measured data for a near Nyquist input frequency signal: f_{IN} = 1.99375MHz at 4MS/s and 1.2V supply and 2V_{PP} input for the swapped (SWAP_EN = ‘ON’) and non-swapped (SWAP_EN = ‘OFF’) cases respectively. The distortion in the case of non-swapped (conventional) architecture is due to the clipping of the buffer for input swing significantly exceeding half the FSIR. The mismatch between the buffers is calibrated only once at start-up and the additional

hardware required is just an adder/subtractor as explained in Section II. Fig.6 shows the SFDR and SNDR of the buffered ADC throughout the Nyquist band at 4MS/s. The peak INL and DNL is respectively 1.2 and 0.5 LSB as shown in Fig.6. The maximum jump in the INL and DNL is around the mid code which corresponds to the switching of all the capacitors in the binary DAC used in this ADC. The total power consumption of the chip is 149μW: 9μW for the ADC and 70μW for each buffer. With an ENOB of 8.73, the Walden FoM for the buffered ADC is 87fJ/conv-step. The mismatch between the buffers is calibrated only once at start-up and the additional hardware required is just an adder/subtractor. Table 1 shows a benchmark of our buffered ADC and the buffered ADCs in [1] and [6]. Note that most of the energy efficient SAR ADCs do not include input buffers which limits the scope of the comparison. For a fair comparison, the Walden FoM including the power of both the input buffer and the ADC is computed and compared in Table 1. In comparison to [1] and [6], our buffered ADC does not require an additional supply voltage for the buffers and it can handle 2V_{PP} input over the full Nyquist band and has the lowest Walden FoM. Therefore, by swapping the input signal paths based on the sign of (V_{INP} – V_{INN}), input buffers can be used that only need to drive either half of the FSIR. This has the advantage that the buffers do not need a separate power supply, it saves power consumption and a linearity degrading complimentary (both PMOS and NMOS) input differential pair is not needed to handle rail-to-rail inputs.

IV. CONCLUSION

The proposed buffered SAR ADC can process near rail-to-rail inputs, offers a high input impedance that can be easily driven by a low power sensor and has low power consumption, making it an excellent choice for IoT applications. Our buffered SAR ADC operates from a single supply voltage (1.2V) and alleviates the need of any additional supply voltage level to interface with wireless sensor nodes. It achieves a lowest reported Walden FoM of 87fJ/conv-step (including buffers) to the best of our knowledge and provides a 2V_{P-P} differential FSIR.

V. REFERENCES

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