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Holistic optimization architecture enabling sub-14-nm projection lithography

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Abstract. Parallel with the introduction of EUV lithography, immersion lithography is being extended to the 14- and 10-nm node, and the lithography performance requirements need to be tightened further to enable this shrink. Next to generic scanner system improvements, application-specific solutions are needed to follow the requirements for critical dimension (CD) control and overlay. The application-specific solutions need a holistic optimization approach for the scanner, the mask, and the patterning process. We will describe the holistic lithography systems architecture that enables dynamic use of high-order scanner optimization based on advanced actuators of projection lens and scanning stages. Next to the scanner system, key components of this architecture are an angle-resolved scatterometer to measure CD, overlay, and focus, and an off-tool computation server to calculate application-specific recipes for the scanner. Based on real production wafer data, we will show the benefit for CD control, focus control, and overlay control, and demonstrate lithography performance levels required for 14- and 10-nm node production. © *2014 Society of Photo-Optical Instrumentation Engineers (SPIE)* [DOI: 10.1117/1.JMM.13.1.011006]

Keywords: 14 nm; 10 nm; immersion lithography; critical dimension uniformity; overlay; focus; diffraction-based overlay; holistic lithography.

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1 Introduction

While the semiconductor roadmap is approaching the single-digit nanometer era, multiple solutions for lithographic patterning are being prepared. As illustrated in Fig. 1, the resolution shrink path initially follows the ArF immersion line and later the EUV line. From 32-nm node on, immersion is used in combination with patterning split methods; from 10-nm on, EUV is expected to be used for the most complex layers.

To support the lithography roadmap, leading edge projection lithography tools are being developed for both ArF (Ref. 1) and EUV.[2] Projection lithography has been the workhorse for semiconductor manufacturing since 1973. The very first projection lithography tool, the Perkin Elmer Micralign, was used to print features of $\sim 3\ \mu$m. Since that time, lithography performance optimization has come a long way. As Fig. 2 illustrates (using overlay as an example),[3] almost three orders of magnitude performance improvements is achieved, and during these four decades, we can recognize different phases in this development.

In the early days, overlay optimization was a more or less manual action, but during the 1980s, the understanding of overlay grew, and linear optimization models linked to projection tool capabilities were derived and used for systematic system setup improvements. The original model for intrafield overlay was proposed by MacMillen and Ryden.[4] Later Brink et al.[5] developed an overlay model that considered both the interfield and intrafield effects and extended the intrafield model toward fifth-order lens distortion variables. In the 1990s, process control in the wafer fab has been adopted widely, and metrology feedback became an adopted method to reduce overlay. One of the first papers describing statistical overlay control was published by Engelsberg and Leach,[6] and a little later Drew and Kemp demonstrated improvements in a wafer fab application with automated overlay feedback.[7] In the early years of the third millennium, the simple overlay process control developed toward advanced process control (APC) for both overlay and critical dimension (CD). Papers of Gould,[8] Ausschnitt,[9] and Laidler[10] published advanced wafer lot optimization schemes improving lithography performance by more than 30%.

With the introduction of more complex scanner systems with advanced projection lens manipulators, higher-order wafer corrections have become available[11] and are being used in wafer manufacturing.[12] With the adoption of double patterning, the lithography optimization has become even more complex, driving to the need of even more flexible actuators. The latest 1.35-NA ArF immersion scanners now include actuators allowing freeform setting of illumination and lens aberration maps. In the ASML TWINSCAN systems, these functions are known as, respectively, FlexRay™ (Ref. 13) and FlexWave™.[14] These actuators allow an almost endless flexibility in optimization. Also, for overlay optimization, higher-order corrections are being used, and here freeform type of corrections are possible using high-order corrections per exposed field (HO-CPE). As explained by Brink,[15] these complex lithography methods require a holistic approach in the optimization, both for the wafer process design phase and in the wafer manufacturing phase. In the design phase, the process windows and metrology target robustness for process variations is maximized, whereas in the manufacturing phase the performance variation is minimized using dynamic process window control.

In this paper, we will discuss the systems architecture we build to support holistic lithography optimization for imaging and overlay. Specifically, we discuss scanner setup improvements for matched-machine overlay, reticle heating

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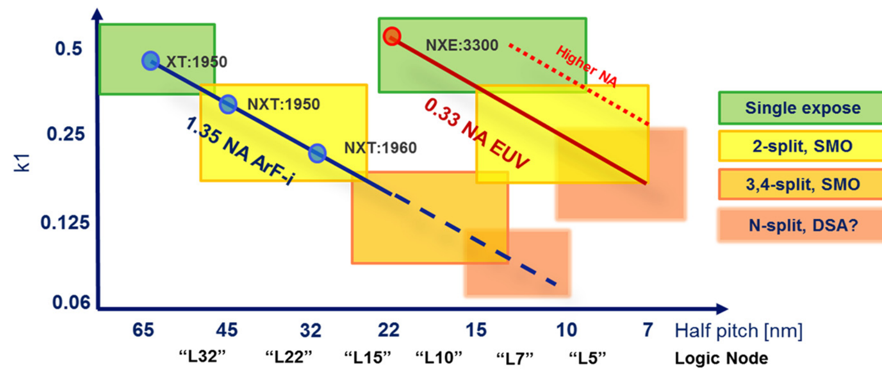

Fig. 1 Lithography patterning solutions ranked using k1 (k1 = Resolution * NA/wavelength).

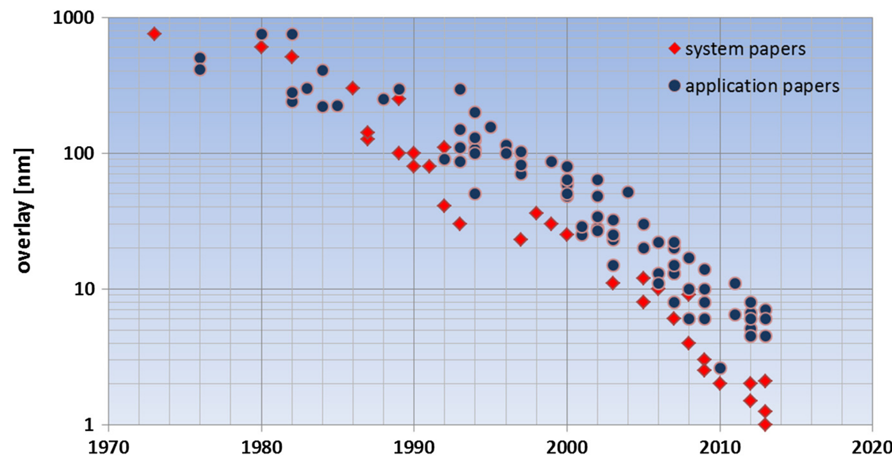

Fig. 2 An overview of published overlay results between 1973 and 2013.

control for improved on-product intrafield overlay, and the usage of high-order field-to-field corrections for imaging, focus, and overlay. These corrections are needed to bring on-product overlay performance to 3 nm and CD uniformity (CDU) to 1 nm. These lithography performance levels are supporting immersion lithography down to the 10-nm node. A more detailed description of the systems architecture we build to enable these corrections is given in Sec. 2. In Sec. 3 we will discuss the experimental results demonstrating the predicted imaging and focus performance improvements. The overlay experimental results and resulting overlay performance roadmap are discussed in Sec. 4. Finally in Sec. 5 we summarize and give our conclusions.

2 Building Blocks for Lithography Performance Control

The key component in the lithography performance control architecture is the scanning exposure tool and its interface to the actuators. Figure 3 shows the important actuator functions of the scanner. A pulsed laser is used to illuminate the reticle via an optical slit, and a lens projects the reticle image on the wafer, while the reticle and the wafer are scanned synchronously. Across-slit dose is actuated with the illuminator system, and together with the dose per pulse control of the laser, free shape dose uniformity patterns can be created per exposed field. A second function of the illuminator is to create the illumination pupil representing the angular distribution of the light illuminating the reticle. With the FlexRay illuminator, freeform pupil shapes can be created. The projection lens's main function is to image the high-resolution patterns of the reticle on the wafer; to control the phase of the diffracted light, the projection lens is equipped with aberration manipulators. With the FlexWave module in the projection lens, it is possible to create freeform wavefront profiles. Across the projected field, it is possible to adjust lens magnification and higher-order image distortion, a function that is needed for intrafield overlay matching. Interfield overlay matching is done by adjusting the wafer grid using the stage positioning actuators. Finally, with the z-positioning of the stage, it is possible to manipulate the focus z-map over the wafer.

In general, the subsystems of the scanner are controlled continuously. The scanner performance control is done with a combination of on-board sensor-based feedback and model-based feed-forward. The set-point of the internal subsystem control loops are determined by system calibrations, the so-called system setup and updated every lot, the so-called lot control. On top of this intrinsic scanner control, the actuators are also used for application-specific optimization, and in this case, the set-points of the actuators get an addition via user-defined corrections.

In Table 1, we give an overview of what type of performance control is possible using wafer-based metrology combined with computational lithography. The latter is especially used for process window optimization and can be used to reduce the metrology burden. For process window extension, source mask optimization (SMO) was introduced some years

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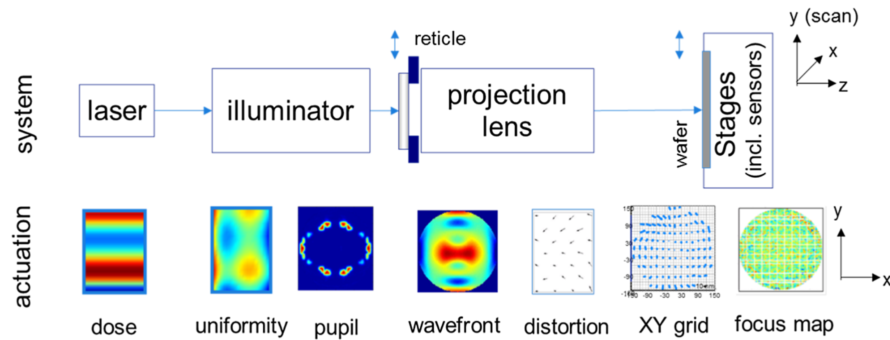

Fig. 3 Building blocks of an exposure system and their actuation capability.

Table 1 Landscape for wafer-based optimization solutions on a 1.35-NA immersion scanner.

	Lens		Illuminator		Stages and lens		
	Wave front	NA	Pupil	Dose	Focus	Wafer *XY*	Field *xy*
Application specific	Process window enhancement			Imaging Optimization		Overlay and alignment optimization	
Scanner stability and matching	Baseline system control						

ago,[16] showing that by co-optimizing mask with illumination source it is possible to increase the exposure latitude and the depth of focus of the critical patterns to be imaged. More recently, the use of pixilated freeform pupils has extended the SMO capability further, and process window evaluation for several device applications is discussed in Ref. 17. Since immersion lithography has been extended to 32-nm patterns, it has been reported that mask three-dimensional (3-D) effects impact the process window, and new developments in the computational lithography arena is to combine SMO with advanced wavefront engineering. Specifically, for FlexWave systems, SMO + FlexWave optimization algorithms have been developed, demonstrating significant gain in depth of focus for a logic application.[14]

The lithography optimization architecture we built is shown in Fig. 4. Next to the scanner we can recognize two other main building blocks: optical scatterometry for overlay, focus, and CD metrology, and an application server for sampling optimization and model-based control.

As explained by VanOppen et al.,[18] the baseline system control is based on exposing monitor wafers with reticles that contain many test targets, such that with high-density sampling the intrafield and interfield fingerprints for overlay, focus, and CDU can be determined. The monitor wafer flow is running in parallel with the production wafer flow, but the frequency of control updates is lower: typically one or two times a week. On the other hand, the updates of the settings for the production wafers is frequent (once per lot) and is based on a more sparse sampling of the imaging and overlay fingerprints.

The second building block of the lithography performance control system is an angle-resolved scatterometer, the principle of which is described in Fig. 5.[19] This high-NA angle-resolved scatterometer for scanner performance control combines measurement of overlay, focus, and CD in one sensor. In an angle-resolved scatterometer, the metrology signal is observed in the pupil of the metrology objective. The targets for overlay and focus are designed such that the signal of the first-order diffraction is measured. The method of measuring overlay with diffraction-based overlay (DBO) is described by Smilde in Ref. 20, and the method of measuring focus with diffraction-based focus (DBF) is

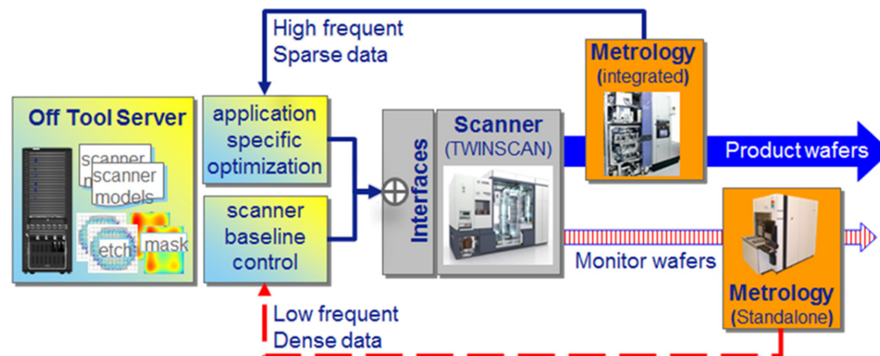

Fig. 4 Lithography optimization systems architecture for process window control.

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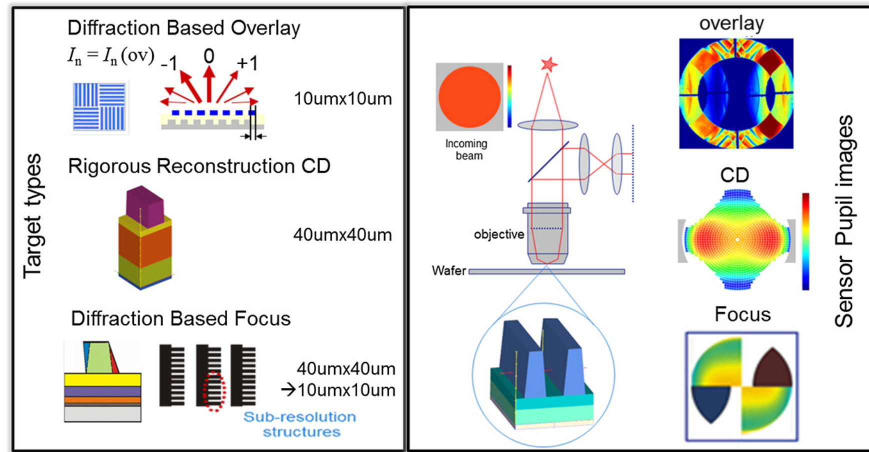

Fig. 5 Principle of the angle resolved scatterometer for overlay, CD, and focus metrology.

described by Benschop et al. in Ref. 21. The DBO overlay measurement is using small ($10\ \mu m \times 10\ \mu m$) in-die targets placed. The in-die targets are important since they enable the metrology of the high-order terms of the intrafield fingerprint. The DBF focus measurement uses scribe line targets, which create structures on the wafer with an asymmetric sidewall. The asymmetry of the sidewall angle is sensitive for scanner focus variations and relatively insensitive for wafer process variations.

Because of the small resolution and the relatively high detection wavelength (>425 nm), the pupil for CD metrology collects only the zero order, which is then rigorously reconstructed to retrieve the full 3-D CD profile of the measured pattern. More detailed explanation and results of this method are discussed by Cramer et al. in Ref. 22.

The metrology tool is used as a standalone version and a wafer track integrated version. The latter is of importance since it enables high frequent and fast updates of the scanner recipe for imaging and overlay corrections, whereas the standalone metrology tool is used for recipe creation and long-term baseline stability control using the monitor wafers. The scanner corrections for production wafers are based on the use of special targets for overlay, focus, and CD placed on the production mask.

The third building block of the performance control architecture is an off-tool lithography computation platform (LCP) server. The LCP is designed to serve multiple scanner and metrology tools at the same time. The server is used to compute the optimum lithography recipe for each scanner and each application. This LCP software contains computational models of the scanner, actual scanner performance data, and fingerprints and calibration data for the application-specific optimizations. For the integrated metrology system, the LCP is used to calculate the optimum sample schemes to enable dynamic high-order scanner corrections.

3 Imaging Performance Optimization

3.1 *Reducing the CD Uniformity Error Budget with Dose and Focus Optimization*

In Fig. 6 we present the CDU roadmap for 1.35-NA immersion applications[23] based on the anticipated improvements of the immersion scanner and based on the assumptions that

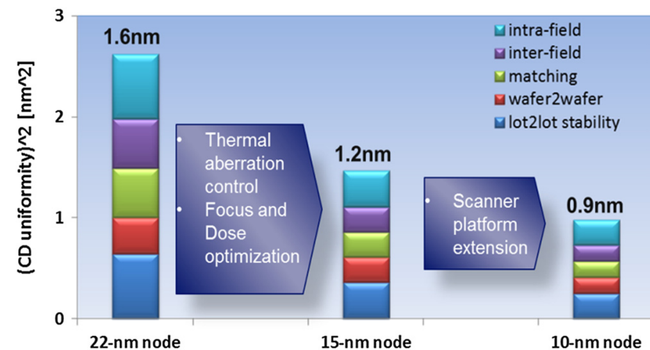

Fig. 6 Anticipated CDU roadmap for logic application.

wafer-based scanner stability control and wafer-based CDU optimization will be implemented. The error budget describes the lot-to-lot errors, wafer-to-wafer errors, matching, and inter- and intrafield terms.

Next to intrinsic scanner improvements, the CDU roadmap is based on application-specific optimization of focus and dose. This optimization makes use of the active dose and focus control actuators in the scanner system. The freeform expose dose interface for the scanner is allowing a two-dimensional vector-based input to create a freeshape dose uniformity pattern per exposed field. The exposed dose per field point is a result of the pulse energy E and the slit transmission T. If the field coordinates are given by (x, y) and the position of the field on the wafer is given by column and row indices (i, j), the exposure dose map $\underline{D}$ is obtained by multiplication of the energy vector with the transmission vector.

$$[\underline{D}(x, y)]_{i,j} = [E(y) \cdot T(x)]_{i,j}. \tag{1}$$

Focus control makes use of the stage z-positioning in six degrees of freedom. Per exposed field (i, j), the focus offset f and focus tilts R_x and R_y can be set. The focus map $\underline{F}$ over the wafer can be described by

$$[\underline{F}(x, y)]_{i,j} = [f + xR_y + yR_x]_{i,j}. \tag{2}$$

The wafer fingerprints for interfield and intrafield are measured with the angle-resolved scatterometer on targets

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designed on the customer product reticle. The CDU fingerprint is measured using full reconstruction and the focus is measured using DBF targets.

The optimization of CDU and focus is described in the work flow chart presented in Fig. 7. CDU and focus are optimized independently. In a first step, the DBF and/or CD targets must be designed. For DBF, the target design is such that for the given scanner illumination setting and the given wafer process stack, the printability of the target is optimized and the scatterometer signal is maximized for detectability of focus signals and robustness against other process perturbations such as dose. Depending on the needed process corrections, the target density on the production mask is determined and designed; this is done for both DBF targets as well as CD metrology sites. In a second step, the sensitivity of the targets for focus and dose is determined. This is done by exposing a focus-expose-matrix of the product mask on the wafer. The DBF targets and/or CD targets are measured as function of focus and dose to create the calibration curves. Now that the optimization cycle has been initialized, the product wafers can be exposed, and during the production process, the scatteromer measures the interfield and intrafield variance of focus and CD and calculates the correctables for the subsequent lots. Finally, the corrections are applied. During wafer production, the CD and focus corrections are monitored in each lot using the integrated scatterometer. Depending on possible drift or changes, the correction recipe can be updated.

3.2 *Experimental Results*

For a logic use case,[21,24] we investigated the benefit of this imaging performance optimization. First, in Fig. 8 we show the experimental results for CDU. The left three groups show CDU of three lots of ∼1.1 nm without any correction. The CD on these lots was measured with the angle-resolved scatterometer, and based on these measurements, corrections were calculated, which were applied when exposing another two lots. These lots (on the right) show a more than 2× improved CDU.

For across-wafer focus optimization on production wafers, we developed a new method based on diffraction-based asymmetric focus targets. For scribe line usage, we use a DBF target with size of 40×40 μm, and later for in-die usage, we will use DBF targets with size of $10\times$ 10 μm. We expect that the typical application will use few marks on the reticle and corrects focus offsets per field. For ultimate performance, the R_x, R_y focus tilt corrections will be used with more DBF targets placed per field. To investigate the benefit of on-product focus optimization, we investigated a logic use case, the experimental results of which are presented in Fig. 9. The test was done on a full wafer exposure with sample layout of 4×8 per field. The test was executed on a back-end-of-line (BEOL) process stack wafer. The applied field-to-field corrections include focus offset, and focus tilts R_x and R_y. The result shows that focus uniformity is improved toward 18 nm, which is an improvement of ∼35%. This is very significant, especially since the process latitude for focus for these BEOL layers is small.

4 Overlay Performance Optimization

4.1 *Reducing the Overlay Error Budget with High-Order Field-to-Field Corrections*

In Fig. 10 we show the on-product overlay error budget breakdown and the overlay improvement roadmap for immersion lithography.[25] This is based on a contact to gate use case. The budget assumes full wafer sampling and full lot metrology evaluation and is given for a matched machine usage and a dedicated chuck usage. In matched mode

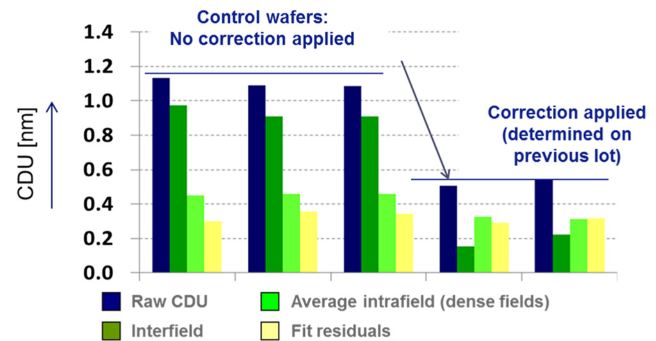

Fig. 8 Results of optimization of CD uniformity fingerprint using free-form dose corrections.

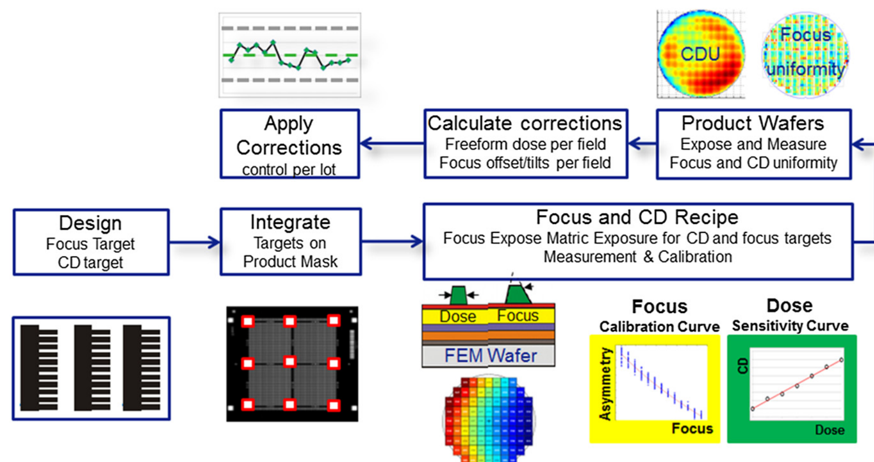

Fig. 7 Optimization flow for CD and/or focus uniformity from target design to control on product wafers.

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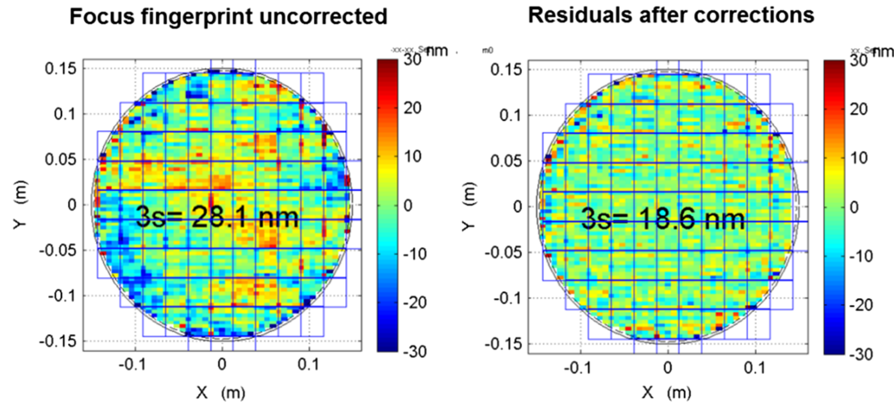

Fig. 9 Results of optimization of across-wafer focus uniformity using diffraction-based focus targets.

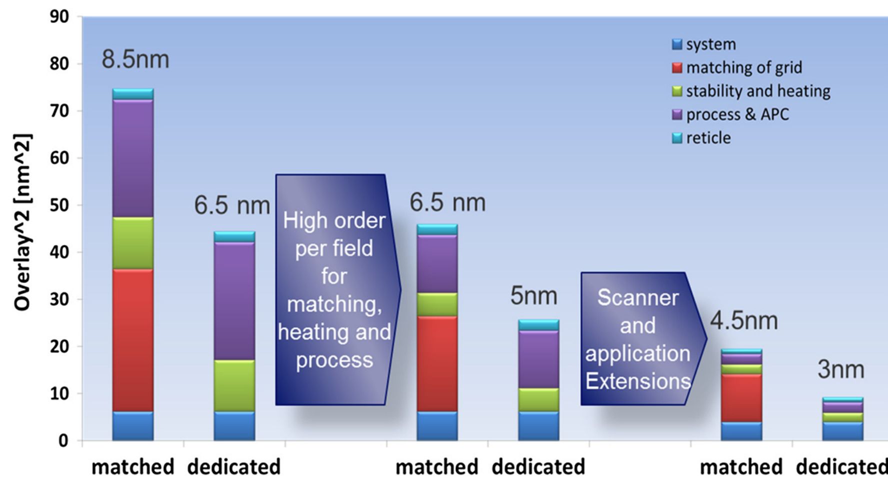

Fig. 10 Anticipated overlay roadmap assuming contact to gate layer.

usage, it is assumed that the different layers are randomly exposed on different machines, and in dedicated mode, it is assumed that the logistics of the wafers is organized such that all critical layers are exposed on one machine with dedicated chuck.

The on-product overlay performance is determined by the scanner and the scanner's interaction with the different process layers. The latter part is called the application-specific part of the budget, whereas the first part is system generic. As can be seen in the budget, the intrinsic systems overlay performance is only a small part of the budget. This part is easily measured and is part of the systems acceptance testing, just as the matched machine overlay. The application parts of the budget are depending on the used reticles, used resist process, and the layers on the wafer. Depending on previous process steps, the wafers can be deformed and the alignment and overlay targets printed on the wafer can be deformed. The reticle content (effective transmission) and the required resist dose determine the lens and reticle heating effects, and with dedicated testing, these effects can be quantified. The wafer deformation and mark deformation is more difficult to quantify from simple testing. A more in-depth study is needed per process step to quantify these contributors. Metrology and APC errors are part of the budget, but are relatively small.

Next to intrinsic scanner platform improvements, the roadmap is based on reducing the error components for matching, heating, and process. These three components can be reduced by applying higher-order corrections for each individual exposed field (i, j). In Eq. (3) we present the description of the wafer deformation map we can set with the scanner actuators. The correction per field is defined as a polynomial up to third order. The correction vector (dx, dy) as defined by this polynomial is already available as lot average intrafield process correction. New for the latest scanners is that with new lens control, this correction can be set different for each individual field, and this can be done without impact on the productivity of the scanner.

$$\begin{pmatrix} dx \\ dy \end{pmatrix}_{i,j} = \begin{pmatrix} k_1 + k_3x + k_5y + k_7x^2 + k_9xy + k_{11}y^2 + k_{13}x^3 + k_{15}x^2y + k_{17}xy^2 + k_{19}y^3 \\ k_2 + k_4y + k_6x + k_8y^2 + k_{10}yx + k_{12}x^2 + k_{14}y^3 + k_{16}y^2x + k_{18}yx^2 + k_{20}x^3 \end{pmatrix}_{i,j}. \tag{3}$$

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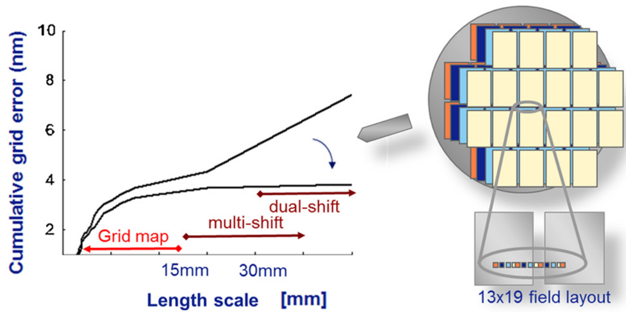

Fig. 11 Illustrating the wafer grid calibration method using multishift exposures to sample spatial grid errors.

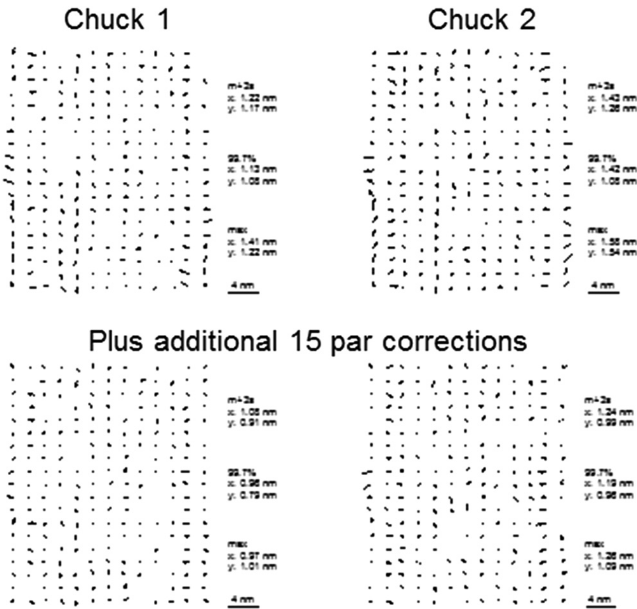

Fig. 12 Experimental results of intrafield distortion after calibrating the immersion tool, with the status after improved grid setup on the top row and that after applying an additional 15-parameter correction on the bottom row.

Depending on scanner system type and correction algorithm, a subset of these 20 parameters is available for field-to-field adjustments. In the next sections it will be shown how these actuators improve scanner matching, scanner heating control, and correction for process overlay effects.

4.2 *Experimental Results: Scanner and Lens Matching*

As Fig. 10 already indicated, for matched machine usage, the matching of the grid is the largest error in the overlay budget. Machine matching is done using the baseline monitor wafer flow as described in Sec. 2. In order to improve the grid calibration, we developed a new method based on multishift exposures to pick up spatial grid errors. In Fig. 11, the principles of this method are illustrated. In the scanner system, the stage positioning is done using a grid plate encoder system. For spatial errors $< \sim 15$ mm scale, the grid plates are first measured at the supplier and additionally calibrated during scanner setup using sensor data of the stage positioning system. For spatial errors $> \sim 15$ mm scale, other system contributors become important as well, and the wafer grid must be calibrated. Here we expose multiple field layouts with overlay and alignment targets on a reference wafer with etched marks on a 13×19 grid per field. The reference wafers approximate a perfectly calibrated scanner that has a very straight grid. The wafers have etched alignment marks and DBO targets such that the wafer grid calibration can be done with either the alignment sensor or the angle-resolved scatterometer. By exposing fields with dual and multishifts over the 13×19 grid, we sample the wafer grid error. By using the stage actuators and the higher-order lens actuators, we can calibrate the grid errors toward the reference wafer. This method results in a field layout independent grid matching. An additional correction with the higher-order process corrections is possible, which will make the matching calibration layout dependent.

With this new calibration method, the matched machine overlay has been improved from 5.5 nm to <4 nm. Proof data of the latter are presented in Figs. 12 and 13. First, Fig. 12 shows the result of the intrafield distortion fingerprint after calibration: the maximum distortion error is 1.6 nm, and after applying additional 15-parameter corrections, this reduces to 1.2 nm.

For across tool matching, we performed an experiment involving five different immersion scanners. The reference wafers are used to calibrate the five different machines. In Fig. 13(a), we present an example result of the achieved matched overlay with respect to the reference wafer. On one of the systems, an overlay of 3.2 nm is obtained (99.7% criterion for full wafer, thru lot). The other machines have similar performance toward the reference wafer. Looking to

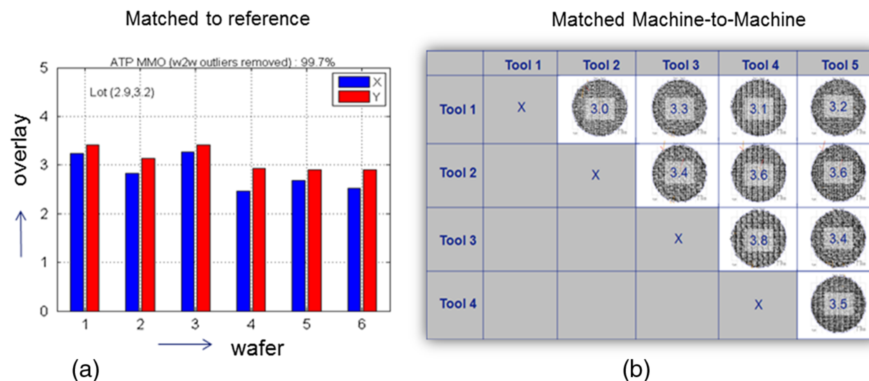

Fig. 13 Experimental results of the new machine matching method. (a) the matched overlay of a six wafer lot to the reference wafer, (b) Result of cross-matching a pool of five tools.

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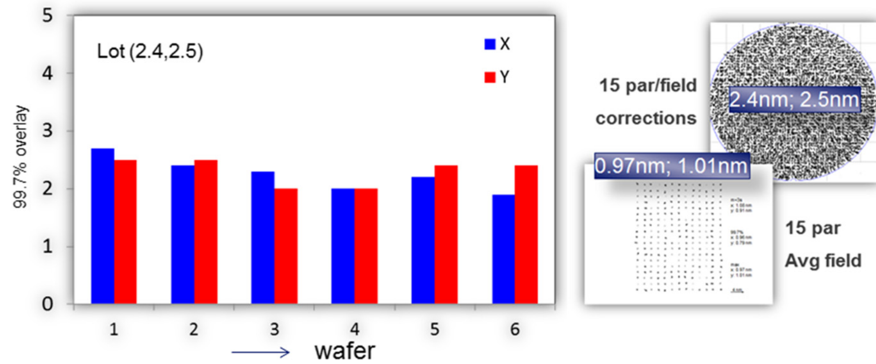

Fig. 14 Experimental results of matched machine overlay after applying the new machine grid calibration method and an additional 15-parameter-per-field correction.

the machine-to-machine overlay, we find matched overlay values between 3.0 and 3.8 nm [Fig. 13(b)].

The matched machine overlay can be improved further with high-order corrections; however, this correction is layout dependent. In Fig. 14, we present the results of such an additional correction, where the data show that the matched machine overlay is reduced to 2.5 nm for the lot of wafers exposed. The correction applied was higher order per field as explained in Sec. 4.4.

4.3 *Experimental Results: Reticle Heating Control*

Overlay heating effects come from the projection lens and from the reticle. The projection lens thermal aberration control improvements are discussed in a previous paper.[23] In the same paper we also presented the status of reticle heating control. Reticle heating is caused by light absorption in the absorption layer on the mask and results in deformation of the mask blank. Reticle heating is especially seen in low transmission mask. The mask deformation is partly corrected by the wafer-to-wafer reticle alignment, but with decreasing overlay requirements, additional measures are needed. In the latest generation immersion tools, we implement a further extension of the reticle heating control, now including 18-parameters field-to-field overlay control (k1 to k20, excluding k17 and k20). In Fig. 15, we present experimental results using a low transmission mask (1.4%), exposed with high-exposure dose ($50\ \mathrm{mJ/cm^2}$) at maximum wafer throughput. For this extreme use case, we are able to reduce the intrafield overlay effect to <2 nm, which is about factor 2 better than the control based on 15 parameters.

4.4 *Experimental Results: Product Overlay Control*

In a wafer fab, GridMapper[10] is used to fine tune the overlay. GridMapper is using higher-order grid corrections and higher-order intrafield corrections to match the expose grid to the desired application-specific grid. GridMapper can also apply linear corrections per exposure (CPE). The corrections are applied per lot.

For more advanced overlay optimization, we extended this functionality to enable more frequent updates (each lot) and to have the high-order intrafield parameters also available for CPE (HO-CPE). For dedicated chuck usage, the corrections can be set different per chuck as well. In the initial phase, 12 parameters are available, but in the near future, this will be extended to 15 parameters and 19 parameters depending on scanner system type. With such a large degree of correction freedom, the wafer metrology burden may explode since these 19 parameters need at least 10 xy measurements per field, which for a full wafer with ∼100 fields already is summing up to ∼1000 measurements. This is not practical for high volume, and that is why HO-CPE needs fingerprint

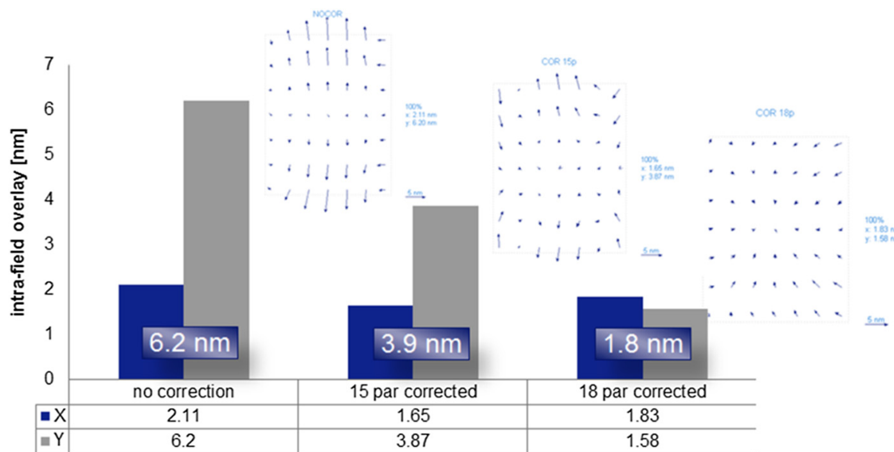

Fig. 15 Experimental results of reticle heating–induced intrafield overlay after applying 15-parameter and 18-parameter correction.

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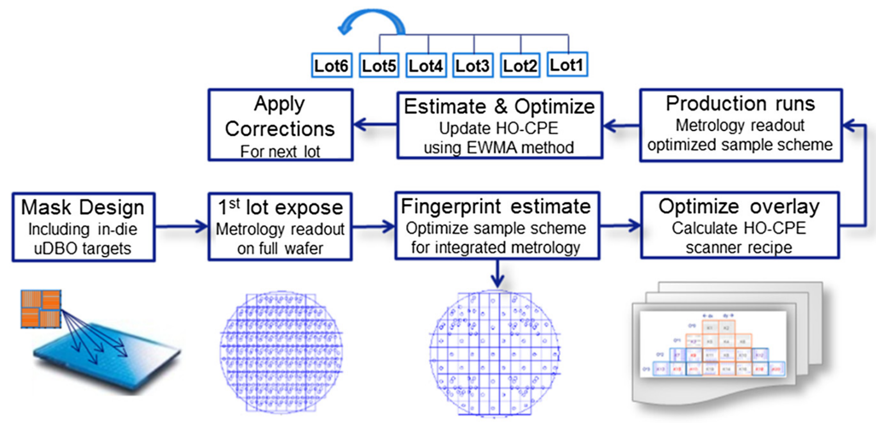

Fig. 16 Overlay optimization flow from target design to control on product wafers using dynamic high-order corrections per exposed field.

model estimation to reduce the metrology burden. In Fig. 16, we illustrate the overlay optimization flow for HO-CPE.

The flow starts with overlay metrology target design and target distribution over the mask. For the designed target, the metrology recipe is created as well. After the reticle is fabricated, the first lot is exposed and the overlay metrology is done on the full wafer layout. For this lot, typically four wafers with 1000 to 2000 points per wafer are measured on the standalone angle-resolved scatterometer. The data are send to the off-tool application server (LCP) and here the wafer fingerprint is calculated. Based on this data, a reduced overlay sample scheme is derived, resulting in ~200 usable metrology points per wafer. Together with the fingerprint estimation model, the sample points give sufficient information for the calculation of the HO-CPEs. The initialization is followed by the high-volume production runs. Here the metrology can be done on the wafer track integrated scatterometer to enable fast feedback. The metrology is done for every production lot. Using the method of exponentially weighted moving average, the updated scanner recipe for HO-CPE is calculated.

In Fig. 17, we present experimental results on the product overlay improvements achieved with this method. The reported overlay numbers are based on full wafer readout (used to verify the benefit of this method). The achieved overlay with 12-parameter HO-CPE of 4.5 nm is ~2 nm lower than the process of record based on the linear 10-parameter per wafer correction and 1 nm lower than the linear six-parameter per field correction.

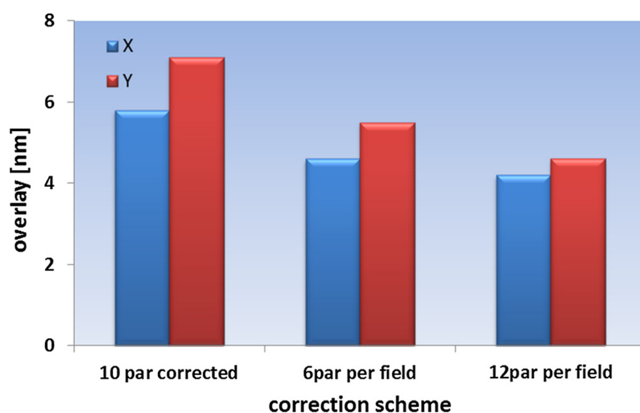

Fig. 17 On-product overlay results for a product like test wafer for three different optimization schemes.

5 Summary and Outlook

Projection lithography remains the workhorse for semiconductor manufacturing. In this paper, we discussed the extension of immersion lithography to the 14- and 10-nm node, but it is expected that the 10-nm node will also be the manufacturing node where we will start to see EUV taking over the most difficult patterning steps.

Lithography performance needs to be improved toward 1-nm CDU and 3-nm on-product overlay. Next to generic scanner system improvements, application-specific solutions are needed to follow the requirements for CD control and overlay. The application-specific improvements are based on a holistic lithography optimization, which combines wafer-based system tuning for imaging and overlay with computational optimizations of process window and process design.

In this paper, we described the systems architecture of holistic lithography including a 1.35-NA immersion scanner, an angle-resolved scatterometer for system stability control and in-line production optimization, and a fab-wide computational server to compute the application-specific recipes of the scanners.

In the experimental section, we discussed result improvements of CDU, focus, and overlay test cases by applying high-order field-to-field corrections. The experimental data presented show that with these corrections the lithography performance can be improved from 20 to 50% depending on the exact case. These performance improvements enable the use of ArF immersion down to the 10-nm node.

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