Highly-doped in-plane Si electrodes embedded between free-hanging microfluidic channels

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Novelty: Highly-doped in-plane Si electrodes were embedded between free-hanging microfluidic channels using Surface Channel Technology. The cross-sectional area of the electrodes can be controlled by tuning the distance between the release windows and the channels. The large cross-sectional area of the electrodes is especially beneficial as microheater, but they also enable resistive or capacitive readout in e.g. flow sensors.

Surface Channel Technology innovation concept. Free-hanging microfluidic channels fabricated by Surface Channel Technology (SCT) [1] are used in various microfluidic applications, like thermal [2] and Coriolis flow sensors [3], pressure sensors [4], fluid parameter sensors [5] and control valves [6]. The key process steps are: **1)** Semi-isotropical channel etch in bulk Si through an array of small slits (Fig. 1a), **2)** channel wall formation by low-stress LPCVD Si-rich Si_xN_y (SiRN, Fig. 1b), **3)** thin-film metal deposition for electrical interconnect (Fig. 1c), and **4)** channel release by semi-isotropically etching the bulk Si through release windows next to the channels (Fig. 1d). The shapes and dimensions of the channels are controlled by the position and density of the slits and the channel etch [3]. In traditional SCT all electrical functionality (e.g. heating and temperature sensing, resistive strain gauges, capacitive readout) is provided by the thin film metal layer. In this paper we propose to integrate additional Si electrodes between the channels as indicated in Fig. 1, which have important advantages like a much higher power dissipation when used as heaters, higher sensitivity when used as strain gauges due to the piezoresistivity of Si, and the possibility of in-plane capacitive sensing. Other approaches to integrate Si electrodes have been proposed before using SOI wafers [3] or refilled trenches [7], but these options require SOI wafers and add more complexity to the fabrication process.

Experimental results. Test masks were designed to realize parallel channels with a Si electrode in between. The distance d between two rows of slits was varied from $55\,\mu\text{m}$ to $65\,\mu\text{m}$. For $d \geq 60\,\mu\text{m}$ two separate channels are formed. The release windows were chosen $200\,\mu\text{m}$ wide. The distance L between two release windows was varied. Fig. 2a shows typical result of fully released channels with Si between the channels. If the release windows are close to the channels, channels are completely released and the Si in between is completely removed (Fig. 2b). For $L = 100$, 140 and 250 μm an increasing amount of Si remains between the channels (Fig. 2c to 2e). For even larger L the channels are no longer completely released.

Application as electrode. The resistance of the Si electrode depends on the doping level and cross-sectional area. We used Boron-doped Si wafers with resistivity ranging from 0.01 to $0.02\ \Omega \cdot \text{cm}$. The results in Fig. 2 show that the cross-sectional area can be designed from approximately $35\,\mu\text{m}^2$ (Fig. 2c) to $720\,\mu\text{m}^2$ (Fig. 2e). Table 1 lists the calculated properties of the resulting Si electrodes in comparison to a typical $10\,\mu\text{m}$ wide, $200\,\text{nm}$ thick Pt electrode on top of the channel. Especially when used as heaters the Si electrodes provide a clear advantage. Supplying the same current density through the electrodes a factor of 10^4 to 10^5 more power can be dissipated due to the combination of higher resistance and larger cross-section. Fig. 2f shows that it is also possible to embed 2 electrodes between 3 adjacent channels. This could e.g. be used to realize a relative permittivity sensor [8].

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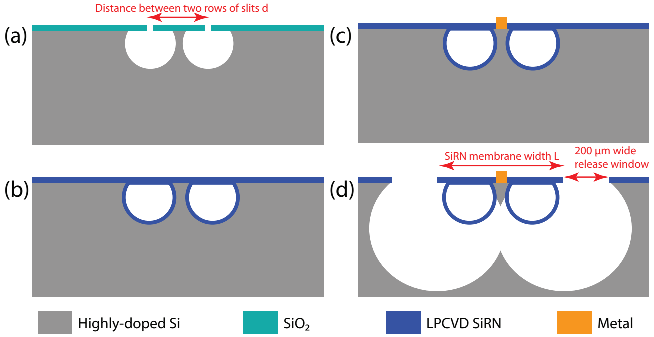

Figure 1: Embedded Si electrodes between two free-hanging channels are fabricated by SCT process in the following key steps. Start with a highly B-doped Si wafer, (a) etch Si through two rows of slits and form two separate channels, (b) deposit SiRN to seal the slits and form SiRN channel walls, (c) sputter and pattern thin film metal to make ohmic contact with the underlying Si, and (d) channel release etch via two $200\,\mu\text{m}$ wide release windows. The SiRN membrane width L determines the release windows location.

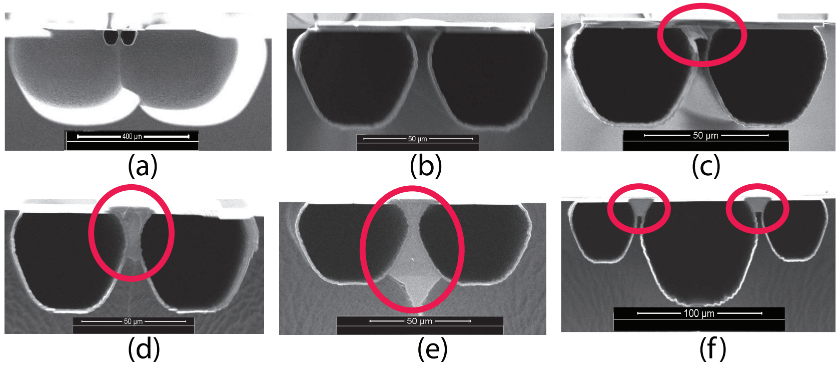

Figure 2: SEM photographs of (a) a fully released channel structure, and close-ups of (b) channels with no remaining Si, (c) a small ($\sim 35\,\mu\text{m}^2$) Si electrode, (d) a medium ($\sim 230\,\mu\text{m}^2$) Si electrode, (e) a large ($\sim 720\,\mu\text{m}^2$) Si electrode, and (f) a 3-channel structure with 2 Si electrodes.

1 mm long microheaters	Resistivity [Ω cm]	Area [μm^2]	Resistance [Ω]	Power per unit length [W m^{-1}] (supply 1 mA)	Power per unit length [W m^{-1}] (supply $5 \times 10^8\ \text{A m}^{-2}$)
200 nm thick Pt	1×10^{-5}	2	50	5×10^{-2}	5×10^{-2}
Small Si electrode	1×10^{-2}	35	2857	2.86	8.75×10^{2}
Medium Si electrode	1×10^{-2}	230	435	4.35×10^{-1}	5.75×10^{3}
Large Si electrode	1×10^{-2}	720	139	1.39×10^{-1}	1.8×10^{4}

Table 1: Comparison between Pt and Si electrodes for Joule heating. For current density of $5 \times 10^8\ \text{A m}^{-2}$, Si electrodes with large cross-sectional area and resistance can dissipate more power per unit length.