Interface Trap Density Estimation in FinFETs from the Subthreshold Current

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***Abstract*—In this work we present a measurement approach to determine the interface trap density in FinFETs as a function of their energy. It is based on the precise determination of the gate voltage dependent ideality factor of the subthreshold current in this device. The required measurement accuracy for temperature, drain current and transconductance is derived, and we propose an implementation for wafer-level device measurement on contemporary test set-ups. Exemplary interface trap distributions are shown as obtained from two FinFET device technologies, featuring the commonly observed bathtub shape.**

***Index Terms*—MOS devices, FinFETs, Current, Complementary MOSFETs (CMOSFETs), Traps, Interface states**

I. Introduction

At the semiconductor-insulator interface in a metal-oxide-semiconductor (MOS) stack, imperfections in the chemical structure lead to interface traps. These localized defects can trap and release mobile charge, leading to drain-current noise [1][2] as well as a reduced electrostatic control of the gate over the channel [3]-[5]. Interface traps are formed during device processing, but can be additionally created by e.g. ionizing radiation and electrical stress. CMOS process development, process control and reliability assessment require an accurate estimate of the interface state density in these devices.

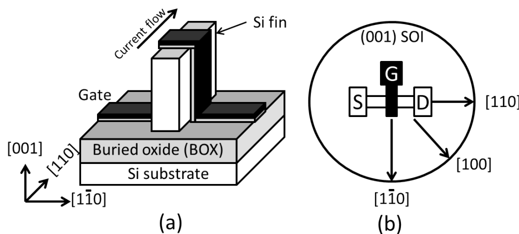

Fig. 1. (a) Bird's eye view of a schematic single fin SOI (1$\bar{1}$0)/[110] FinFET and (b) its orientation on the silicon wafer. The fin has source and drain connections, and the channel region is surrounded by the gate dielectric and the gate metal. In this device configuration there is no separate body contact. Two device sets were used for the experiments: device set I in which the fin height H_{FIN} is 65 nm, and device set II where H_{FIN} = 150 nm. The figures are not to scale.

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Several methods are known to experimentally estimate the interface trap density of states (D_{it}) [3],[4], such as the low-frequency (quasi-static) capacitance-voltage ($C-V$) method, the conductance method, the high-frequency $C-V$ method, and charge pumping. Some of these require specific test equipment, and they all require a separate backgate or body contact. The latter, in particular, is a problem in many device configurations such as FinFETs because separate body contacts cannot be realized, see for instance Fig. 1.

Therefore, we propose to extract the interface trap density from subthreshold current measurements, extending a technique earlier proposed for bulk MOSFETs [6]. In the remainder of this article we will refer to the new method as the $g_{\mathrm{m}}/I_{\mathrm{D}}$ method.

Prior art related to this work deals with subthreshold current modeling of planar SOI MOSFETs [7]-[11] in which there is an unavoidable asymmetry between the trap densities at the gate dielectric-SOI and SOI-buried-oxide (BOX) interfaces. In some of these reports analytical models have been used for extracting the D_{it} in FD-SOI MOSFETs [10], [11]. Also in the field of GAA Si nanowire FETs analytical models have been used with [12],[13] or without [14] the aid of numerical simulation tools.

In this work, we focus on the measurement issues in the $g_{\mathrm{m}}/I_{\mathrm{D}}$ method for D_{it} estimation of fully-depleted symmetric FETs. In section II the basic methodology is briefly introduced. Section III covers the experimental details and the results. Section IV describes the accuracy of the method and the necessary measurement precision, after which the conclusions are drawn in section V.

II. Relation between subthreshold current and trap density

In this section we postulate a newly derived relationship between the subthreshold current and the interface state density. It is based on the assumptions that the depletion charge can be neglected in FinFETs, and that the transistor under study shows negligible short-channel effects. Further, the trap distribution is assumed to be uniform along the channel. For subthreshold, we derived that the ideality factor m follows:

$$m = \frac{dV_{\mathrm{GS}}}{d\psi_{\mathrm{s}}} = \frac{1}{u_T}\frac{I_{\mathrm{D}}}{g_{\mathrm{m}}} = 1 + \frac{d}{d\psi_{\mathrm{s}}}\int_0^{\psi_{\mathrm{s}}} \frac{C_{\mathrm{it}}(\psi)}{C_{\mathrm{ins}}} d\psi = \frac{C_{\mathrm{ins}} + C_{\mathrm{it}}(\psi_{\mathrm{s}})}{C_{\mathrm{ins}}}. \tag{1}$$

Hence,

$$C_{\mathrm{it}}(\psi_{\mathrm{s}}) = \left(\frac{1}{u_T}\frac{I_{\mathrm{D}}(\psi_{\mathrm{s}})}{g_{\mathrm{m}}(\psi_{\mathrm{s}})} - 1\right) C_{\mathrm{ins}}. \tag{2}$$

In these equations, V_{GS} is the gate-source voltage, ψ_s is the surface potential, $u_T = kT/q$ is the thermal voltage, I_D the drain current, g_m the transconductance, C_{it} the interface trap capacitance per unit area, and C_{ins} is the insulator capacitance per unit area. Because equation 2 is used to derive C_{it} from the ratio between transconductance and drain current, we name this approach the g_m/I_D method. The trap density follows from [3]:

$$D_{it} = \frac{1}{q^2} C_{it}. \tag{3}$$

Further, since at the mid gap energy level ψ_s = 0 V we can assume that

$$E - E_v \approx \frac{E_g}{2} + q \cdot \psi_s, \tag{4}$$

ignoring the contribution of the effective densities of band states and where E, E_v, and E_g are the energy, valence band edge energy, and bandgap, respectively.

Equation (4) is valid provided that the (electron) quasi-Fermi level does not vary much along the channel length so that the same energy level E is probed across the entire channel. This implies that the method works best for a low applied V_{DS}. On the other hand, a certain drain-source bias is of course necessary to measure the subthreshold current. At a given measurement temperature T it is recommended not to exceed $V_{DS} \simeq u_T$.

We further need to relate the surface potential ψ_s to the applied gate voltage V_{GS}. To that purpose, we employ the long-channel subthreshold current relation [3], [5], [15]:

$$I_D = I_0 \cdot e^{\frac{\psi_s}{u_T}} \left(1 - e^{-\frac{V_{DS}}{u_T}}\right), \tag{5}$$

where V_{DS} is the drain-source voltage, and

$$I_0 = q\mu_n n_i u_T \cdot \frac{N_{FIN} A_{body}}{L} \tag{6}$$

with $A_{body} = W_{FIN} \cdot H_{FIN}$ and $A_{body} = \pi \cdot R^2$ for Fin- and nanowire-FETs [16], [17], respectively. μ_n, N_{FIN}, W_{FIN}, H_{FIN}, R and L are the electron mobility, amount of wires or fins, fin width, fin height, nanowire radius and channel length, respectively.

We derive ψ_s from I_D using equations (5) and (6) for each applied bias. Then, using equations (1)-(4) it is possible to construct the trap density as a function of $E - E_v$ from the subthreshold $I - V$ curve. The derivation of the equations above, and a rigorous test of the approach using TCAD simulations, are the topic of a paper in print [18]. In this article we discuss the characterization aspects of the g_m/I_D technique with a particular focus on the accuracy of the obtained results.

III. Experimental

We characterized FinFETs from two fabrication lines to investigate the g_m/I_D method experimentally. The first set of SOI FinFETs, device set I, features an HfSiO gate dielectric with an effective oxide thickness of 1.6 nm and a TiN gate capped with polysilicon. The fin height is 65 nm. For the processing details, see [19].

The second set of SOI FinFETs, device set II, features 150 nm high Si fins, an 11 nm thermally grown SiO_2 gate oxide and a TiN gate capped with polysilicon. The process details are documented in [20].

The devices studied in this paper have the $(1\bar{1}0)$/[110] orientation, *i.e.* a [110] channel transport direction and $(1\bar{1}0)$ oriented sidewalls, as depicted in Fig. 1; and comprise 5 parallel fins (N_{FIN} = 5).

Fig. 2 shows exemplary current-voltage (I_D-V_{GS}) characteristics for various fin and gate dimensions for both sets of devices. The characteristics were recorded with a Keithley 4200 semiconductor parameter analyzer and a Cascade probe station at V_{DS} = 25 mV. For all measurements the temperature T was fixed at 300 K using a low temperature chuck (PM300) of Advanced Temperature Test Systems (ATT Systems). All studied devices had negligible short-channel effects.

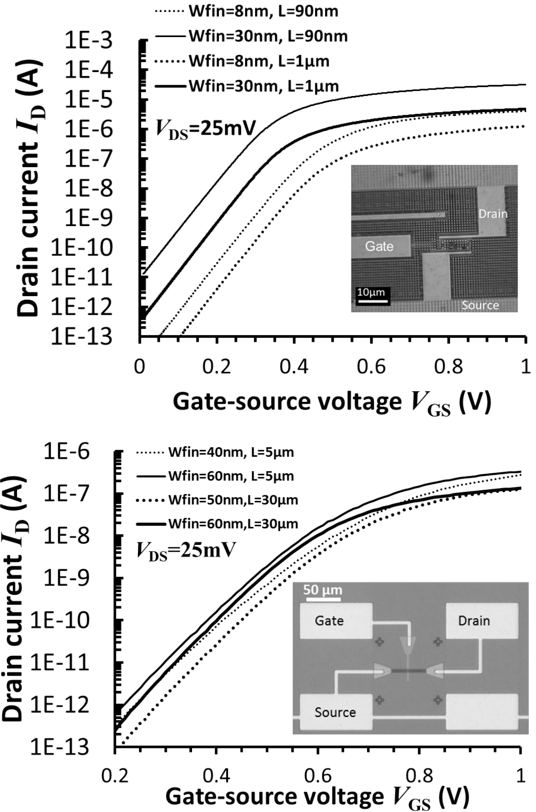

Fig. 2. I_D-V_{GS} characteristics of the fabricated FinFETs (V_{DS} = 25 mV) for various fin widths (W_{FIN}) and gate lengths for (a) device set I and (b) device set II. The insets are optical micrographs of a 5-fin FinFET.

For analyzing the electrical results we used pre-amplifiers which enabled us to measure currents down to the 10 fA range. The step size in V_{GS} was fixed to 0.5 mV ($\Delta V_{GS} = 0.5$ mV). We used a running least squares fit on 41 consecutive measurements, fitting a linear function on ln(I_D) versus V_{GS}, to obtain precise values of g_m and I_D by averaging out measurement noise. From these values the surface potential itself, and the surface potential dependent ideality factor m were computed. Some of these results are shown in Fig. 3.

The results indicate that for device set I the ideality factor $m \approx 1$, and starts to increase from V_{GS} = 0.2 V onwards. For the device set II m is higher, typically starting from around 1.5 and monotonously increasing. The more noisy curves could be

related to the relatively high trap density. Spikes, as visible in Fig. 3b, occur randomly on some devices and are likely a measurement artifact. The curves in Fig. 3 cover mainly the subthreshold regime.

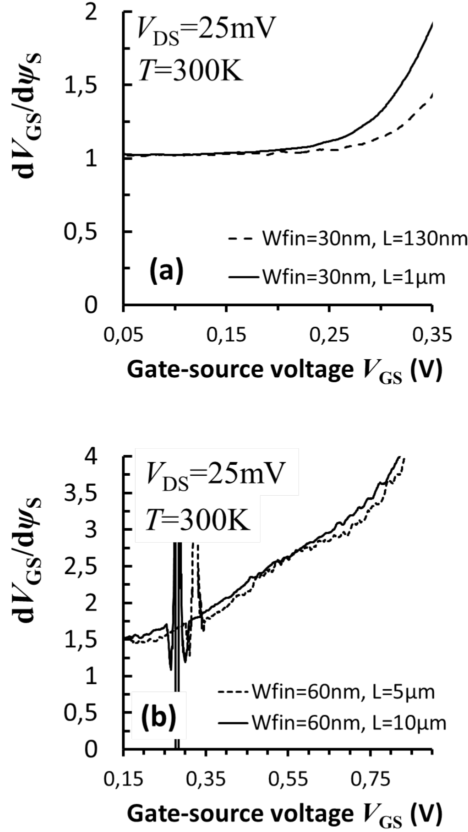

Fig. 3. Extracted ideality factors against V_{GS} for (a) W_{FIN} = 30 nm (device set I), and (b) W_{FIN} = 60 nm (device set II).

For estimating $D_{it}(E)$ equations (2)–(4) have been used as shown in Fig 4. As can be seen traditional bathtub-shape curves have been obtained ranging from around 0.15 eV above mid gap up to the conduction band edge; for the lower energy levels the results appear rather noisy. By plotting the same curves on semilog scale (Fig. 4b) the minimum D_{it} values can be determined which are around $3{\cdot}10^{11}$ $cm^{-2}eV^{-1}$ for W_{FIN} = 20 and 30 nm. For lower energy levels between 0.7 and 0.85 eV the trap density for W_{FIN} = 8 nm could not be measured, indicating lower values.

Fig. 5 shows some results obtained on device set II for a gate length of 5 μm. The results indicate higher D_{it} values than for device set I, irrespective of the gate length (not shown) or fin width. For device set II the technique loses resolution towards midgap due to measurement accuracy, while for device set I it is due to gate-induced drain leakage.

IV. Accuracy of the Method

Measurement errors propagate into the $D_{it}(E)$ determination, and the presented technique is quite sensitive to such errors. In this section we discuss the main causes of erroneous D_{it} determination and their mitigation.

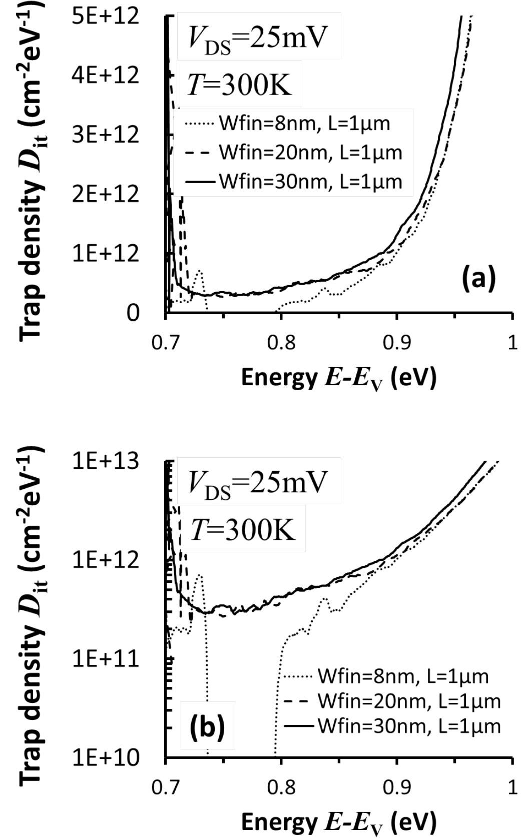

Fig. 4. Extracted trap density D_{it} against the energy $E - E_v$ for device set I using equations (2) and (4). (a) linear scale, and (b) semi-log scale.

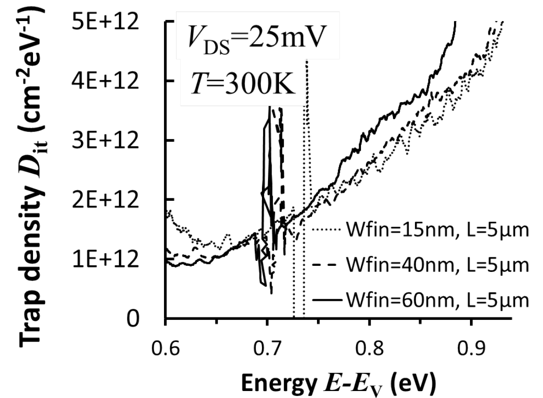

Fig. 5. Extracted trap density D_{it} against the energy $E - E_v$ for device set II using equations (2) and (4). The gate length is 5 μm.

Three parameters require precise determination for the g_m/I_D method to be accurate: the device temperature T, drain current I_D, and transconductance g_m. The D_{it} itself is sensitive to all three; the trap energy $(E - E_v)$ relies on the accurate determination of T and I_D, but is much less sensitive to measurement errors. We therefore focus this discussion on the effect of errors of these three parameters on D_{it} as determined using equations (2) and (3).

From equation (2) and using $g_\mathrm{m} = I_\mathrm{D}/mu_T$ we can derive that an error in I_D measurement, δI_D, leads to an error δD_it following:

$$\delta D_\mathrm{it} = \frac{mC_\mathrm{ins}}{q^2}\frac{\delta I_\mathrm{D}}{I_\mathrm{D}} \approx \frac{mC_\mathrm{ins}}{q^2}\frac{\delta g_\mathrm{m}}{g_\mathrm{m}}. \quad (7)$$

Because I_D and g_m are extracted from the same data points, it is not safe to assume that δI_D and δg_m are uncorrelated. Assuming $m = 1$ and an EOT of 1 nm, a 100-ppm error on the drain current measurement will lead to an error on D_it of 2.2 $\times 10^9$ cm^{-2}eV^{-1}. The same can be stated for the g_m determination. Relative measurement errors in the 100-ppm regime are readily obtained with wafer-level current measurements, also with automatic prober systems (see e.g. [21]). However care must be taken in the low current regime below 1 nA where the accuracy tends to deteriorate. For an accurate determination of interface trap density nearer to midgap, test structures with many parallel fins are therefore recommended, to obtain higher overall subthreshold currents. However such test structures were not available for this work.

Similarly, we find the impact of a temperature error δT to be approximated by:

$$\delta D_\mathrm{it} \approx \frac{mC_\mathrm{ins}}{q^2}\frac{\delta T}{T}. \quad (8)$$

This is a critical factor in the D_it extraction. An error of the device temperature as specified for our PM300 thermochuck, 0.6 K, with the same assumptions as above, leads to an error in the D_it determination of 4.4 $\times 10^{10}$ cm^{-2}eV^{-1}. Clearly, a more accurate temperature-controlled chuck in equilibrium is advised - modern thermo-chuck systems control the wafer temperature better than 0.1 K. Alternatively, the local temperature can be recorded during measurement by different means. Self-heating of the transistor can likely be ignored in the measurement as we work in subthreshold.

As the accuracy of this D_it measurement technique then reaches 10^{10} cm^{-2}eV^{-1} or better, it becomes possible to study single traps in small finFETs (as long as they exhibit long-channel characteristics). We speculate that the $g_\mathrm{m}/I_\mathrm{D}$ technique proposed here can thus be used to study single-trap behavior in more detail, as well as possible D_it variability issues in this type of devices.

Besides experimental accuracy, it is reported in literature that the subthreshold current method becomes inaccurate in case of doping nonuniformity [3], [4] and non-uniform oxide charge [6]. For fully-depleted devices with low body doping the first issue is circumvented. Non-uniform oxide charge may still be a factor of concern.

V. Conclusions

This article presents the characterization aspects of the newly developed $g_\mathrm{m}/I_\mathrm{D}$ method to extract D_it of symmetric fully depleted field-effect transistors from the subthreshold current. Our experimental data show a traditional bathtub-shape like trap density against the energy ranging from around 0.15 eV above mid-gap up to the conduction band edge. An error propagation analysis shows that particular care is required in the device temperature measurement and g_m determination to obtain accurate results. An accuracy better than 10^{10} cm^{-2}eV^{-1} can be obtained with contemporary wafer-level characterization tools.

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