Integration of Solar Cells on Top of CMOS Chips Part I: a-Si Solar Cells

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***Abstract*—We present the monolithic integration of deep-submicrometer complementary metal–oxide–semiconductor (CMOS) microchips with a-Si:H solar cells. Solar cells are manufactured directly on the CMOS chips. The microchips maintain comparable electronic performance, and the solar cells show efficiency values above 7%. The yield of photovoltaic cells on planarized CMOS chips is 92%. This integration allows integrated energy harvesting using established process technologies and, as such, is an important step toward wireless autonomous microsystems (i.e., "smart dust").**

***Index Terms*—Above integrated circuit (IC), amorphous Si (a-Si), complementary metal–oxide–semiconductor (CMOS), energy harvesting, energy scavenging, monolithic integration, photovoltaic (PV) cells, solar cells, ubiquitous computing.**

I. Introduction

UBIQUITOUS computing [1] requires the development of the so-called smart dust [2], i.e., wireless autonomous sensor nodes. One core challenge to such long-lived wireless pervasive systems is their power supply. Cable wiring is prohibitively expensive and impractical. Contemporary batteries can only supply very little total energy (~ 1–3 J/mm^3) until they run out, and their lifetime is anyway limited to 1–3 years [3], [4], which is shorter than the typical physical lifetime of sensors and electronics.

However, some continuously operated integrated circuits (ICs) were reported to draw less power than 1 μW/mm^2 [5]. The time-averaged power consumption can be even lower by running at a low duty cycle. At such power consumption levels, the harvesting (or "scavenging") of energy from the direct surroundings becomes an option. Energy sources include sunlight, wind, electromagnetic fields, temperature gradients, and mechanical vibrations [6].

A comparison of energy-harvesting techniques is presented in Table I. The table is limited to approaches that are likely complementary metal–oxide–semiconductor (CMOS) compatible. This compatibility allows a high level of integration, which is a prerequisite for low-cost mass fabrication. The performance comparison is made per surface area (as in [7]), because CMOS power consumption scales with chip area. The table makes clear that solar cells can provide competitive power levels even in an indoor environment. In addition, an alternating-current-to-direct-current (dc) conversion is required for most alternatives but not for photovoltaics (PVs).

In this paper, we show that a thin-film amorphous-silicon (a-Si) solar cell can be manufactured directly on a CMOS chip. Lu *et al.* [15] describes the first results of such experiments. The monolithic integration of solar cells was presented on top of unpackaged 0.13- and 0.25-μm CMOS dies. Here, the motivation and background considerations are expanded, and ~~an~~ additional experimental detail ~~is~~ given. We also present new experiments on different CMOS generation (0.18 μm), ring-oscillator (RO) test results, and an improved integration process, leading to the better performance of the solar cells on CMOS in terms of efficiency and yield.

II. Choice of Technology

A. Solar-Cell Technologies

On the size scale of microchips, thin-film solar cells can be considered the most mature one of the technologies listed in Table I. They offer both long-term reliability ($>$ 20 years) and low-cost mass production. From the system perspective, their merits include the delivery of dc power and output voltage hardly dependent on the illumination intensity. Last but not ~~the~~ least, the PV power generation will scale with chip area, similar with the power consumption of a chip.

For indoor-light energy harvesting, the choice of solar-cell technology is critical. By employing monocrystalline-silicon (c-Si) solar cells for indoor energy harvesting, researchers found that the indoor efficiency of c-Si is only 10%–40% of outdoor efficiency, due to a mismatch of the c-Si band gap with the indoor fluorescent light spectrum [9], [16]–[18].

In Table II, one can see that c-Si solar cells have relatively poor indoor efficiency. Other technologies such as a-Si or copper–indium–gallium–selenide (CIGS) solar cells can maintain an efficiency value of around 7% under indoor-light illumination.

Other considerations further narrow down the options for solar-cell integration on CMOS. We discarded CdTe-based cells in view of the environmental concerns with cadmium, which might hamper industrialization (the replacement of lead in solder has been a painstaking process in the electronics industry

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TABLE I
COMPARISON BETWEEN (PRESUMABLY CMOS COMPATIBLE) ENERGY HARVESTERS AND THAT BASED ON THE a-Si SOLAR CELL. FOR THE ENERGY HARVESTERS USING MECHANICAL VIBRATION, ONLY THOSE MATCHING GENERAL VIBRATION SOURCES [6] ARE INCLUDED

Harvester	Reference	area (mm^2)	power/area ($\mu W/mm^2$)	Requirements
a-Si solar cell, outdoor	van Veen [8]	13	72	AM1.5 (sunlight)
a-Si solar cell, indoor	Van Veen [8] Reich [9]	13	0.07~0.7	Indoor lighting, 1-10 W/m^2
Piezoelectric	Elfrink[10]	49	0.49	Good frequency match required
Electromagnetic	Jones [11]	99	0.37	
Electrostatic	Arakawa [12]	400	0.015	
Thermo-electric	Böttner [13]	1.12	0.6	Gradient > 5 ºC
Micro-windmill	Holmes [14]	113	0.02	5 m/s wind speed

TABLE II
SOLAR-CELL EFFICIENCY AT OUTDOOR (AM 1.5) AND INDOOR-LIGHT ILLUMINATION CONDITIONS. THE INDOOR LIGHT IS A REDUCED-INTENSITY AM 1.5 SPECTRUM; THE c-Si AND a-Si SOLAR CELLS ARE COMMERCIAL PRODUCTS, AND THE OTHERS ARE LABORATORY SAMPLES. DATA ARE FROM [9] AND [19]

	Bulk solar cells		Thin-film solar cells			
Light intensity	c-Si	GaAs	Photo-chemical	CdTe	a-Si	CIGS
Outdoor 1 kW/m^2	12.5%	12.4%	4.0%	4.7%	7.5%	12.9%
Indoor 10 W/m^2	3.2%	8.7%	4.7%	3.7%	6.7%	7.7%

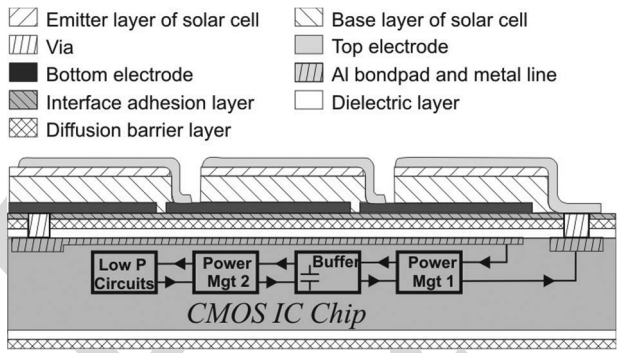

Fig. 1. Envisaged autonomous microchip comprising of a PV cell for energy collection, power management circuits, integrated energy storage (e.g., high-density capacitor or solid-state battery) and low-power circuits. The PV cell can be realized on the chip's front or back side.

[20]). Photochemical-dyed solar cells, as well as the currently known polymer solar cells, have stability concerns over the microsystem's envisaged lifetime [21], [22].

Thus, we ended up with a-Si and CIGS solar cells as the most attractive candidates for the monolithic integration. CIGS-based cells have the highest efficiency among the existing (thin film and monojunction) types, be it at relatively high process temperatures [23]. In addition, a-Si solar cells perform very well at indoor-light-illumination conditions. The a-Si approach can be expanded to create tandem cells for higher efficiency and output voltage. For both CIGS and a-Si technologies, the production equipment is suitable for low-cost monolithic integration on CMOS. The work of CIGS integration on CMOS is presented in Part II.

B. Monolithic Integration

There are two approaches to realize a solar-cell-based energy harvester: hybrid assembly and monolithic integration. Hybrid assembly is off the shelf, allows rapid prototyping, and offers the freedom of using different sizes for the energy-generating and energy-consuming parts.

On the other hand, monolithically integrated devices bear the promise of a smaller overall size and reduced manufacturing cost per system. The existing silicon wafer can be used as the photoconversion medium on bulk silicon [24] or silicon-on-insulator [25]. Our approach is along the "Above-IC" processing philosophy (see, e.g., [26]). By creating a PV cell above an existing IC, the transistor and interconnect density are uncompromised, and freedom of choice appears for the solar-cell technology; note that the indoor efficiency of c-Si cells is limited.

Our work follows up on earlier integration results of a-Si photodiodes on CMOS [27]–[29], which show that a-Si p-n and p-i-n diodes can be successfully integrated in an above-IC approach. However, the current objective is more challenging, although partly the same materials are involved. First, we aim to combine standard CMOS with standard PV processing, assuming that the two may take place in different manufacturing facilities. Second, photodiodes operate in a significantly different environment in terms of temperature, light intensity, and, hence, current density. Finally, in this paper, we show, i.e., both for the CMOS and solar-cell parts, direct functionality comparisons between stand-alone and integrated samples.

Fig. 1 shows the monolithic integration of a solar cell on a chip by "above-IC" CMOS postprocessing. The daisy-chained solar cells convert light into electricity, and the generated power is supplied to the underneath CMOS chips by the vias and aluminum leads. The chip electronics, in addition to the low-power functional circuits, include the energy storage and management modules (common to all energy-harvesting systems). Temporary energy storage can be provided using an integrated high-density capacitor or a solid-state battery. One likely approach (not pursued in this paper) is to employ the upper interconnect layers of the CMOS chip to this purpose. Between the CMOS chips and the solar cell, an intermediate film (or stack of films) is required to serve three purposes: for electrical insulation, to create a diffusion barrier against impurity contamination, and for better adhesion.

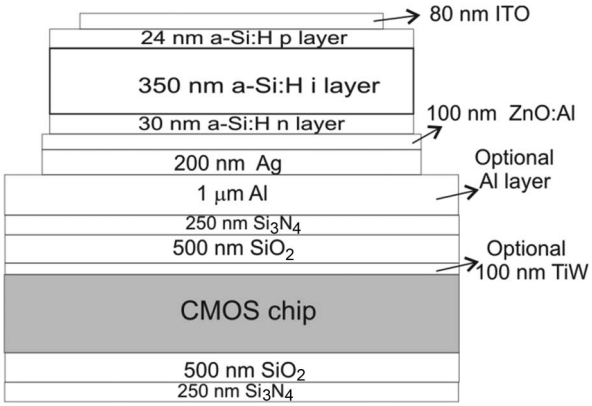

Fig. 2. Schematic view of the a-Si:H n-i-p solar cell on top of a CMOS chip (not to scale).

III. Sample Fabrication

The experimental approach reported in this paper consisted of six steps:

1) the electrical pretest of the CMOS chip;
2) the deposition of chip protection films;
3) solar-cell deposition;
4) solar-cell characterization;
5) removal of the solar cell and the protection films only for Cu process control modules (PCMs);
6) the final electrical test of the CMOS chip.

A schematic cross-sectional view of the realized a-Si:H n-i-p solar cell on a CMOS chip (i.e., after step 4) is shown in Fig. 2. In this section, the sample fabrication is further detailed.

The above procedures were carried out on a variety of CMOS samples from different manufacturers, so as to investigate the generic applicability of our integration approach. The starting substrates were as follows. One type of substrates is the Timepix chip [30]. This is a CMOS chip processed in six-metal 0.25-μm technology utilizing shallow trench isolation and an aluminum interconnect. The second type is a six-metal 0.18-μm CMOS chip with an Al interconnect, where saw-line PCMs with ROs were characterized. The third CMOS generation studied is a 0.13-μm CMOS chip with a copper interconnect. We used PCMs processed up to the first metal. These three types of CMOS substrates are labeled as Timepix, Ringo, and Cu-PCM, respectively, in the remainder of this paper. For reference, the solar cells were also deposited on a surface-textured Asahi U-type SnO:F-coated glass.

To make a fair comparison, a sample holder (see the left side in Fig. 3) was designed to fabricate the solar cells on all three CMOS chips and the glass reference in the same run, with the same process conditions. In addition, one CMOS chip (the Cu-PCM) was positioned upside down, to deposit the solar cell on the back side. The sample holder, including the samples, and the final devices, are shown in Fig. 3.

A. Planarization of the Chip Surface

The glass plates employed in conventional solar-cell production have well-chosen surface roughness. A slightly textured surface is used as it aids in the in-coupling and scattering

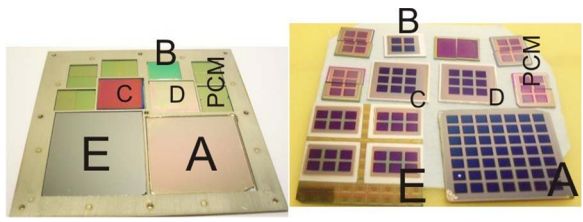

Fig. 3. Realized samples with a-Si solar cells. A, B, C, D, and E indicate the glass-reference plates, Timepix, Cu-PCM (i.e., the solar cell made on the front side and the solar cell made on the back side), and Ringo chips, respectively. The patterning is realized by a stainless-steel shadow mask.

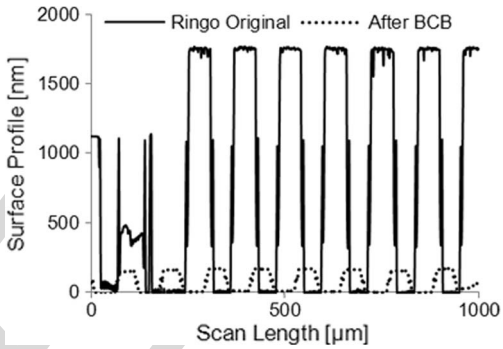

Fig. 4. Surface profile of the Ringo chip before and after the BCB polymer planarization layer.

of incoming light. However, excess roughness will lead to problems with the step coverage of the thin-film stack.

The interconnect of CMOS chips is normally planarized, except for the uppermost layers. Topography exists due to the upper metal layer and the patterned scratch protection layer. We found that the topography on unprepared CMOS chips is too high to be negligible. We also processed solar cells on the backside of CMOS chips; also on that side, considerable topography is found, depending on the pretreatment (such as backlapping).

Earlier work on a-Si solar-cell integration on Timepix and Cu-PCM chips showed no direct impact of roughness on the solar-cell efficiency [15], but the Ringo chips exhibit even higher topography (see Fig. 4). Therefore, we chose to planarize the Ringo-chip surface by benzocyclobutene (BCB) [31]. 2.8-μm BCB was spin coated and then cured in a varying-temperature process peaking at 350 °C. A surface profilometer measurement on the Ringo chip before and after planarization is shown in Fig. 4. Sufficient planarization is achieved, as later confirmed from PV performance measurements (see Section IV-B).

B. Passivation Layer Deposition

Before the solar-cell integration, a proper passivation layer needs to be applied to the chip surface, to prevent the chips from possible damage or contamination. In this paper, an optional 100-nm-thick magnetron-sputtered TiW layer (used later as an etch-stop layer), a 500-nm plasma-enhanced-chemical-vapor-deposited (PECVD) SiO_2 layer, and a 250-nm PECVD Si_3N_4 layer were sequentially deposited on top of the CMOS chips. Another optional 100-nm SiO_2 layer can be used to increase the

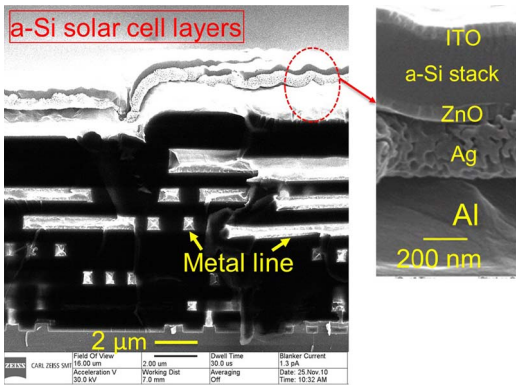

Fig. 5. Helium ion microscopy of an a-Si solar cell fabricated on top of the Timepix chip. The metal lines, via the CMOS chips, and the layer-by-layer structure of the a-Si solar cell on top of the chip can be seen.

adhesion of the solar-cell bottom electrode. On the back side of the chips, only the SiO_2 and Si_3N_4 layers were deposited. The deposition of these layers did not affect the underneath CMOS chip, as verified in dedicated experiments following the same procedure as designed in Section V. After the chip passivation, 1 μm of Al was further deposited as a part of the bottom electrode of the solar cells. This layer is not strictly necessary, but it lowers the series resistance and allows easy probing for current–voltage (I–V) characterization.

C. Solar-Cell Deposition

The a-Si:H solar cells were realized at Utrecht University (UU) using a well-established process, which was detailed in [8]. Briefly, the a-Si:H cell fabrication comprised the following steps. First, 200 nm of Ag and 100 nm of ZnO:Al were deposited by means of radio-frequency (RF) magnetron sputtering, using a multitarget sputter tool. Second, n-type, intrinsic, and p-type a-Si layers were sequentially deposited by PECVD in a multichamber system [32]. The silicon layer thicknesses are 30, 350, and 24 nm, respectively. During the deposition, the processing temperature did not exceed 200 °C. Finally, an 80-nm-thick indium–tin–oxide (ITO) layer was RF sputter deposited as the solar-cell top electrode.

Three process adaptations were made compared with the previous work [15]. The p-type Si layer is now microcrystalline rather than amorphous. The realized samples were optionally annealed at 140 °C in an N_2 ambient for 16 h, and the optional Au grid mentioned in [15] has not been employed for the new experiments, at the expense of solar-cell efficiency, for better comparison. In addition, the active area of the realized solar cells is now 0.16 cm^2 for all samples.

Fig. 5 shows a cross-sectional image of a realized solar cell on a Timepix chip, where the image was obtained with a helium ion microscope [33]. Images taken from the glass-reference cells confirm that the layers are structurally similar.

D. Solar-Cell Deprocessing

After the current density–voltage (J–V) characterization of the integrated solar cells for chips, which needed the electrical characterization again, all the functional and passivation layers were removed from the Cu-PCM chips, to open the bond pads and to enable the electrical testing of the underlying devices (i.e., MOS field-effect transistors (MOSFETs) and MOS capacitors). For deprocessing, an HCl solution was used to remove the ITO, ZnO:Al, and Ag films; a 25% Tetramethylammonium hydroxide solution was applied for etching the a-Si:H layers; Buffered HF was used for removing SiO_2 and Si_3N_4; phosphoric acid (85%) was applied to remove Al metallization; and a hydrogen peroxide solution was used to remove TiW.

On the Timepix and Ringo chips, the solar cells can be kept during CMOS retesting because the solar cells are deposited away from the relevant bond pads using a shadow mask.

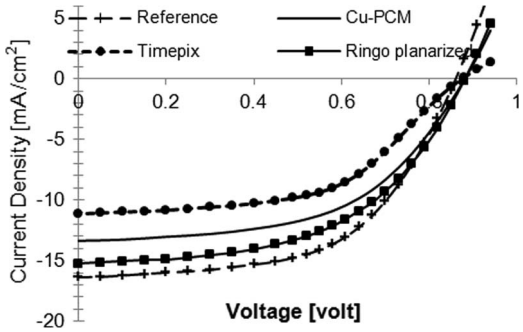

Fig. 6. J–V curves of solar cells with the highest efficiency on the reference sample and on different CMOS chips under AM 1.5 illumination. All solar cells were integrated on the chip's front side.

IV. Experimental Results

In this section, we present the solar-cell performance, including the solar-cell efficiency and yield.

A. PV-Cell Functionality

The J–V measurements have been done at UU to characterize solar cells on the reference glass substrate and the CMOS chips. The measurements were performed under a 100-mW/cm^2 Air Mass (AM) 1.5 condition.

Fig. 6 shows the J–V curves of the solar cell with the best efficiency on the glass-reference cell and the solar cell integrated on the front-side of different generation CMOS chips. Fig. 7 shows the J–V comparison of a solar cell integrated on the same type of a CMOS chip from [15] and this paper. From the J–V curves, the important parameters, i.e., related to the PV performance of the solar cells, were extracted and listed in Table III.

In Fig. 6, it is seen that the current density of the solar cell on glass and CMOS shows proper exponential increase with the bias voltage [34]. In Fig. 7, one can see that there is no S shape around the open voltage V_{oc} anymore compared with [15]. This indicates that our new process using a microcrystalline-silicon p-type layer and an annealing process at 140 °C in N_2 can guarantee an ohmic contact between the functional Si layers and the ITO electrode.

The series resistance R_s of the solar cells in the new experiment is 16 Ωcm^2 (see Table III), which is less than half the value obtained in previous work [15]. The reduction of series resistance is the main contribution of the efficiency improvement of this paper compared with the work in [15].

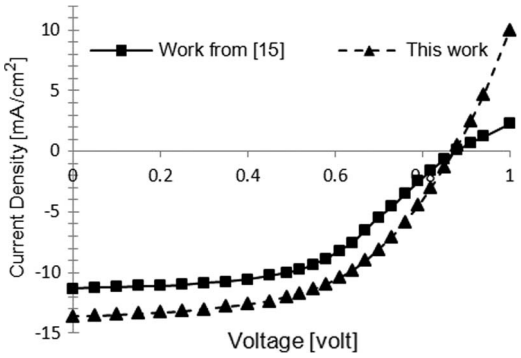

Fig. 7. J–V comparison under AM 1.5 illumination between the earlier work [15] and the new solar-cell experiment. For both runs, the a-Si solar cells are integrated on the back side of the Cu-PCM chip.

TABLE III
PARAMETERS OF a-Si:H SOLAR CELLS ON DIFFERENT SUBSTRATES (ALL THE MEASUREMENTS ARE DONE UNDER AM 1.5 ILLUMINATION AND ALL THE CELLS HAVE AN ACTIVE AREA OF 0.16 cm^2). FOR COMPARISON, THE FIRST FOUR SAMPLES ARE FROM THIS PAPER, AND THE LAST TWO ROWS SHOW THE RESULTS FROM OUR PREVIOUS WORK [15]

Samples	*Efficiency*	J_{sc} mA/cm^2	V_{oc} V	FF	R_s Ω cm^2	R_p Ω cm^2
Glass	7.9%	16.4	0.86	0.56	12	623
Ringo chip planarized	7.1%	15.2	0.88	0.53	14	756
Cu-PCM chip front-side	6.4%	13.4	0.88	0.54	16	784
Cu-PCM chip, backside	6.4%	13.6	0.87	0.54	16	837
Cu-PCM chip, backside [15]	5.2%	11.3	0.88	0.52	44	1324
Timepix, front-side [15]	5.2%	11.1	0.88	0.54	41	748

Table III further shows that the solar-cell efficiency can be well above 5% on different generation CMOS chips. For the BCB-planarized Ringo chips, 7.1% efficiency is achieved. Compared with the earlier work [15], the efficiency gap between glass and CMOS has diminished from 2.8% to less than 1% (BCB planarized). The remaining 1% gap is due to the fact that the reference cells intentionally have a diffusely scattering textured silver back reflector, which enhances the optical light trapping in the device [27], whereas the cells on the CMOS chips have a more specular back reflector. The thickness of the active absorber layer is the same in both cells; hence, the collection performance is the same. For these reasons, on CMOS chips, J_{sc} is lower, whereas the fill factor is the same as for the reference cells. Indeed, from the second column of Table III, we can see that the short-circuit current J_{sc} on glass is higher than that on CMOS chips.

B. Solar-Cell Efficiency and Yield

As discussed in Section III-A, the surface profile amplitude of the CMOS chip is different from that of the glass substrate in our previous work [15]. Fig. 8 shows the surface profile amplitude for the used CMOS chips. Fig. 9 shows the solar cells' best efficiency as a function of the surface profile amplitude. As in [15], the efficiency of a-Si solar cells is not influenced by

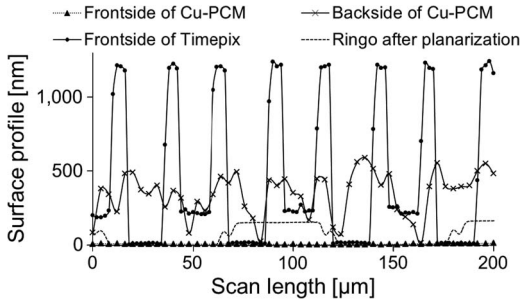

Fig. 8. Surface topography of as-fabricated different-type CMOS chips, which are measured by a profilometer.

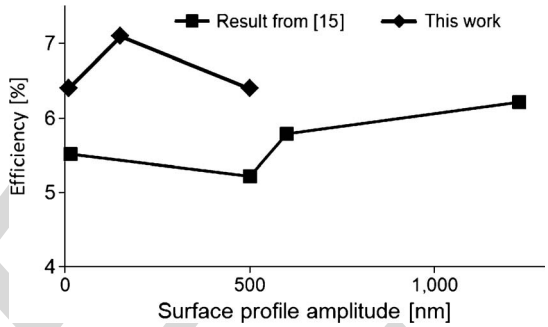

Fig. 9. Efficiency of a-Si:H solar cells deposited on CMOS chips with different surface topography. In both experiments, the a-Si:H solar cell maintains its efficiency on a very rough surface.

TABLE IV
YIELD OF a-Si SOLAR-CELL INTEGRATION ON TOP OF CMOS CHIPS OF DIFFERENT SURFACE AMPLITUDE FROM PREVIOUS WORK [15] AND THIS PAPER. ONLY SOLAR CELLS ON GLASS FROM THE PREVIOUS WORK [15] HAVE AN ACTIVE AREA OF 0.13 cm^2, WHEREAS THE OTHERS HAVE AN ACTIVE AREA OF 0.16 cm^2

Substrate	# cells tested	Surface profile amplitude (nm)	Previous work [15]	Yield This work
Glass	49	250	75%	92%
Ringo	24	150	No data	92%
Cu-PCM backside	9	500	44%	89%
dummy	16	700	19%	No data
Timepix frontside	4	1230	25%	0%

surface profile amplitude, indicating a good step coverage of all solar-cell thin-film layers.

It is well known that the solar-cell yield is related to substrate roughness [35]. In Table IV, the solar-cell yield is summarized. It is clear that, if the surface profile amplitude is less than 500 nm, the yield is hardly influenced. However, for a profile larger than 1 μm, the yield drops down to 25%. The yield of the BCB-planarized samples reached 92% and was closed to that of the textured-glass reference cell. This result also coincides with the findings in [35].

V. CMOS PERFORMANCE AFTER SOLAR-CELL INTEGRATION

In this section, the CMOS functionality after a-Si solar-cell integration is addressed. Capacitance–voltage (C–V) and I–V measurements are reported on the Cu-PCM chips, which is

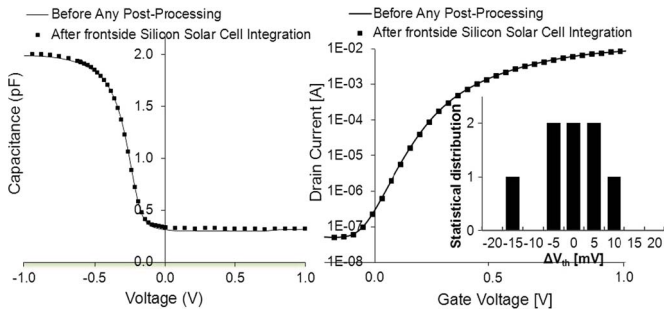

Fig. 10. (Left) Typical C–V curves of a MOS capacitor before and after a-Si:H solar-cell integration on the chip's front side. (Right) I–V curves of an n-channel MOS transistor before and after the same postprocessing. The inset shows the threshold voltage shift statistics of eight transistors.

followed by the tests of the functionality of CMOS ROs and a full mixed-signal CMOS circuit (Timepix).

A. C–V and I–V Measurements on the Cu-PCM Chips

The C–V curves of MOS capacitors and the I–V curves of MOS transistors were measured before and after the solar-cell integration, using a Keithley 4200 SCS at the University of Twente.

The MOS capacitor area was 1.44×10^{-6} cm^2 with a gate oxide thickness of 2.2 nm. All capacitance measurements were carried out at a frequency of 1 MHz. The MOSFET has a gate length of 130 nm. The drain–source voltage was 1 V, and the source and the body were connected to ground for the transistor measurements.

The a-Si solar cell can be integrated on the front or the back side of the Cu-PCM chip, and electrical characterization has been done on both of them. An almost identical performance has been observed for both; therefore, only the results for the front-side integration are shown here.

Fig. 10 shows no visible difference on the C–V curves of the MOS capacitor and the I–V curves of the MOS transistor before and after the solar-cell front-side integration.

From the C–V and I–V curves, the key performance parameters were derived: the gate leakage current and drain saturation current (i.e., $I_{\rm leak}$ and $I_{\rm on}$, respectively, which were both obtained at $V_{GS} = 1$ V), the OFF-state current $I_{\rm off}$, the threshold voltage $V_{\rm th}$, and the subthreshold swing S. The values averaged over eight transistors are shown in Table V. After the solar-cell integration, the changes of all the parameters are small. The most significant shift is observed for the threshold voltage of the front-side integrated solar cell. The absolute average value of this change ($\sim$5 mV) is quite acceptable in view of similar $V_{\rm th}$ shifts encountered after conventional packaging processes [36].

B. Functionality of CMOS ROs

A RO is widely used as a tool to characterize CMOS performance [37]. In our experiments, the power consumption and the output frequency versus the enable voltage of a 17-stage RO have been measured before and after the solar-cell integration by Keithley 4200 SCS and an Agilent/HP 54642A oscilloscope.

TABLE V
MOSFET PARAMETERS BEFORE AND AFTER a-Si:H SOLAR-CELL INTEGRATION ON THE CHIP'S FRONT SIDE (VALUES AVERAGED OVER EIGHT TRANSISTORS)

	Before Processing	After solar cell integration	Absolute change	Relative change
$I_{\rm leak}$ (μA)	17.11	17.16	0.05	0.2%
$I_{\rm on}$ (mA)	8.21	8.39	0.19	2.5%
$I_{\rm off}$ (nA)	745	744	1	0.1%
$V_{\rm th}$ (mV)	-127	-122	5	3.9%
S (mV/dec)	80	80	0	0.0%

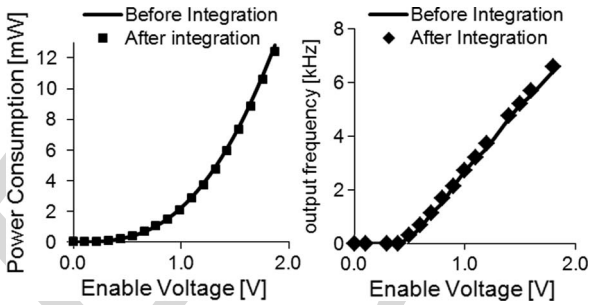

Fig. 11. (Left) Power consumption and (right) output frequency versus enable voltage of the RO before and after the a-Si solar-cell integration. The RO is read out via an embedded 512-times frequency divider.

TABLE VI
DIGITAL AND ANALOG TEST RESULTS OF THE TIMEPIX CHIP BEFORE AND AFTER a-Si:H SOLAR-CELL INTEGRATION ON THE CHIP'S FRONT SIDE

	Digital Testing		Analog Testing	
	Bad columns (out of 256)	Bad pixels (out of 65536)	Bad columns (out of 256)	Bad pixels (out of 65536)
Before integration	8	2127	9	2875
After integration	9	2258	12	4578

The RO includes a 512-times divider to reduce frequency at the output. The results are shown in Fig. 11.

One can observe that there is no significant impact of the integration on the RO performance both in terms of power consumption and oscillating frequency.

C. Functionality of the Timepix Chip

The Pixelman software [38] and an automated probe station were employed for functional testing of the Timepix chips at the Nikhef Institute in Amsterdam, The Netherlands. The program tests the functionality of analog CMOS circuitry arranged in 256 columns of 256 pixels. Each pixel contains 550 transistors. It should be noted that the postprocessed chips were of a lower quality category than those normally used. A fraction of the pixels and columns therefore malfunction before solar-cell integration. A summary of the test results is presented in Table VI.

The number of bad columns for both the digital and analog tests increased marginally; 98.8% of the chip pixels were unaffected by the solar-cell integration. The change is insignificant according to Timepix test experts, on the basis of test repetition experience. Like the findings with Cu-PCM and Ringo chips, the Timepix results indicate the possibility of postintegrating solar cells above standard CMOS circuits.

VI. Conclusion

In this paper, we have successfully integrated a-Si:H n-i-p solar cells on CMOS chips by postprocessing. The solar cells on-chip showed an efficiency value around 7.1% under AM 1.5 irradiation conditions. This efficiency is comparable with that of the glass reference and can be further increased by texturing the underlying CMOS or the solar cell's bottom electrode. The cell yield is equally high on glass and on BCB-planarized CMOS.

For postprocessing, we used unpackaged CMOS chips of three generations. Results are presented on 0.13-μm (Cu-backend) CMOS microchips with PCM test structures, 0.18-μm-technology (Al back end) 17-stage ROs, and 0.25-μm (Al back end) CMOS ICs (Timepix). All three microchips showed unaffected CMOS performance after postprocessing.

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References

[1] M. Weiser, "The computer for the twenty-first century," *Sci. Amer.*, vol. 265, no. 3, pp. 94–104, 1991.

[2] B. Warneke, M. Last, B. Liebowitz, and K. S. J. Pister, "Smart dust: Communicating with a cubic-millimeter computer," *Computer*, vol. 34, no. 1, pp. 44–51, Jan. 2001.

[3] M. Armand and J. M. Tarascon, "Building better batteries," *Nature*, vol. 451, no. 7179, pp. 652–657, Feb. 2008.

[4] V. Pop, H. J. Bergveld, P. H. L. Notten, and P. P. L. Regtien, "State-of-the-art of battery state-of-charge determination," *Meas. Sci. Technol.*, vol. 16, no. 12, p. R93, Dec. 2005.

[5] S. Hanson, Z. Foo, D. Blaauw, and D. Sylvester, "A 0.5 V sub-microwatt CMOS image sensor with pulse-width modulation read-out," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 759–767, Apr. 2009.

[6] S. Roundy, D. Steingart, L. Frechette, P. Wright, and J. Rabaey, "Power sources for wireless sensor networks," *Wirel. Sens. Netw.*, *Lecture Notes in Computer Science*, pp. 1–17, 2004.

[7] R. J. M. Vullers, R. V. Schaijk, H. J. Visser, J. Penders, and C. V. Hoof, "Energy harvesting for autonomous wireless sensor networks," *IEEE Solid-State Circuits Mag.*, vol. 2, no. 2, pp. 29–38, Spring 2010.

[8] M. K. van Veen and R. E. I. Schropp, "Amorphous silicon deposited by hot-wire CVD for application in dual junction solar cells," *Thin Solid Films*, vol. 403/404, pp. 135–138, Feb. 2002.

[9] N. H. Reich, S. Y. Kan, W. G. J. H. M. van Sark, E. A. Alsema, S. Silvester, A. S. H. van der Heide, R. W. Lof, and R. E. I. Schropp, "Weak light performance and spectral response of different solar cell types," in *Proc. 20th Eur. Photovoltaic Solar Energy Conf. Exhib.*, Barcelona, Spain, 2005, pp. 2120–2123.

[10] R. Elfrink, V. Pop, D. Hohlfeld, T. M. Kamel, S. Matova, C. De Nooijer, M. Jambunathan, M. Goedbloed, L. Caballero, M. Renaud, J. Penders, and R. van Schaijk, "First autonomous wireless sensor node powered by a vacuum-packaged piezoelectric MEMS energy harvester," in *IEDM Tech. Dig.*, 2009, pp. 543–546.

[11] P. Glynne-Jones, M. J. Tudor, S. P. Beeby, and N. M. White, "An electromagnetic, vibration-powered generator for intelligent sensor systems," *Sens. Actuators A, Phys.*, vol. 110, no. 1–3, pp. 344–349, Feb. 2004.

[12] T. Tsutsummo, Y. Suzuki, N. Kasagi, and Y. Sakane, "Seismic power generator using high-performance polymer electret," in *Proc. 19th IEEE Int. Conf. Micro Electro Mech. Syst.*, 2006, pp. 98–101.

[13] H. Böttner, J. Nurnus, A. Gavrikov, G. Kühner, M. Jägle, C. Künzel, D. Eberhard, G. Plescher, A. Schubert, and K.-H. Schlereth, "New thermoelectric components using microsystems technologies," *J. Microelectromech. Syst.*, vol. 13, no. 3, pp. 414–420, Jun. 2004.

[14] A. S. Holmes, G. Hong, K. R. Pullen, and K. R. Buffard, "Axial-flow microturbine with electromagnetic generator: Design, cfd simulation, and prototype demonstration," in *Proc. 17th IEEE Int. Conf. MEMS Tech. Dig.*, Maastricht, The Netherlands, pp. 568–571.

[15] J. Lu, W. Liu, C. H. M. van der Werf, A. Y. Kovalgin, Y. Sun, R. E. I. Schropp, and J. Schmitz, "Above-CMOS a-Si and CIGS solar cells for powering autonomous microsystems," in *IEDM Tech. Dig.*, 2010, pp. 31.3.1–31.3.4.

[16] A. Nasiri, S. A. Zabalawi, and G. Mandic, "Indoor power harvesting using photovoltaic cells for low-power applications," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4502–4509, Nov. 2009.

[17] A. Hande, T. Polk, W. Walker, and D. Bhatia, "Indoor solar energy harvesting for sensor network router nodes," *Microprocess. Microsyst.*, vol. 31, no. 6, pp. 420–432, Sep. 2007.

[18] H. Shao, C.-Y. Tsui, and W.-H. Ki, "A micro power management system and maximum output power control for solar energy harvesting applications," in *Proc. Int. Symp. Low Power Electron. Des.*, Portland, OR, 2007, pp. 298–303.

[19] J. F. Randall and J. Jacot, "Is AM1.5 applicable in practice? Modelling eight photovoltaic materials with respect to light intensity and two spectra," *Renew. Energy*, vol. 28, no. 12, pp. 1851–1864, Oct. 2003.

[20] Y. Li, K. S. Moon, and C. P. Wong, "Electronics without lead," *Science*, vol. 308, no. 5727, pp. 1419–1420, Jun. 2005.

[21] A. Hinsch, J. M. Kroon, R. Kern, I. Uhlendorf, J. Holzbock, A. Meyer, and J. Ferber, "Long-term stability of dye-sensitised solar cells," *Progress Photovolt., Res. Appl.*, vol. 9, no. 6, pp. 425–438, 2001.

[22] M. Jørgensen, K. Norrman, and F. C. Krebs, "Stability/degradation of polymer solar cells," *Solar Energy Mater. Solar Cells*, vol. 92, no. 7, pp. 686–714, Jul. 2008.

[23] W. N. Shafarman and J. Zhu, "Effect of substrate temperature and deposition profile on evaporated $Cu(InGa)Se_2$ films and devices," *Thin Solid Films*, vol. 361, pp. 473–477, 2000.

[24] A. J. Mouthaan, "Integrated cascade of photovoltaic cells as a power supply for integrated circuits," *Sens. Actuators*, vol. 5, no. 4, pp. 285–292, Jul. 1984.

[25] O. Bulteel, R. Delamare, and D. Flandre, "High-efficiency solar cell embedded in SOI substrate for ULP autonomous circuits," in *Proc. IEEE Int. SOI Conf.*, 2009, pp. 2.5.1–2.5.2.

[26] J. Schmitz, "Adding functionality to microchips by wafer post-processing," *Nuclear Instrum. Methods Phys. Res.*, vol. 576, no. 1, pp. 142–149, Jun. 2007.

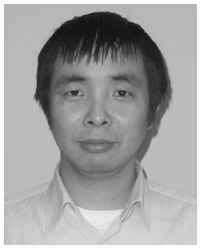
[27] T. Lule, S. Benthien, H. Keller, F. Muetze, P. Rieve, K. Seibel, M. Sommer, and M. Bohm, "Sensitivity of CMOS based imagers and scaling perspectives," *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2110–2122, Nov. 2000.

[28] J. A. Theil, "Advances in elevated diode technologies for integrated circuits: Progress towards monolithic instruments," *Proc. Inst. Elect. Eng.—Circuits, Devices Syst.*, vol. 150, no. 4, pp. 235–249, Aug. 2003.

[29] C. Miazza, S. Dunand, N. Wyrsch, A. Shah, N. Blanc, R. Kaufmann, and L. Cavalier, "Performance analysis of a-Si:H detectors deposited on CMOS chips," in *Proc. Amorphous Nanocrystalline Silicon Sci. Technol.*, 2004, pp. 513–518.

[30] X. Llopart, R. Ballabriga, M. Campbell, L. Tlustos, and W. Wong, "Timepix, a 65k programmable pixel readout chip for arrival time, energy

and/or photon counting measurements," *Nuclear Instrum. Methods Phys. Res.*, vol. 581, no. 1/2, pp. 485–494, Oct. 2007.
[31] K. Paik, H. S. Cole, R. J. Saia, and J. J. Chera, "Studies on metal/benzocyclobutene (BCB) interface and adhesion," *J. Adhesion Sci. Technol.*, vol. 7, no. 5, pp. 403–415, 1993.
[32] R. E. I. Schropp, K. F. Feenstra, E. C. Molenbroek, H. Meiling, and J. K. Rath, "Device-quality polycrystalline and amorphous silicon films by hot-wire chemical vapour deposition," *Philos. Mag. B*, vol. 76, no. 3, pp. 309–321, 1997.
[33] B. W. Ward, J. A. Notte, and N. P. Economou, "Helium ion microscope: A new tool for nanoscale microscopy and metrology," *J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct.*, vol. 24, no. 6, pp. 2871–2874, Nov. 2006.
[34] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. Hoboken, NJ: Wiley-Interscience, 2007, p. 23.
[35] H. B. Li, R. H. Franken, J. K. Rath, and R. E. I. Schropp, "Structural defects caused by a rough substrate and their influence on the performance of hydrogenated nano-crystalline silicon n-i-p solar cells," *Solar Energy Mater. Solar Cells*, vol. 93, no. 3, pp. 338–349, Mar. 2009.
[36] H. Ali, "Stress-induced parametric shift in plastic packaged devices," *IEEE Trans. Compon., Packag., Manuf. Technol. A*, vol. 20, no. 4, pp. 458–462, Nov. 1997.
[37] M. Bhushan, A. Gattiker, M. B. Ketchen, and K. K. Das, "Ring oscillators for CMOS process tuning and variability control," *IEEE Trans. Semicond. Manuf.*, vol. 19, no. 1, pp. 10–18, Feb. 2006.
[38] T. Holy, J. Jakubek, S. Pospisil, J. Uher, D. Vavrik, and Z. Vykydal, "Data acquisition and processing software package for Medipix2," *Nuclear Instrum. Methods Phys. Res.*, vol. 563, no. 1, pp. 254–258, Jul. 2006.



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