Fabrication and properties of GeSi and SiON layers for Above-IC Integrated Optics

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***Abstract*—A study is presented on silicon oxynitride material for waveguides and germanium-silicon alloys for p-i-n diodes. The materials are manufactured at low, CMOS-backend compatible temperatures, targeting the integration of optical functions on top of CMOS chips. Low-temperature germanium-silicon deposition, crystallization and doping are studied for integrated photodetection up to ~1500 nm wavelength. An investigation of the process window for laser crystallization is presented aiming towards the localization control of crystal boundaries and the achievement of crystals larger than 2 micrometer. Further, an inductively-coupled-plasma chemical vapor deposition process is presented for silicon oxynitride manufacturing at 150 °C wafer temperature, yielding low-loss material in a wide optical spectral range. Integration schemes for an optical plane on top of CMOS using these materials are discussed.**

Keywords-CMOS, microfabrication, integrated circuit fabrication, above-IC, post-processing, temperature budget, thermal budget, process integration, integrated optics, MEMS, waveguides, photodetectors, germanium-silicon, silicon-germanium, SiON, PECVD, WDMA.

I. Introduction

The semiconductor industry is adjusting focus towards the so-called "More than Moore" innovation paradigm. By this is meant that microchip progress may not only follow from technology driven progress like miniaturization such as described by Gordon Moore [1], but can also come from the addition of new components and new functions inside the microchip. Examples are the introduction of passive components [2], biosensors [3], spin logic [4] and plasmonics [5], to name a few.

The fabrication sequence where the CMOS electronics is first fabricated (devices as well as multilevel interconnect), then followed by the subsequent fabrication of additional devices on top of this stack, draws particular interest, for its compactness, high performance potential and manufacturing convenience. This approach, dubbed Above-IC or CMOS post-processing, has been pursued since the 1980's [6]. It offers great opportunities for the field of microelectronics [7][8].

The monolithic integration of optical with electrical functions can already boast large commercial successes, such as digital micromirror technology [6] and CMOS active pixel sensors [9]. These examples are application-specific; to offer generic optical functionality in integrated circuits, a platform technology is required with the basic optical and electro-optical building blocks.

In this article we present investigations towards the integration of optical functions on top of CMOS, along the lines discussed in [10]. In particular, we pursue the monolithic integration of an optocoupler: a photonic data connection with electronic input and output (see e.g. [11]). An optocoupler consists of an electrically modulated light source, a light waveguide, and a photodetector. Integrated light sources are beyond the scope of the present article. In this paper, materials for light detection as well as waveguiding are studied, expanding on our earlier publications [12,13]. This article provides additional background information and presents new data to support the choices made in process optimization. We further present and compare integration schemes for these materials in the Above-IC context.

II. Process Integration Scenarios

The light source for integrated optical functions in microelectronics is normally an external (laser) light source [14], as an efficient integrated light source is not yet available in silicon technology. The CMOS substrate is opaque, so the obvious access routes for incoming light are from the side or from above the chip. For example, the integrated optical platform developed by Luxtera and ST [15] currently connects fibers from the top, but the third generation introduces side-connectivity to improve the form factor.

For photodetection we envisage a p-i-n diode as argued e.g. in [16]. Three arrangements can couple waveguides to p-i-n photodetectors: in-plane, detector-first or waveguide-first, as sketched in Figure 1. In the in-plane arrangement of Figure 1a, the quality of the connecting interface between the two is a key point of concern. At this (vertical) interface, it is difficult to control the flatness, the composition and the interface quality when normal microfabrication techniques are used. Issues include the risk of lower-density materials formed during

deposition over a step, contamination of the sidewall during anisotropic etching, process control of the etching angle and sidewall roughness. The presence of highly doped regions close to the waveguide should be avoided

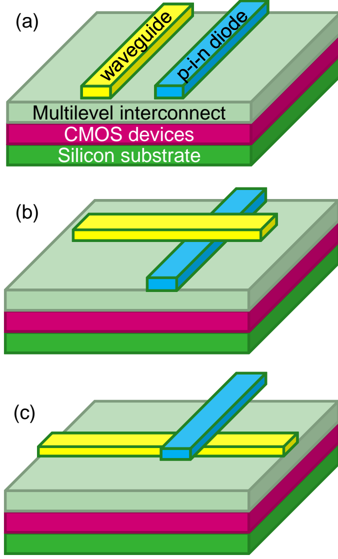


Fig. 1: three arrangements for the integration of waveguides and photodetectors on top of CMOS. (a) in-plane positioning; (b) detector-first arrangement; (c) waveguide-first arrangement.

to prevent absorption of photons to be detected. This limits the possible configurations and particularly complicates the integration of vertical p-i-n stacks.

Detector-first (Figure 1b) or waveguide-first (Figure 1c) then seems a better choice, where the waveguide crosses the intrinsic part of a lateral p-i-n diode. The fabrication of a horizontal interface is generally much better controlled, and is easier modified, e.g. by polishing. As the electronics are at the bottom side and the light source comes from the side or the top, the detector-first arrangement (Figure 1b) seems more convenient to interconnect. In this case, the upper layer of the detector is where most of the photoconversion takes place. This seems an appropriate choice in particular for polycrystalline semiconductor layers, as these commonly have larger crystals and less defects at the upper side, whereas the bottom interface can be rather difficult to control. As an intermediate solution between Figures 1a and 1c, the detector can be fabricated to wrap around the waveguide (see e.g. [17]).

A general consideration in these arrangements is the absorption length of the chosen wavelength in the semiconductor, which determines the geometrical parameters (layer thickness, lateral size). Similarly the dimensions of the waveguide determine the optical modes as well as the confinement of the electromagnetic energy (related to losses). As they critically determine the system performance, ideally, the dimensions of the waveguide and the photodetector are separately optimized. When multiple wavelengths occur in the system (e.g. WDMA), different lateral sizes may be designed to accommodate these.

III. Polycrystalline Germanium Silicon

Silicon is an excellent material for photodetection in the visible range, as exemplified by the success of CMOS active pixel sensor imagers [9]. Above-IC formation of silicon photodiodes was successfully achieved about a decade ago [18,19]. However, silicon becomes transparent in the near-infrared. Germanium detectors are therefore studied as an alternative (see e.g. [17]). Finer tuning of the responsivity is possible using germanium-silicon alloys. This is illustrated by Figure 2, which presents the responsivity of a simple p-i-n diode in Si_xGe_{1-x} alloys as a function of the silicon fraction x. These films are conveniently deposited using low pressure chemical vapor deposition (LPCVD) at CMOS back-end compatible temperatures. Our work focused on the optimization of GeSi alloys with x = 0.85 but the results can be generalized to a broader range of germanium-silicon ratios.

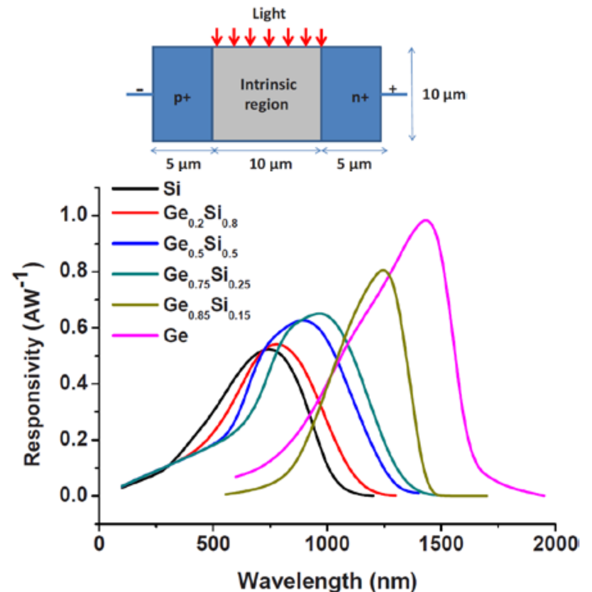


Fig. 2: Room-temperature responsivity of p-i-n photodiodes in monocrystalline germanium-silicon alloy, depending on wavelength and alloy composition, simulated by Silvaco-Atlas (the simulated geometry is depicted in the upper sketch).

P-i-n diodes can either be formed by sequential deposition of in-situ doped layers, or by the deposition of an undoped layer followed by local formation and activation of highly doped n and p regions. In the above-CMOS integration scheme a vertical p-i-n diode seems less convenient, as discussed in section II. Therefore, we consider the formation of lateral p-i-n structures

necessary, and as a result local doping and activation must be pursued.

Given the tight thermal budget constraint in above-IC manufacturing, a furnace or rapid thermal anneal is too hot for the activation of p-type and n-type regions at appreciable doping levels. Therefore pulsed-laser crystallization is employed here to briefly reach a very high local temperature in the GeSi alloy without too much heating of the substrate underneath. By enforcing superlateral grain growth [20,21], sketched in Figure 3, laser crystallization leads to very large crystal grains with a preferred orientation.

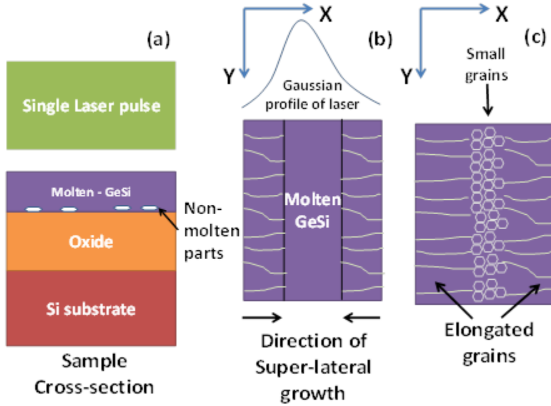


Fig. 3: Schematic sketch showing (a) near-complete melting of GeSi as seen from cross-section where non-molten islands are indicated in white; (b) a top view of super-lateral growth during crystallization after a laser pulse. Two solidification fronts move from the edges of the irradiated region towards the center; (c) a top view of the crystallized film. The elongated grains are separated by a narrow region of smaller-grain material, caused by the spontaneous nucleation of the bulk super-cooled liquid at the center. By scanning the laser, this small-grain region shifts over the wafer.

Grain boundaries in the polycrystalline material lead to reduced conductivity and component variability. To steer the grain location during the crystallization process, a periodic lateral thickness variation was formed orthogonal to the laser scan direction using a GeSi line pattern covered by a blanket GeSi layer. The laser treatment is optimized for sequential super-lateral growth to occur only in between the patterned lines.

The process window was determined by systematically varying the process parameters (laser beam width, pulse energy, pulse overlap) and physical analysis of the samples, mostly by scanning electron microscopy, electron backscatter diffraction (EBSD) and sheet resistance measurements, as detailed in [12]. A typical EBSD image of the obtained polycrystalline material is shown in Figure 4. Note the periodicity in the main grain boundaries running vertically, at positions dictated by the GeSi line pattern. The finally obtained films exhibit crystalline grains much larger than the GeSi film thickness of 100-150 nm, as depicted in Figure 5, characteristic of superlateral growth.

Fig. 4: Exemplary grain orientation map of a laser-crystallized 100-nm $Ge_{0.85}Si_{0.15}$ film on SiO_2, characterized by electron backscatter diffraction during top-view SEM imaging. (Colors indicate grain orientation as indicated in the legend). The laser beam scanned this sample in the vertical direction, leading to the formation of elongated crystal grains.

The films were B, P and As-doped by ion implantation. After laser crystallization, resistivities in the tens of mΩ.cm were achieved with all three impurities, corresponding to active doping concentrations around 10^{19} cm^{-3}. This completes the material engineering necessary to fabricate GeSi photodetectors at CMOS-backend compatible substrate temperatures.

IV. SiON Waveguides

A waveguide's most important property is its optical transparency. We chose to study a material that is transparent in a wide spectral range from visible to 1800 nm, and with a refractive index considerably higher than 1.46 (SiO_2, used in the CMOS intermetal dielectric stack). Amorphous silicon, a well-studied material for waveguiding, is then excluded as it strongly absorbs light at visible wavelengths. Silicon nitride and silicon oxynitride (SiON) with a small oxygen fraction meet these requirements and their integration with CMOS processing is well mastered.

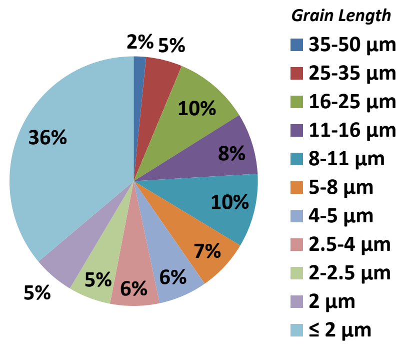


Fig. 5: Distribution of grain sizes in the optimized laser-crystallized film.

The traditional deposition techniques for SiON in microfabrication are LPCVD and plasma enhanced chemical vapor deposition (PECVD). In either case, a high temperature is required to obtain low optical losses: in LPCVD, the deposition temperature is typically 800 °C [22]. PECVD allows deposition well below 450 °C; however, plasma-deposited films have a high hydrogen content in the form of Si-H and N-H bonds. Since these bonds cause high optical losses at wavelengths around 1500 nm [23], an annealing step at temperatures between 1000-1150 °C is commonly applied for hydrogen removal [24-26]. Alternatively, for ultra-thin films (~10 nm) plasma post-treatment at 300 °C was shown to reduce the hydrogen content [27].

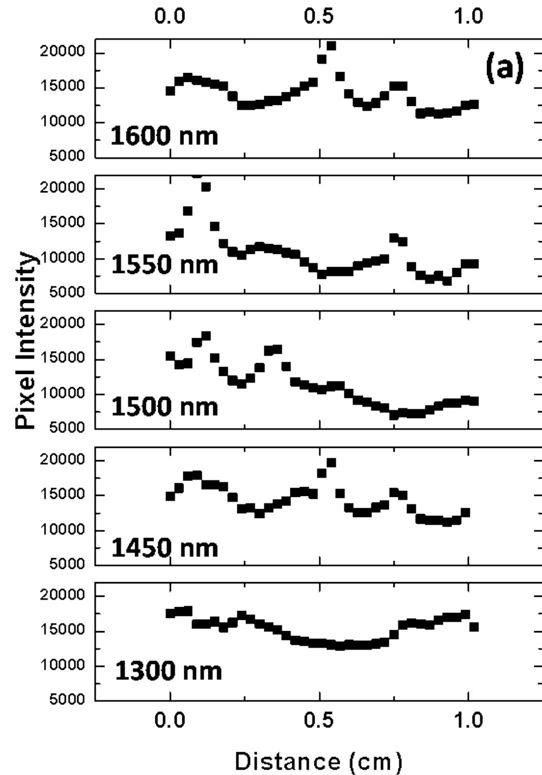
An additional consideration is that any layer stacked on top of CMOS should cause limited mechanical stress to avoid damage to the chip. It has been shown [28] that the mechanical stress in PECVD silicon oxynitride films can be lower compared to PECVD silicon nitride. The refractive index of silicon oxynitride (or SiON) is tunable from 1.46 (SiO_2) to 2.02 (Si_3N_4) [28] (both values are for 632 nm wavelength).

In this work, we use inductively-coupled PECVD (ICPECVD) at 150 °C to deposit silicon oxynitride films. High density PECVD is known to provide better quality films compared to conventional PECVD. Earlier work in our group had shown that ECR plasma depositions of SiO_2 and Si_3N_4 around room temperature led to films with very low hydrogen content [29,30]. This was followed by deposition of high quality silicon dioxide at 150 °C using ICPECVD [31] with the same deposition system as in the present work.

In a series of deposition experiments, we found a process window for high-quality silicon nitride films with approximately 5% oxygen content, SiON, at 150 °C. To obtain good-quality material (with high refractive index and low optical losses) at such low temperatures, it proved essential to use a high-density plasma with a large $Ar:N_2$ ratio, as detailed in [13].

The layers were deposited on 4” silicon wafers covered with 8 µm thermally grown SiO_2. Transverse-electric (TE) polarized light either from a 1300-nm laser diode or a tunable laser (1450-1600 nm) is coupled into the SiON film (acting as slab waveguide) by a prism. The scattered light of the propagating fundamental TE mode is captured by a digital infrared camera across the diameter of the wafer. The losses are determined from the captured images, as depicted in Figure 6.

The obtained losses were typically around a factor 3 better than prior art, as detailed in Figure 7, without any post-deposition anneal. Materials analysis has shown that



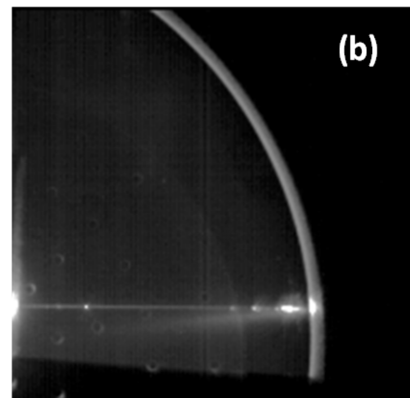


Fig. 6. (a) The propagation of light measured in terms of pixel intensities over 1 cm distance; (b) an example of an image captured using the prism coupling set up with infrared camera.

the deposited films have a negligible concentration of Si-H and N-H bonds, explaining these lower losses

compared to LPCVD and PECVD materials published in literature. The recorded losses are sufficiently low for several optical functions, definitely for infrared optocoupling. A 0.25-µm CMOS chip covered with the optimized SiON film showed unaffected digital and analog performance [13].

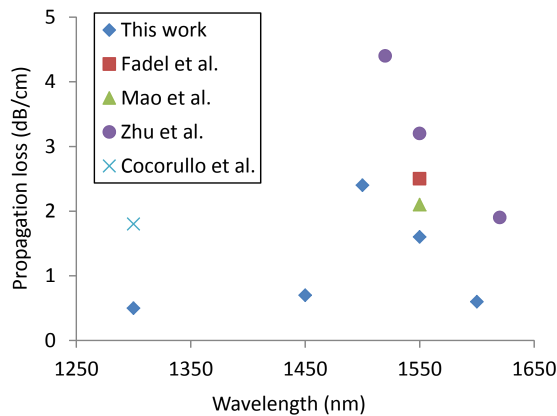


Fig. 7. Experimentally achieved SiON waveguide losses measured by the prism coupling technique and benchmarked against earlier works [32-35] including a-Si and Si_3N_4 waveguides.

Waveguiding above CMOS is far from straightforward, as the electromagnetic energy should be well contained within the waveguide itself to achieve high propagation lengths. This in turn requires a high refractive index of the waveguide's core material. In addition, claddings can assist in the confinement of the optical modes, so that absorption in the structures around (in particular: underneath) the waveguide is suppressed. Silicon nitride has a convenient refractive index around 2.0, well above that of the materials used in CMOS intermetal dielectrics. Given that the metallization stack in modern integrated circuits is several micrometers thick, the existing intermetal dielectric could serve as a lower cladding layer to separate the waveguide from the lossy substrate. (Low-k dielectrics may help to improve the vertical optical insulation.) Metal lines, as well as CMP tiles in the metal layers [36] should be avoided in the near vicinity of the waveguide for undisturbed light propagation. And finally, patterning with very low edge roughness is required for low-loss waveguides; therefore in practice higher losses can be expected than the values obtained by slab waveguide measurements as our data in figure 7.

V. Conclusions

Two material systems are treated in this paper, SiON and GeSi, for their application in microsystems with an integrated-optics plane on top of CMOS. For both, we have shown that excellent optical and electrical properties can be obtained while maintaining a low substrate temperature (to preserve CMOS functionality). The choice for SiON and GeSi offers freedom of compositional tuning towards the application (mainly through the O:N and Ge:Si ratios). Prospects of this microsystem approach lie in the further miniaturization of systems with a combination of optical and electronic functionality.

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