

# MOSFET Degradation under RF stress

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**Abstract**—We report on the degradation of MOS transistors under RF stress. Hot-carrier degradation, NBTI and gate dielectric breakdown are investigated. The findings are compared to established voltage- and field driven models. The experimental results indicate that the existing models are well applicable into the GHz range to describe degradation of MOS transistors in an RF circuit. The probability of gate dielectric breakdown rapidly reduces at such high stress frequencies, offering added design margin for RF power circuits such as power amplifiers for mobile communication.

**Index Terms**—CMOS, RF, RF CMOS, dielectrics, breakdown, reliability, device reliability, hot carrier degradation, NBTI, dielectric breakdown

## I. INTRODUCTION

The understanding of MOS transistor degradation under user conditions is critical for supplying the market with reliable integrated circuits. Accelerated lifetime tests and degradation models have been successfully developed and applied for advanced CMOS. However, these models describe the performance evolution under dc or low-frequency stress, and are typically verified up to  $\sim 10$  MHz. For use in RF circuits, the applicability of these degradation models under RF stress conditions should be known up to a few GHz. Some authors have compared DC stress conditions to AC conditions (see e.g. [1]), but RF stress is only marginally addressed in literature.

This stems mainly from the difficulty to perform accurate reliability experiments at frequencies exceeding 10 MHz. Models describing MOS degradation under electrical (and thermal) stress are voltage or electric-field based. Verification of these models at higher frequencies thus calls for the generation of well-defined RF voltage signals. In [2] we presented a method of generating well-defined RF voltage signals for on wafer experiments. This method allows us to perform a large variety of different RF reliability experiments, without the need of designing test structures for every individual experiment. Only one generic test structure is required.

Using this technique, we were able to perform a large amount of experiments to compare the degradation of MOSFETs under RF stress conditions to degradation under AC stress conditions with frequencies below 10 MHz. In this paper we will show results concerning hot-carrier degradation, NBTI and gate dielectric breakdown.

The following section will present the experimental approach in more detail. Then, the three degradation mechanisms are studied separately in sections III-V. The paper concludes with recommendations for reliable RF CMOS design.

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## II. METHODOLOGY

The key idea of the methodology applied in this paper is to make use of sinusoidal shaped voltage signals. The benefit of using sinuses is twofold:

- 1) Stress conditions are comparable for all frequencies, therefore duty cycle corrections are not needed.
- 2) Sinusoidal voltage signals are relatively easy to generate, thereby allowing the use of Vector Network analyzers (VNAs) to generate stress voltages.

A VNA is capable of measuring the power of the incoming and reflected power waves in an RF measurement setup. If the absolute power level is also known, the voltage waveform at the device under test can easily be determined.

In the methodology used in this paper we connect the VNA in a one-port setup, thereby generating the desired voltage level at one of the signal pads of the device under test (DUT). In [2], [3] we explained the necessary calibration steps that allow to relate the measured power waves at the signal ports of the VNA to the voltage level at the DUT. The technique was then successfully applied to carry out charge pumping measurements at RF [3]. In the latter paper we also presented experimental evidence for the accuracy of the voltage levels generated. In order to determine whether signal distortion due to the nonlinearities of the input impedance of the DUT is negligible, the expected voltage waveform can be calculated from the measured input impedance of the DUT over the entire voltage range of interest.

In digital CMOS, the duty cycle encountered in normal operation usually relaxes the degradation situation compared to worst-case lifetime estimates. However, in RF circuits voltage signals exceeding nominal supply voltage are no exception, especially in power amplifiers (PA's) [4]. The reliability of these circuits therefore deserves special attention. This paper reports on hot-carrier degradation in nMOS transistors (as pMOS devices are more robust against this degradation mode); on NBTI in pMOS transistors (NBTI is negligible in nMOS devices); and on gate dielectric breakdown on nMOS transistors. Due to their higher current driving capabilities, nMOSFETs are preferred over pMOSFETs in RF PA design. For this reason gate dielectric breakdown under RF stress is of most relevance in nMOSFETs.

A Rohde & Schwarz ZVB 20 Vector Network Analyzer generates the RF voltage, an HP4156A semiconductor parameter analyzer is used for the DC biasing and measurements. All devices used were laid out in a ground-signal-ground configuration, optimized for RF measurements. The gate was connected to one signal pad and the drain to the other. The source was tied to the substrate and connected to the ground plane. The devices were connected on-wafer using Suss  $|Z|$  probes. The equipment was connected to a PC through an

IEEE 488 bus. The measurement procedure was controlled using Labview software.

### III. RF HOT CARRIER DEGRADATION

#### A. DC and AC models for hot carrier degradation

Hot carrier degradation occurs in MOS transistors due to highly energetic charge carriers flowing in the MOSFET channel. The carriers cause physical damage and charge trapping, leading to a change of device parameters such as the threshold voltage. This effect has been widely discussed in literature (see e.g. [5]). The effect can be observed in both nMOSFETs and pMOSFETs; nMOS device degradation is most significant.

The hot carrier degradation rate depends on the drain and gate voltages. For nMOSFETs with channel lengths  $> 0.25 \mu\text{m}$ , hot carrier degradation is severe in three different regions of gate bias voltage [6]. In more advanced devices with channel lengths below  $0.25 \mu\text{m}$  the maximum degradation rate shifts to high gate voltage levels ( $V_G \cong V_D$ ), attributed to the increasing importance of electron-electron scattering [7].

The occurrence of different modes of hot carrier degradation at different gate voltage signals makes the lifetime prediction of AC and RF circuits challenging. In [8] a theoretical analysis is given of RF to DC lifetime ratios under such stressing conditions. When comparing AC hot carrier degradation to DC degradation Mistry et al. showed that use can be made of quasi-static assumptions [9]. The same work shows how all occurring hot carrier degradation mechanisms can be considered to accumulate following a Matthiesen-like relation. No frequency dependence would be expected in that case.

Early reports indicating that AC hot carrier degradation rises with increasing frequency were explained by Bellens et al. as a measurement artifact [10]. They showed that the self inductance in the measurement cables can cause large voltage overshoots. This finding stresses the importance of generating well-defined voltage levels for performing AC reliability experiments. For AC hot carrier experiments up to 10 MHz this signal distortion due to cable inductance can be overcome by adding a large parallel capacitor to the drain [10]. For higher frequencies additional effects such as signal distortion due to impedance mismatch come forward.

To circumvent these measurement issues, several research groups use integrated circuits to generate on-chip frequencies exceeding 100 MHz to stress a device [11], [12], [13], [14]. These self-stressing structures typically contain oscillator and inverter circuits to generate on-chip high frequency stress signals. Using these structures, hot carrier experiments with inverter switching frequencies up to 369 MHz were already reported as early as 1994 [14]. None of these experiments revealed unexpected effects occurring during AC stress. Presti et al. [15] recently showed hot carrier degradation results for an nMOS transistor operating at 1.9 GHz. But, while effective for evaluating the given exemplary PA, Presti's approach prevents an accurate comparison with lower frequency signals.

When performing RF hot carrier experiments it is important to realize that the highest voltage signals occur at the drain side of the devices, if the devices are used in PA's. We therefore investigate RF hot carrier degradation with an AC

drain voltage while keeping the gate voltage constant. This is different from earlier AC hot carrier experiments where the behavior of digital circuits was mimicked. For these experiments an AC gate voltage with constant drain voltage could better describe actual circuit behavior.

Of course, in real RF PA's the gate voltage will not be perfectly constant, as otherwise no amplification of any RF signal would take place. This effect may be neglected to first order because the gate voltage amplitude is relatively low combined with the fact that maximum damage occurs at maximum drain voltage.

#### B. Measurement setup for hot carrier degradation

In figure 1 a schematic illustration of the measurement setup is given. The instrument details are given in Section II. Measurements were performed on devices in two different

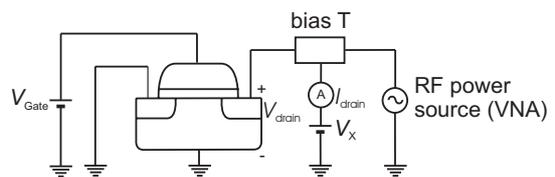


Fig. 1. Schematic drawing of the RF hot carrier measurement setup.

technologies. The type A devices were 90 nm process devices and the type B devices were processed in a  $0.13 \mu\text{m}$  process. The type A devices have a gate channel length of  $0.10 \mu\text{m}$  and the total gate width is  $120 \mu\text{m}$ , consisting of 4 identical cells each having 6 gate fingers of  $5 \mu\text{m}$  wide. The type B devices have a channel length of  $0.13 \mu\text{m}$ . The total gate width is  $192 \mu\text{m}$ , consisting of 8 identical cells each having 8 gate fingers of  $3 \mu\text{m}$  wide.

In the experiments a DC voltage was applied to the gate, while an RF voltage was generated at the drain port. The devices are biased in inversion. This poses an extra difficulty in generating well-defined RF voltage signals: the impedance seen by the RF power source can become very low and has a strong dependency on the drain voltage.

It is important to guarantee that the hot carrier degradation during stress can not be attributed to the DC component of the stress signal. This can be guaranteed with a large-signal drain voltage. Very little degradation is then expected at the low part of the drain voltage cycle, while fast degradation may occur when the drain voltage is high. This approach was verified by testing the DC hot carrier degradation of same-type devices at several drain biases.

The drain voltage amplitude is limited by harmonic distortion, originating because the impedance seen at the drain depends strongly on the drain voltage. Therefore a signal integrity analysis, as discussed in section II was done before any RF hot carrier experiment was performed, at the highest frequency used in the experiments, i.e. 3.2 GHz. The amplitude was kept low enough to keep harmonic distortion at a negligible level.

The bias conditions lead to a considerable DC drain current. Figure 1 shows that the DC component of the drain voltage is

set using  $V_X$ , which is connected to a bias Tee. The bias Tees used during the measurements were the internal bias Tees of the VNA, connected at its DC biasing ports. This connection caused an extra parasitic series resistance of approximately  $7 \Omega$ . With DC drain currents flowing in the order of 100 mA to 300 mA, this may cause a DC voltage drop between  $V_X$  and  $V_{D, \text{drain}}$  of 0.7 to 2.1 V. To account for this, we measure the DC relation between  $V_X$  and  $V_{D, \text{drain}}$  prior to any measurement, and use this to apply a corrected  $V_X$  bias.

### C. Hot carrier measurement results

In figure 2 device parameter degradation is plotted against the frequency of the stress signal for the type A devices. The stress signal consisted of a DC gate voltage of 2.5 V, while the drain voltage signal was sinusoidal between 1.5 and 2.5 V. The hot carrier stress was periodically interrupted, to measure  $V_T$  and  $I_{D, \text{sat}}$ .  $V_T$  was obtained by measuring  $I_{D, \text{drain}}$  as a function of  $V_{\text{Gate}}$  with  $V_X$  set to 0.1 V and using the maximum-derivative extrapolation method of [16].  $I_{D, \text{sat}}$  was defined as the DC drain current with  $V_{\text{Gate}}$  set to 1.2 V and  $V_X$  set to a value corresponding to a  $V_{D, \text{drain}}$  of 1.2 V. Figure 2 indicates

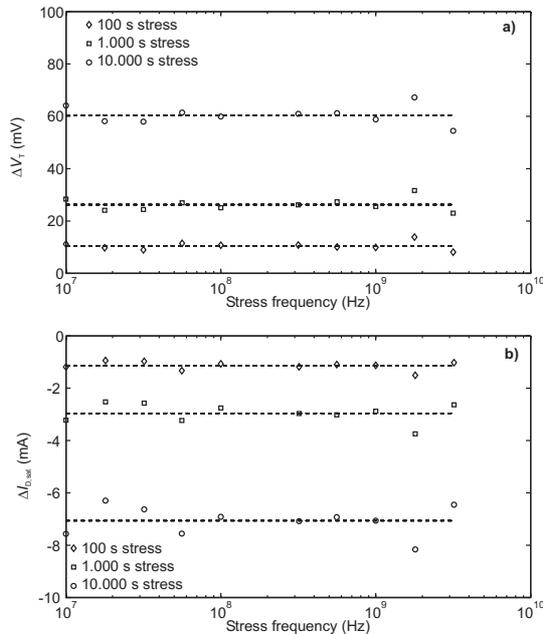


Fig. 2. Hot carrier degradation of  $V_T$  (top) and  $I_{D, \text{sat}}$  (bottom) as a function of frequency for the type A devices. The drain voltage signal is sinusoidal between 1.5 and 2.5 V. The gate voltage was 2.5 V during all stress measurements. Degradation levels are plotted after 100 s, 1,000 s and 10,000 s of stress. The dashed lines are meant as a guide to the eye.

that between 10 MHz and 3.2 GHz the frequency of the stress signal has no influence on device parameter degradation for the type A devices.

The results presented in figure 3 show the device parameter degradation as a function of stress time for the type A devices. The solid lines in figure 3 show the best fit over all data points assuming a power law relation. For this technology, the time exponent  $n$  was found to be 0.41 respectively 0.39 for the average degradation in  $V_T$  and  $I_{D, \text{sat}}$ . These values are typical for the time dependence of hot carrier degradation.

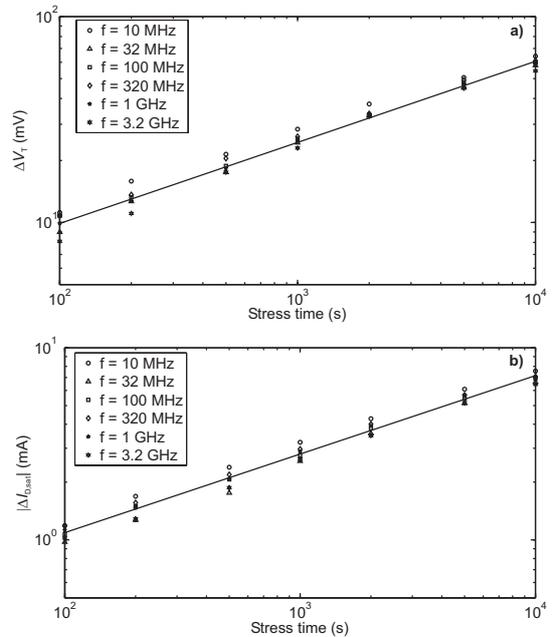


Fig. 3. Hot carrier degradation as a function of time for the type A devices. The stress consisted of a constant gate voltage of 2.5 V and the drain voltage signal varied between 1.5 and 2.5 V. The frequency of the drain voltage signal was varied. In a)  $V_T$  degradation is shown and in b)  $I_{D, \text{sat}}$  degradation. The solid lines show the degradation as a function of time using the average time exponent of 0.41 respectively 0.39 for figures a) and b).

Similar experiments were performed on the type B devices where the stress signal consisted of a gate voltage of 1.5 V and the drain voltage signal varying sinusoidally between 1.0 and 2.6 V. The frequency was varied from 10 MHz to 3.2 GHz. Again, no frequency dependence is found, and the power law time exponent was found to be 0.45 respectively 0.42 for  $V_T$  degradation and  $I_{D, \text{sat}}$  degradation.

From RF hot carrier measurements on 90-nm and 130-nm nMOS transistors, we conclude that no frequency dependence exists in the amount of hot-carrier degradation, as monitored in  $V_T$  and  $I_{D, \text{sat}}$ . This is in line with the existing physical models of hot-carrier degradation. The experimentally validated range of the existing models is as such extended with an order of magnitude, from the earlier 369 MHz [14] up to 3.2 GHz. This verification is very important for predicting circuit lifetime based on known voltage waveforms, such as the work presented in [8].

## IV. RF NBTI DEGRADATION

### A. DC and AC models for NBTI

Negative Bias Temperature Instability (NBTI) is a degradation mode of MOS transistors under negative gate stress at elevated temperatures. It leads mainly to a gradual threshold voltage shift, related to charge trapping in the gate dielectric. The phenomenon is recently reviewed [17]. It is more disturbing in pMOS than in nMOS transistors. Its characterization and modeling are troubled by recovery effects occurring directly after stress. The translation of DC to AC degradation is not straightforward due to these recovery effects.

Similar to hot carrier degradation, NBTI parameter shift as a function of time follows a power law. Recent literature has

revealed a typical value for the time exponent  $n$  of 0.16-0.17. This value can be obtained if parameter degradation is measured without removal of the stress signal, using for instance the on-the-fly technique of Huard [18]. If recovery effects are not properly taken care of, like in conventional stress-measure-stress approaches, higher values of  $n$  around 0.25 may be found.

NBTI degradation under AC stress conditions has been discussed in various papers. Controversy exists on the presence of a frequency dependent component in NBTI. Alam et al. claim that on the basis of the reaction-diffusion model no frequency dependence should be found [19]. Other authors claim that the recovery mechanism can be completely or partly be attributed to the detrapping of holes in deep oxide traps [18], [20]. Under this assumption some frequency dependence may be expected.

Experimental results concerning AC NBTI degradation reflect a similar disagreement on the frequency dependence of AC NBTI degradation. Different papers show a clear frequency dependence of NBTI degradation [21], [22], [23], [24], [25], [26]. It has also been claimed that only the formation of positive oxide charge contributes to any frequency dependency, while interface state generation is frequency independent [27]. Others have experienced no frequency dependence at all for AC NBTI degradation [28], [29], [30].

The frequency range discussed in these papers generally does not exceed the MHz range. Only in [26], [30] NBTI degradation under RF stress conditions is discussed. In [26] use is made of a ring oscillator circuit and device parameter degradation is monitored indirectly using degradation in the oscillation frequency. The approach in [30] on the other hand allows direct extraction of  $V_T$  shifts. In [30] no frequency dependence of NBTI degradation was reported in the entire frequency range from 1 Hz to 2 GHz. On the contrary, in [26] degradation at 100 MHz and 3 GHz was found to differ. In this section additional experimental results will be presented that may shed more insight on any frequency dependence of NBTI under RF stress conditions.

### B. Measurement setup for NBTI

RF NBTI measurements were performed using the measurement setup as shown in figure 4. The instrument details are given in Section II. RF voltage signals were superimposed on

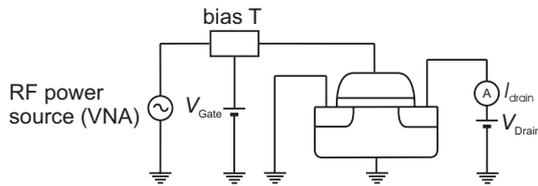


Fig. 4. Schematic drawing of the RF NBTI measurement setup.

the DC voltage  $V_{Gate}$  through the use of a bias Tee. During stress  $V_{Drain}$  was set to 0 V.

Measurements were performed on pMOSFETs in two different technologies. The type C devices were processed in a 90 nm node process and the type D devices were pMOSFETs processes in a 0.13  $\mu\text{m}$  process. The type C devices have a gate

channel length of 0.10  $\mu\text{m}$  and the total gate width is 120  $\mu\text{m}$ , consisting of 5 identical cells each having 8 gate fingers of 3  $\mu\text{m}$  wide. The type D devices, have a gate channel length of 0.13  $\mu\text{m}$  and the total gate width is 192  $\mu\text{m}$ , consisting of 8 identical cells each having 8 gate fingers of 3  $\mu\text{m}$  wide.

RF NBTI measurements were performed using a stress-measure-stress procedure in which the sinusoidal stress voltage signal is periodically interrupted. To limit recovery effects, device degradation was monitored using only one device parameter,  $V_T$ .  $V_T$  was obtained following [16] from a DC  $I_{Drain}-V_{Gate}$  curve with  $V_{Drain}$  set to 0.1 V. A few seconds pass between stress and measurement.

The chuck temperature used in the experiments was 125  $^{\circ}\text{C}$ . The stressing gate voltage  $V_{pp}$  was 3 V for the type C devices and 2.5 V for the type D devices. The DC bias  $V_{Gate}$  was -1.5 V for the type C devices and -1.25 V for the type D devices.

### C. Measurement results for NBTI

The frequency dependence of NBTI degradation is investigated in the frequency range from 10 MHz to 3.2 GHz. In figure 5,  $V_T$  degradation is plotted against stress frequency for the type C and type D devices.

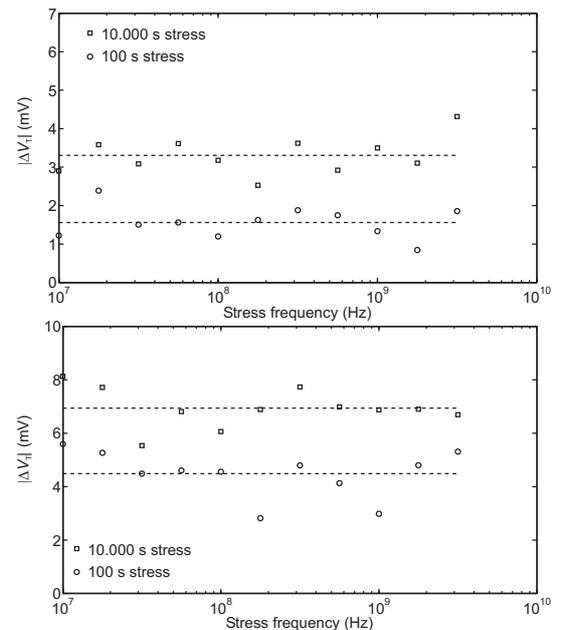


Fig. 5. Top:  $V_T$  degradation plotted against frequency for RF NBTI stress on the type C devices. The stress signal consisted of a constant gate voltage of -1.5 V superimposed on a sinusoidal voltage signal with  $V_{pp} = 3$  V. Bottom:  $V_T$  degradation for type D devices after RF NBTI stress. The gate stress is biased at -1.25 V superimposed on a sinusoidal voltage signal with  $V_{pp} = 2.5$  V. All measurements were performed at 125  $^{\circ}\text{C}$ . The dashed lines are drawn to guide the eye.

Although both figures show some spread on the data, a clear trend is visible: NBTI degradation has no observable frequency dependence. This observation is in agreement with the theory of [19] and the experimental results presented in [28], [29], [30].

The time dependence of NBTI degradation under RF stress is displayed in figure 6 for the type C devices. The exponential

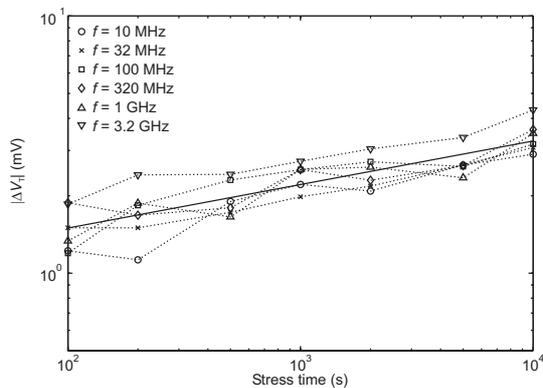


Fig. 6.  $V_T$  degradation as a function of stress time for the type C devices after an RF NBTI stress. The RF stress consisted of a sinusoidal DC gate voltage of  $-1.5$  V superimposed on a sinusoidal voltage signal with  $V_{pp}$  of  $3$  V. This was done for various frequencies ranging from  $10$  MHz to  $3.2$  GHz. The measurements were performed at  $125^\circ\text{C}$ . The solid line is a power-law fit yielding a time exponent of  $0.17$ .

time dependence reported before can be clearly recognized. The solid line shown in this figure is the average value of  $|V_T|$  degradation over all frequencies. Remarkably the time exponent of this average degradation was found to be  $0.17$ . This value is typically found with on-the-fly-measurements where recovery effects are completely eliminated.

A comparison between this RF behavior and DC NBTI measured on the same-type devices is shown in figure 7. The

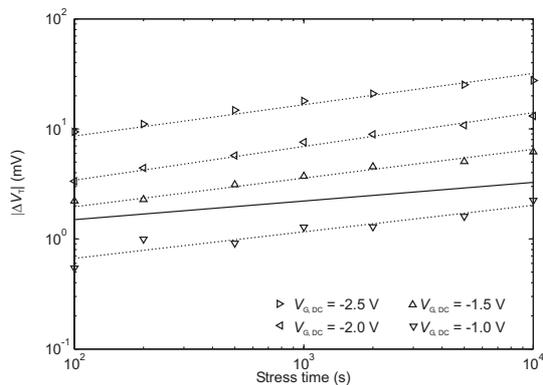


Fig. 7. DC and RF NBTI degradation of  $V_T$  plotted against stress time for the type C devices. The DC stress voltage was varied from  $-1.0$  V to  $-2.5$  V. The dotted lines are fitted to the data using a power-law time dependence with a time exponent of  $0.25$ . The solid line is the average degradation of  $|V_T|$  under RF NBTI stress as shown in figure 6.

DC degradation exhibits a time exponent  $n$  of  $0.25$ . The clearly different slopes seem to indicate that recovery effects are less pronounced in RF NBTI degradation. This may find its origin in the continuous on-and off switching of the device in RF NBTI experiments. During the off period recovery effects may take place that cause the difference with the DC stress results.

This means that for developing accurate models describing RF NBTI degradation these recovery effects should be carefully taken into account. For this purpose the use of various kinds of voltage waveforms might prove to be very insightful. Generating these waveforms at frequencies exceeding  $10$  MHz might be cumbersome. Based on the observed frequency

independence on the other hand, it may suffice to perform these experiments below  $10$  MHz. These low frequency data can then also be applied in describing RF NBTI degradation.

## V. GATE OXIDE BREAKDOWN UNDER RF STRESS

### A. DC and AC models for oxide breakdown

Gate oxide breakdown is the event of a sudden increase in the gate current when a high electric field is applied across the gate dielectric (or, when a large current is forced through it). It is the manifestation of a conducting channel formed inside the gate dielectric. Dielectric breakdown is reviewed by Lombardo et al. [31]. In this section oxide breakdown under RF stress conditions will be discussed.

Gate oxide breakdown is typically characterized using the time-to-breakdown  $t_{bd}$  measured in an accelerated test (with voltage or current stress higher than real-life conditions). For devices with an oxide thickness below  $5$  nm, gate oxide breakdown is voltage driven [32]. The time-to-breakdown can be described using a power-law model [33]. For ultra-thin oxide devices  $t_{bd}$  can therefore be written as:

$$t_{bd} \propto V_G^{-m} \quad (1)$$

In this expression  $V_G$  is the gate voltage and  $m$  is the power-law exponent. Reported  $m$  values are between  $30$  and  $40$ . This expression reveals that a minor increase in the gate voltage may dramatically decrease device lifetime.

Lifetime enhancement under AC stress has been observed by several authors [34], [35], [36], [37], [38], [39]. This effect is most pronounced under bipolar stress conditions. It has been attributed to frequency dependent hole trapping kinetics and the detrapping of holes during zero or negative bias stress [36]. These experiments have only been performed with frequencies up to  $10$  MHz. In [4] oxide breakdown under RF stress conditions was investigated by designing RF power amplifier circuits and recording  $t_{bd}$  values. The presented results revealed no difference in  $t_{bd}$  values between PA's operating at  $80$  MHz or  $1.8$  GHz. This approach very accurately mimics device operation under RF circuit conditions, but it is very laborious to properly investigate any frequency dependence; in [4] only two stress frequencies were discussed. Our RF voltage generation approach enables the generation of equivalent voltage signals at different frequencies, allowing a more thorough investigation.

### B. Oxide breakdown measurement setup

RF breakdown experiments were performed on nMOS transistors using the measurement setup shown in figure 8. The devices were processed in a  $0.13$   $\mu\text{m}$  process flow and have a gate channel length of  $0.13$   $\mu\text{m}$ . The total gate width of the devices is  $128$   $\mu\text{m}$ , consisting of  $2$  identical cells, each having  $64$  gate fingers of  $2$   $\mu\text{m}$  wide.

During the experiments the gate of the devices was stressed with a sinusoidal voltage signal. The peak-to-peak of the sinusoidal signal  $V_{pp}$  was set to  $3.35$  V and the DC gate bias offset  $V_{Gate}$  to  $1.675$  V. During the experiments the DC gate current  $I_{Gate}$  was monitored and used for the detection of breakdown events. Breakdown was defined as the time when a

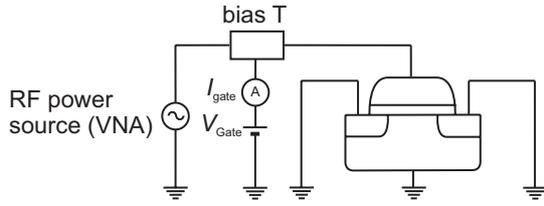


Fig. 8. Schematic drawing of the measurement setup used for RF oxide breakdown experiments.

relative increase of  $\geq 5\%$  in  $I_{\text{Gate}}$  was found. The result of this definition is illustrated in figure 9, showing gate current versus time for typical samples with their identified breakdowns. Hard

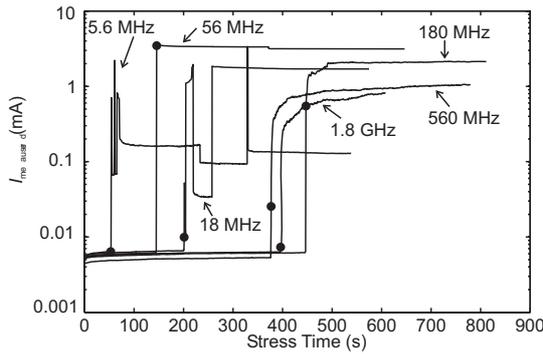


Fig. 9. Recorded  $I_{\text{Gate}}$  plotted against time. For each stress frequency one typical example is shown. The big dots indicate the moment in time where breakdown is detected using the 5% definition.

breakdown events are well identified on the given samples. Soft breakdown events may possibly be missed, but the use of the bias Tee limits a more accurate measurement of  $I_{\text{Gate}}$ .

### C. Oxide breakdown measurement results

Measurements were performed with stress frequencies ranging from 5.6 MHz to 1.8 GHz. The measurements at 5.6 MHz were done with the VNA replaced by an Agilent 33250A signal generator. For every frequency 20 samples were stressed and the  $t_{\text{bd}}$  values were recorded. The samples used for the different frequencies were randomly distributed over the wafer.

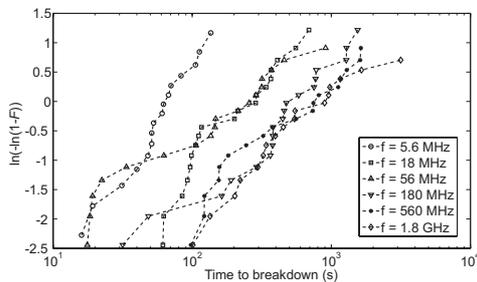


Fig. 10. Weibull plots showing the distribution of  $t_{\text{bd}}$  values for all measurement frequencies used.

In figure 10 the  $t_{\text{bd}}$  values are displayed in a Weibull plot for all stress frequencies. The figure reveals a gradual increase in the recorded  $t_{\text{bd}}$  values with increasing stress frequency.

Fitting a monomodal Weibull distribution using the maximum likelihood technique yields values for  $t_{63}$  (time at which 63% of the devices has failed) and  $\beta$  (representing the slope of the distribution).

The fitted values of  $t_{63}$  and  $\beta$  are plotted in figure 11. In this

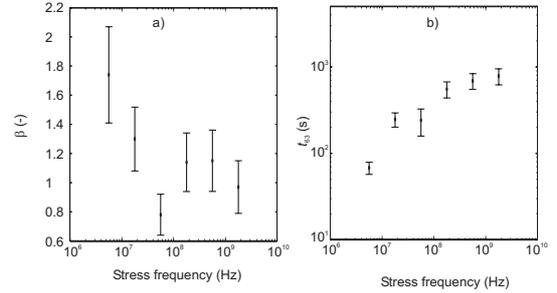


Fig. 11. Weibull parameters as obtained using a maximum likelihood estimation. The parameters are plotted against stress frequency with the standard deviation of the likelihood function included. A clear increase in  $t_{63}$  can be observed as a function of frequency;  $\beta$  appears to remain relatively constant at the highest frequencies but it fluctuates at the lower frequencies.

figure a clear increase in  $t_{63}$  can be observed with increasing frequency. The corresponding value of  $\beta$  on the other hand does not show a clear trend. At the highest frequencies it appears to remain relatively constant while it fluctuates more at lower frequencies. On the basis of the dielectric thickness (EOT = 1.5 nm), a value around 1.1 is expected [40].

The lifetime enhancement is in accordance with earlier reported results at lower frequencies [34], [35], [36], [37], [38], [39]. A striking difference with these earlier reported results is the relatively large increase in lifetime for unipolar stress signals. This (to our knowledge) has not been shown before. A possible explanation for this effect could be the increased importance of hole trapping kinetics for frequencies above 10 MHz rather than hole detrapping. This explanation is in line with the model presented in [36] where hole detrapping was regarded as the main cause of lifetime enhancement for bipolar stress signals. Hole trapping kinetics was considered a possible mechanism for lifetime enhancement for AC stress signals, but it could not explain the large difference between unipolar and bipolar stress signals.

Remarkably, our results seem to contradict the results presented in [4] where unipolar stress signals with frequencies of 80 MHz and 1.8 GHz were compared and no increase in lifetime could be observed. The exact voltage waveform used in [4] is significantly different from the sinusoidal gate voltage signals used in this section; this indicates that the exact stress voltage waveform is a very important factor in the exact amount of lifetime enhancement with AC and RF stress signals. Further studies are required to gain a complete understanding.

A lifetime increase of a factor 14 can be observed between 5.6 MHz and 1.8 GHz. Taking  $m = 35$  in eq. 1 this would result in an increase in the allowable  $V_{\text{pp}}$  from, for instance, 1.2 V to 1.28 V. This is an increase of 80 mV - or 10% headroom for an analog designer. Our results suggest, that gate voltage constraints based on DC dielectric breakdown evaluations may be relaxed for RF CMOS applications.

## VI. CONCLUSIONS

Using a previously reported RF voltage generation technique, the degradation of deep-submicron MOS transistors under RF stress is investigated. This technique allows the assessment of RF CMOS reliability for a variety of degradation modes, using one basic set of instruments and devices.

Hot-carrier stress on nMOS devices proves to follow existing models up to 3.2 GHz, while this was only confirmed up to 369 MHz until now. The hot-carrier degradation models are thus applicable for the reliability estimation of RF CMOS circuits.

NBTI degradation measurements on pMOS devices show, remarkably, that the time-evolution of the threshold voltage follows a power law with a slope as low as 0.17. This can possibly be attributed to recovery effects taking place during RF stress. No frequency dependence was found in  $V_T$  degradation under NBTI stress conditions, up to 3.2 GHz.

Dielectric breakdown measurements have revealed a considerable frequency dependence, indicating that increased headroom is available for RF CMOS design. This effect is known for bipolar stress, but has not been reported before on unipolar stress, which occurs more commonly in typical CMOS designs.

Existing models will give a conservative, but reasonably accurate prediction of the reliability of RF CMOS circuits. Higher operating voltages may be allowed when the dominant failure mechanism is gate oxide breakdown. A technology-specific evaluation should be made to quantify the available headroom, to offer designers the full potential of their technology.

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