RF-CV measurements on metal gate capacitors

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Gate leakage has complicated the layout and measurement of C-V test structures. In this paper the impact of metal gate introduction to *C-V* test structure design is discussed. The metal gate allows for wider-gate structures and for the application of n^+-p^+ diffusion edges. We show both theoretically and with experimental data, that both design modifications lead to a test structure with less overall area, and higher quality factors at the higher measurement frequencies.

Introduction

The gate leakage current density of next-generation CMOS technologies is forecast to extend beyond 1 kA/cm^2 [1], which complicates the characterization of MOS transistors with electrical techniques such as charge pumping and capacitance-voltage (*C-V*) measurements [2,3]. Increasing the measurement frequency to well above 1 MHz is one way to suppress the disturbing effect of gate leakage that gained considerable interest in recent years [4-7].

In this paper, an excursion is made to metal gate CMOS. Metal gates with their intrinsic benefit of much lower gate resistance offer a broader design margin for *C-V* test structures, as well as non-selfaligned source and drain implantations. We discuss the layout optimization of a high-frequency (or RF) *C-V* test structure given these new boundary conditions, and present first data from medium-k/metal-gate RF-CV measurements.

Low series resistance design

When going to higher frequencies, considerably more attention must be paid to the combination of measurement equipment, cabling, and test structures [7]. In test structure design, the two key issues to address are device series resistance on one hand, and non-quasistatic effects in the channel (in inversion) on the other. The non-quasistatic effects limit the channel length L roughly to $\leq$ 1 µm for measurements up to a few GHz, see e.g. [8]. Designing for low series resistance is less straightforward.

In this section we summarize equations that can be used to estimate the external resistance of a MOS capacitor with transistor topography, i.e. a gate finger with width W and length L, and with a highly doped source of carriers on two sides. We further connect the gate on both sides, and use an NMOS device as example. See figure 1.

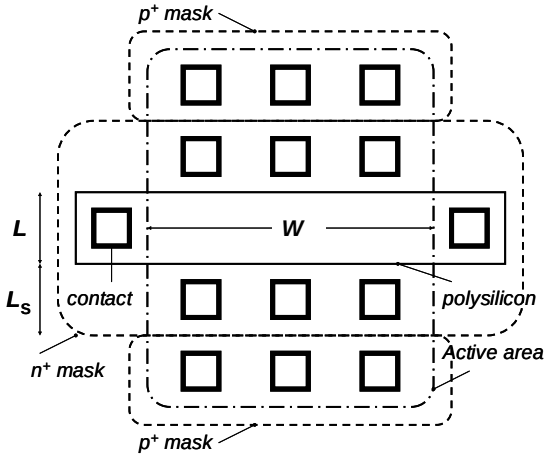

Figure 1: test structure layout sketch for an NMOS capacitor with n$^+$ diffusion edges and closely spaced well contacts. The key layout parameters are L, W and L_s. To reach the required overall capacitance, several of these structures can be drawn in parallel.

The gate resistance of such a structure with silicided polysilicon gates was shown to be [9]

$$R_{\mathrm{gate}} = \frac{1}{12}\frac{W}{L}\rho_{\square,\mathrm{g}} + \frac{1}{2}\frac{W_{\mathrm{ext}}}{L}\rho_{\square,\mathrm{g}} + \frac{1}{2}\frac{R_{\mathrm{via}}}{N_{\mathrm{via}}} + \frac{\rho_{\mathrm{con}}}{WL} \quad (1)$$

Referring to ref. [9] for further details, this equation expresses how the gate resistance is built up of gate sheet resistance $\rho_{\square,\mathrm{g}}$, an additional term for the gate material outside the active region, the resistance in contacts between poly and metal-1, and the silicide-polysilicon contact resistance. For the clarity of reasoning, we simplify the above equation to

$$R_{\mathrm{gate}} \approx \frac{1}{12}\frac{W}{L}\rho_{\square,\mathrm{g}} \quad (2)$$

This approximation holds well when W is large. At the other side of the gate dielectric, the series resistance is either dominated by the sheet resistance of the inversion layer (in inversion) or by the well resistance (in depletion and accumulation).

In analogy with eq. (2), the effective small-signal resistance of the inversion channel can be approximated as

$$R_{\mathrm{channel}} \approx \frac{1}{12}\frac{L}{W}\rho_{\square,\mathrm{ch}} \quad (3)$$

with

$$\rho_{\square,\mathrm{ch}} = \frac{1}{\mu_{\mathrm{eff}} C_{\mathrm{ox}}(V_{\mathrm{gs}} - V_{\mathrm{T}})} \quad (4)$$

A good C-V measurement in inversion is therefore obtained with a test structure where the design parameters W and L are chosen such that

$$\frac{W}{L} = \sqrt{\frac{\rho_{\square,ch}}{\rho_{\square,g}}} \quad (5)$$

at which point $R_{\mathrm{gate}} + R_{\mathrm{channel}}$ shows a minimum. Since the channel resistance (~1 kΩ/□) is much larger than gate resistance (~10 Ω/□) this calls for a long-width, short channel device, as normally applied.

The well resistance is most relevant for accumulation and depletion capacitance measurements. When the well is contacted via the chuck, and the resistance of the wafer plays a role, an external resistance of a few hundred ohms can easily occur [10]. Top side contacts can reduce this resistance. A general expression for the well resistance is not transparent because of the freedom in topological solutions and the vertically varying doping concentration in the well [11]. Here, after [11] for simplicity we assume that the well contacts run parallel to the gate finger on both sides (as in figure 1), and also that the resistance below the source/drain regions is dominant. This leads to the expression

$$R_{\mathrm{well}} = \frac{1}{2}\frac{L_{\mathrm{s}}}{W}\rho_{\square,\mathrm{w}} \quad (6)$$

with $\rho_{\square,\mathrm{w}}$ the sheet resistance of the well below a source/drain implantation (typically in the 0.1-10 kΩ/□ range). To suppress the significance of R_{well}, efforts should

focus on getting the well contact close to the channel, given a fixed technology (and hence fixed $\rho_{\square,w}$).
The minimization of overall external resistance R can now be carried out using equations (2), (3) and (6) and given the sheet resistances in a certain technology. (It should be noted that the choice of W and L do not affect the relative significance of the oxide conductance g_{ox} and the oxide capacitance C_{ox} as both scale with gate area.)

Test structures with metal gates
From the above discussion it is clear that the layout optimization depends on the gate's sheet resistance. Figure 2 shows how the quality factor in inversion for metal gates remains high when very wide transistors are laid out – while for poly gates the optimum quality factor is already reduced by gate resistance for gate fingers around 1 µm width. The trend for Q_{opt} is derived using equations (2), (3) and (6) and following the equation $Q_{opt} = \{4\, g_{ox} R(1+ g_{ox} R)\}^{-½}$ [4].

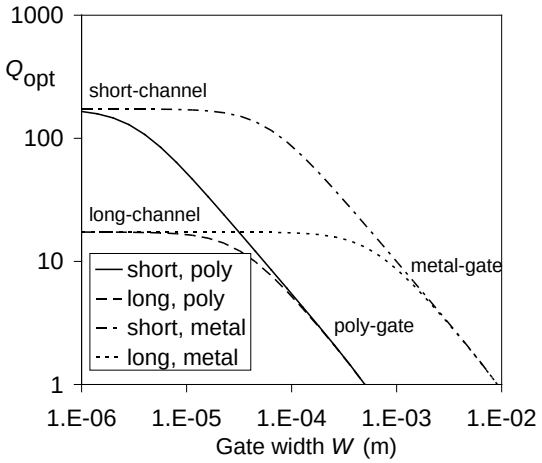

Figure 2: highest achievable quality factor Q_{opt} [4] in inversion for short-channel (0.1 µm) and long-channel (1 µm) gates with poly or metal gates, as calculated following eqs. (2), (3) and (6) and using the technology values listed in table 1.

Parameter	Value (inversion)	Value (accumulation)
$R_{sheet,g}$	0.03 / 10 Ω/□	0.03 / 10 Ω/□
$R_{sheet,ch}$	10 kΩ/□	n/a
$R_{sheet,w}$	n/a	250 Ω/□
L	0.1 / 1 µm	0.1 / 1 µm
g_{ox}	1 MS/m^2	1 MS/m^2
C_{ox}	15 mF/m^2	15 mF/m^2

Table 1: values used in the modeled capacitor structures.

The same trend is found in depletion and accumulation, because R_{well} and $R_{channel}$ have the same W dependence (eqs. (3) and (6)). Summarizing, the switch to metal gates leads to a wider freedom in the choice of W, yielding a higher optimum Q value in some cases.

The well resistance can be drastically reduced when a p^+ and an n^+ implantation are used on either side of the gate. In polysilicon gate technologies this leads to uncontrolled gate doping; however, a metal gate is not affected by the source/drain ion implantations. A structure as in figure 3 can now be fabricated, with a p^+ edge and an n^+ edge around each gate. The two-gate layout yields automatic compensation of the lithographic misalignment between the n^+ and p^+ implantation masks. Note that the effective channel resistance in inversion will quadruple, because of the single-sided minority carrier supply for each gate!
With the p^+ implant this close to the gate, a smaller overall test structure area is needed for a given $W*L$ overall capacitor dimension. With larger W per gate finger, the structure is also more compact because less gate fingers are needed. A metal-gate C-V test structure can thus be laid out in a more compact manner than a polysilicon-gate test structure, especially when the multifinger approach is used.

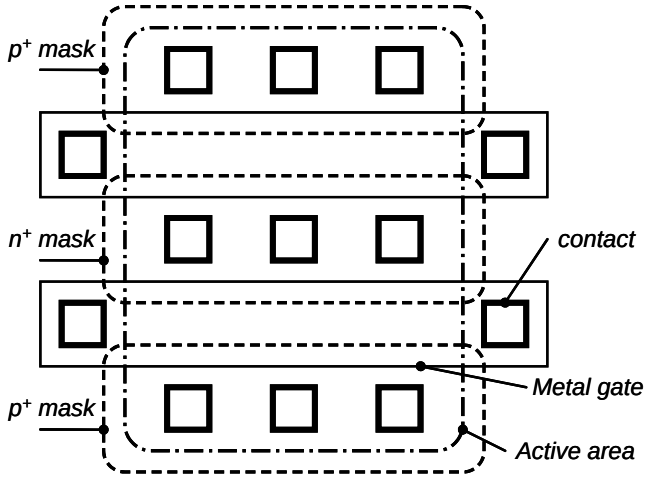

Figure 3: layout of a metal-gate MOS capacitor, with an n^+ and a p^+ diffusion edge around each gate, to facilitate the supply of both electrons and holes.

Experimental results
The test structure depicted in figure 3 was manufactured with an experimental process in the MESA+ Clean Room. The process features 1.5 µm lithography, a 2.1 nm EOT Al_2O_3 gate dielectric, and a TiN/Al gate. A 20 mΩ-cm p-type wafer was used without additional channel doping. The dielectric and TiN capping are ALD-deposited without vacuum break, in a home-built ALD cluster system. The technique results in a very thin interfacial SiO_2 of 0.3 nm. Note that the channel length can be laid out in submicron dimensions in spite of the limited lithographic capabilities: the effective channel length is determined by the offset between n^+ and p^+ masks (and implantation straggle and lateral diffusion).
The gate capacitance as extracted from Y11 with a three-element equivalent circuit is shown for two devices in Figure **X**. *etc*

To derive a specific capacitance, structures with several n^+-p^+ spacings ('channel lengths') are required. **The dielectric's insulating capabilities were rather poor compared to literature reports, and three orders of magnitude above theoretical expectations. This made a capacitance-voltage measurement the more interesting to carry out.**

Two devices as sketched in figure 3, with different gate lengths, were characterized to obtain the capacitance per unit area of the channel. The result is shown in figure 4. The quality factor of both test structures is well above 10 at all test frequencies (while $Q < 1$ at 1 MHz, because g_{ox} reaches values around 100 µS at high bias). The overall series resistance in accumulation is less than 10 Ω. We extracted the capacitance from Y_{11} using a three-element equivalent circuit. The frequency independent result is a clear indication that the capacitance extraction is effective. **Z_{11}-Z_{12} extraction [12] yielded comparable results.**

Inversion is not observed in the *C-V* curve. The main reason for this is the high V_T of the device (estimated to 1.42 V using the current criterion 100 nA*W/L). The low mobility (due to the ultra-thin SiO_2 interfacial oxide), and non-quasistatic effects in these long channels cause a poor observability of inversion just above threshold.

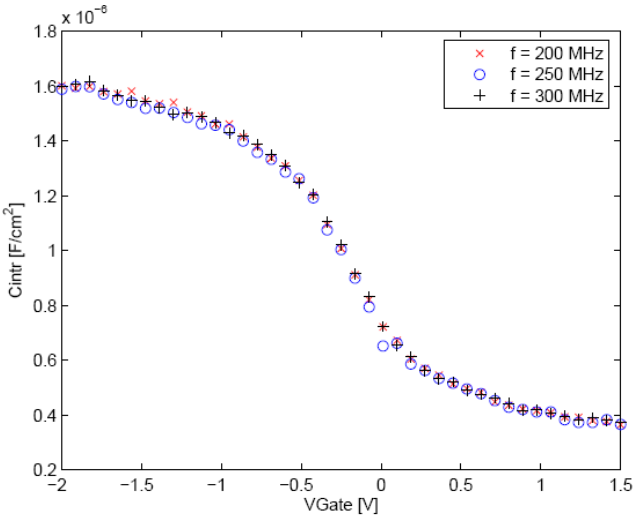

Figure 4: Intrinsic (channel) capacitance as obtained from the RF-CV measurement of two Al_2O_3/TiN MOS capacitors (W/L = 100 µm / 2.2 µm and W/L = 100 µm / 4 µm) with the gate overlapping an n^+ implant on one side and a p^+ implant on the other.

Test structures with the p^+ implant mask a few micrometers away from the metal gate exhibit an increase of the series resistance in accumulation and depletion (around a factor 2), as expected. However, capacitance measurements on such structures are still well feasible. This is illustrated with the *C-V* measurement result shown in figure 5. The lateral shift of the p^+ implant has the potential benefit that the p-type region of the channel is uniformly doped. This makes the analysis of the C-V measurement more straightforward. As compared to the situation where an n^+ implantation lies in between the gate and this p^+ contact, the resistance between the well contact and the channel region is still considerably less.

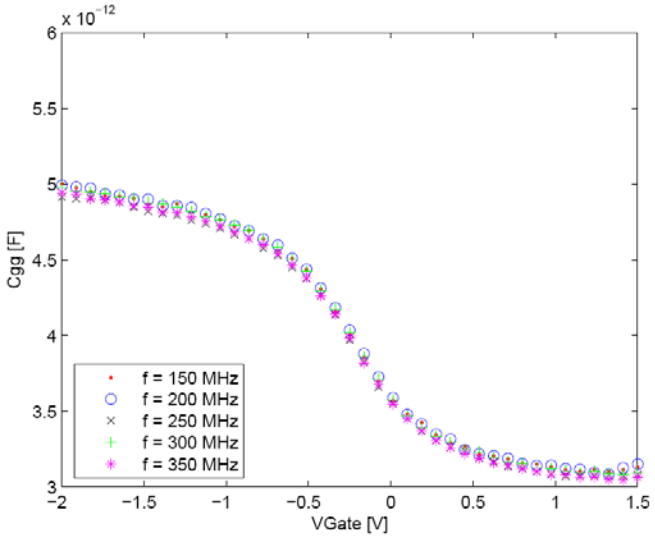

Figure 5: Capacitance C_{gg} of an Al_2O_3/TiN MOS capacitor (W/L = 100 µm / 2.2 µm) with the gate overlapping the n^+ implant, while the p^+ region is slightly moved away from the gate.

Conclusions

In this paper the impact of metal gate introduction to *C-V* test structure design is discussed. The metal gate allows for wider-gate structures and for the application of n^+-p^+ diffusion edges. Both design modifications lead to a test structure with less overall area, and higher quality factors at the higher measurement frequencies.

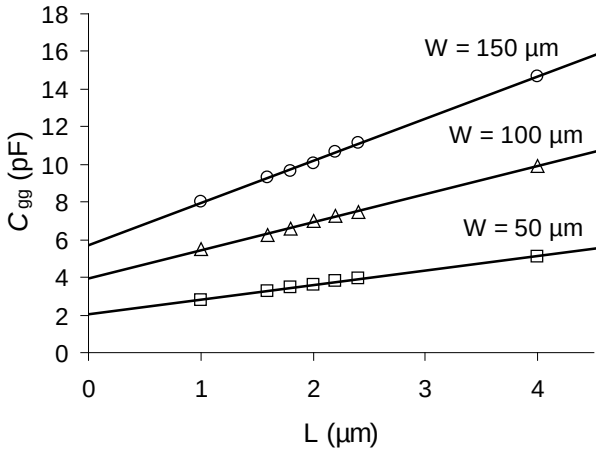

*Figure **X**: Measured gate capacitance at V_g = -2 V on test structures with various W and L dimensions. The capacitance neatly scales with gate length and width. Using*

these measurements, capacitance offsets (due to edge effects) can be established.

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