EMI Reduction in Class-D Amplifiers by Actively Reducing PWM Ripple

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***Abstract*—Class-D amplifiers switch high voltages and currents at high frequencies and hence produce electromagnetic interference (EMI). This work presents a technique to reduce the high frequency ripple, which is still present after the output filter. A Class-A ripple reduction amplifier is put in parallel to the output of the Class-D amplifier, each having their own feedback loop with digital filters. High ripple reduction loop gain is achieved at the PWM frequency by using a resonator as digital loop filter. Dissipation in the Class-A amplifier is reduced by using a low common-mode signaling technique. Common-mode and differential-mode switching components at the PWM frequency are reduced by 27 dB and 18 dB respectively. Total system efficiency is 79% at 40 W output power.**

***Index Terms*—Audio power amplifier, class-D amplifier, ripple reduction, delta-sigma analog to digital converter, electromagnetic interference (EMI), BD modulation.**

I. Introduction

CLASS-D power amplifiers are well suited for audio amplification, and have hence become the standard for power amplifiers in electronics for consumer, mobile and automotive applications. High efficiency is realized by switching the power stage transistors on and off, eliminating the dissipation associated with Class-AB amplifiers. This allows for high power output in a small form factor, as only a modest heat sink suffices. Total harmonic distortion (THD) performance of Class-D amplifiers has become equal to, or better than, the performance of Class-AB amplifiers. Both the high efficiency and high audio performance have resulted in a growth in the use of Class-D audio amplifiers [1].

The increased efficiency of Class-D has side effects, namely electromagnetic interference (EMI) due to high frequency switching. It is common to use switching frequencies of several hundreds of kilohertz, which do produce harmonics in the AM radio band. Furthermore, the fast switching transients produce frequency content in the high megahertz range which can interfere with, for example, the FM radio band. As set-top box or car audio amplifier systems connect the speakers via long leads, these leads will function as an antenna for the common-mode (CM) switching residue.

Manuscript received –; revised –. This work was supported by Stichting Technische Wetenschappen (STW), the Dutch Technology Foundation under Project 13911.

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Class-D amplifiers can utilize different modulation schemes when their output stage is in a bridge-tied-load (BTL) configuration [2]. The EMI reduction techniques that are explained later depend on the modulation scheme that is used, hence we will now first discuss these modulation schemes.

The most straightforward one is AD modulation as shown in Fig. 1. In an AD modulated system, the input signal is compared to the triangular reference and when the input exceeds the reference in value, a high output level is generated, otherwise a low output level is generated. This output signal is fed to the positive half bridge and an inverted version of it is fed to the negative half bridge.

Ideally, AD modulation will not excite a CM signal over the load, because the signal is purely differential. In reality mismatch between the LC filters will cause CM to differential mode (DM) conversion of the ripple, because the attenuation in the stop band isn't exactly equal.

BD modulation takes the same approach for the positive half bridge, however, to generate the negative half bridge signal, the input signal is inverted before it is compared to the reference to obtain the PWM signal as shown in Fig. 2. In idle this means that there is no DM voltage over the load, however the full PWM ripple is now present in the CM.

In a low CM signaling scheme the positive half bridge is responsible for amplifying the positive part of the input signal, and the negative half bridge the other part. This is done by clipping the positive half and the negative half of the input signal below and above zero, respectively, before comparing them to the reference, as can be seen in Fig. 3.

Several studies have been done to reduce EMI in Class-

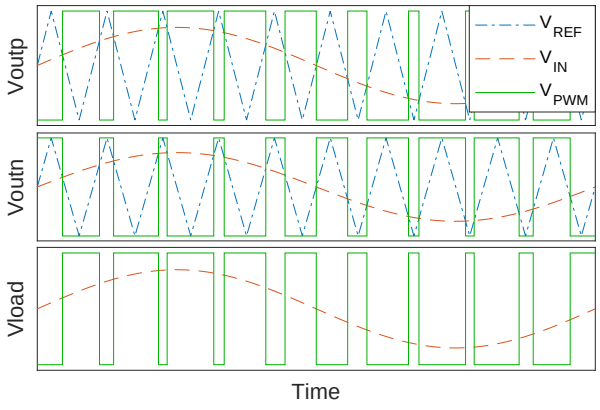

Fig. 1. Input, reference and output waveforms as result of AD PWM for a sinusoidal input signal.

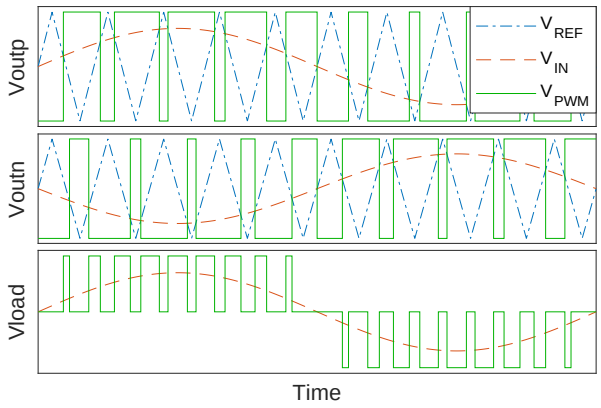

Fig. 2. Input, reference and output waveforms as result of BD PWM for a sinusoidal input signal.

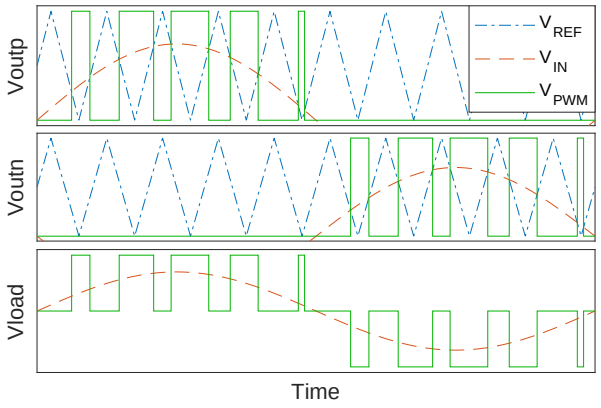

Fig. 3. Input, reference and output waveforms as result of low CM signalling PWM for a sinusoidal input signal.

D amplifiers, for instance in automotive electronics and to allow filterless operation in mobile devices. Three techniques are seen in literature, namely, switching frequency modulation [3]–[5], CM modulation [3], [6], [7] and Class-AB/D [8]–[13].

Switching frequency modulation (FM) of the PWM carrier is done by modulating the system clock or the triangle carrier wave. Modulation is done using a triangle pattern in [3], or a uniformly distributed pseudo-random spread spectrum signal in [4] and [5]. These techniques are applicable for both AD and BD modulation.

CM modulation is a technique that can be applied in BD modulated Class-D amplifiers. Since a zero-output level can be made by pulling both bridge halves to supply or ground, a degree of freedom exists. By randomizing the switching pattern for the zero-output level, the CM power is spread over a larger frequency range and consequently, EMI is reduced. In [3] the randomization is done using a pseudo-random sequence. A more advanced method is used in [6], where the pseudo-random sequence is noise shaped, specifically to have notches around defined AM radio frequencies. Finally the authors of [7] proposed a different BTL topology with two extra transistors to be able to shunt the load accompanied by a 3-level modulation scheme.

Class-AB/D is a technique that combines a linear amplifier with a switched-mode amplifier to improve efficiency by delivering most of the power via the switched-mode amplifier instead of the linear amplifier. A feedback loop is built around the linear amplifier to compensate the imperfections, such as distortion and the ripple current, of the switched-mode amplifier. The switched-mode can be controlled by sensing the current of the AB amplifier and using hysteretic control. However, it is difficult to make high loop gain over both the audio band and the PWM frequency range using analog filters while ensuring stability, moreover the AB amplifier will draw a quiescent bias current [9]–[12].

The FM and CM modulation techniques result in spreading the power of the interference over a wider band effectively increasing the noise floor. In Class-AB/D a lot of quiescent power is spent to eliminate the ripple in idle conditions, which is bad for efficiency.

In this paper a technique is proposed to reduce the CM and DM PWM ripple of a Class-D amplifier after the LC-filter by 27 dB and 18 dB respectively. This is achieved by utilizing a digital loop filter with high gain at the PWM frequency to actively compensate the ripple. Additionally, to limit dissipation in the ripple reduction circuit, a low CM signaling technique is used in a BTL configuration.

The paper is organized as follows. Section II presents the ripple reduction technique, section III presents the design method of the ripple feedback loop, section IV provides experimental results, and conclusions are drawn in Section V.

II. Operation Principle

A. Active ripple reduction

To reduce the ripple, first the output voltage is sensed and filtered to obtain the ripple signal. Subsequently that signal is used to draw the ripple current out of the filter inductor so it cannot go to the load and hence the ripple will not radiate from the speaker leads.

Fig. 4 shows the proposed topology consisting of a fixed carrier PWM class-D amplifier and a ripple reduction circuit. An ADC digitizes the voltage over the load and feeds it to a loop filter. This loop filter has high gain at the PWM frequency and low gain in the audio band. The output signal of the filter is converted back to an analog voltage to drive a Class-A amplifier, consisting of a MOS transistor (M_1) which serves as a current source closing the feedback loop.

A key difference of this technique with respect to the other modulation techniques [3]–[7] is that the power is removed from the spectrum, instead of being spread out over neighboring frequencies. Another advantage compared to classic AB/D amplifiers is the high gain at f_{PWM}, which is made

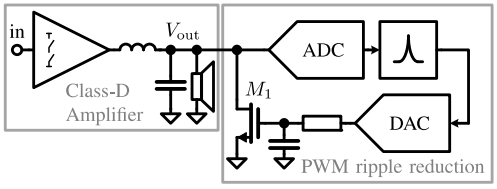

Fig. 4. Ripple reduction using a Class-A amplifier driven by a digital loop after the output filter of a Class-D amplifier.

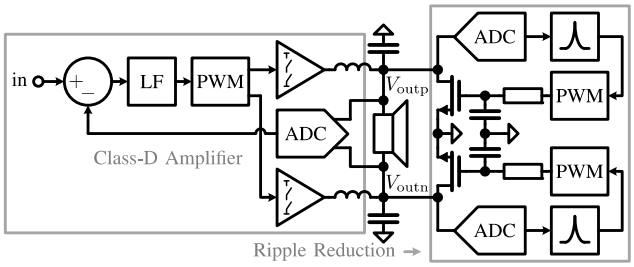

Fig. 5. BTL implementation of the ripple reduction circuit after the output filter of a Class-D amplifier.

possible by the digital filter. A down-side of the single-ended implementation is high dissipation in M_1. M_1 is biased in Class-A and always conducts a bias current while experiencing a V_{DS} of V_{out} of the amplifier. V_{out} is at half the supply and for a fixed bias current the dissipation of transistor M_1 is proportional to V_{out}.

B. Low common-mode signaling

To reduce dissipation, the V_{DS} over M_1 in Fig. 4 has to be reduced. By going to a BTL topology, a ternary modulation scheme [2] can be used that adds a degree of freedom to choose the CM level. Dissipation can be reduced by reducing the idle output CM voltage and thereby setting V_{DS} over the MOS transistors closer to ground. This BTL topology is shown in Fig. 5.

The top half of Fig. 6 shows the half bridge signals to have a low CM level. Achieving this lower CM level is done by subtracting an offset from the positive and negative half bridge signals. When the half bridge signals are high in amplitude, the subtracted offset will clip the signal at the lower bound $V_{\mathrm{D},0}$. This $V_{\mathrm{D},0}$ is defined to keep the Class-A MOS transistors saturated. To maintain linearity, the part that was clipped off below $V_{\mathrm{D},0}$ is added to the other half bridge signal as shown in Fig. 6. The bottom half of Fig. 6 shows the DM and CM output signals. Note that the V_{DM} is the reconstructed sine and V_{CM} is at 5 V except when one of the half bridge signals is clipped below $V_{\mathrm{D},0}$.

A low CM level reduces the idle power dissipation [14], but also reduces the performance of the amplifier. When one of the half bridges is clipped to $V_{\mathrm{D},0}$, just one half bridge is driving the load. During this transition the loop filter has to process an instantaneous change in slope from the output of the amplifier.

In the top half of Fig. 7 the contribution of each half bridge for a certain output voltage is given. Around idle output, both the HBs are controlling the signal and once the output signal goes over approximately $|V_{\mathrm{DD}}|/4$ one of the HBs is clamped to $V_{\mathrm{D},0}$. The bottom half of Fig. 7 shows the total dissipation as function of the instantaneous output voltage. The dissipation curve for active ripple reduction with conventional AD or BD modulation [2] is drawn to show the advantage in power dissipation of the low CM switching over normal AD or BD modulation. As audio has a high peak to average power ratio [15], most of the signal content resides in the valley of the

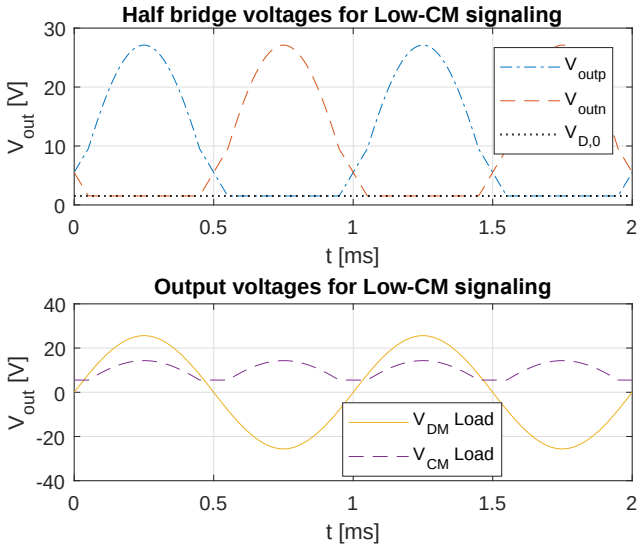

Fig. 6. Waveform illustrating the effect of low-CM signaling on half-bridge outputs (top) and CM and DM outputs (bottom).

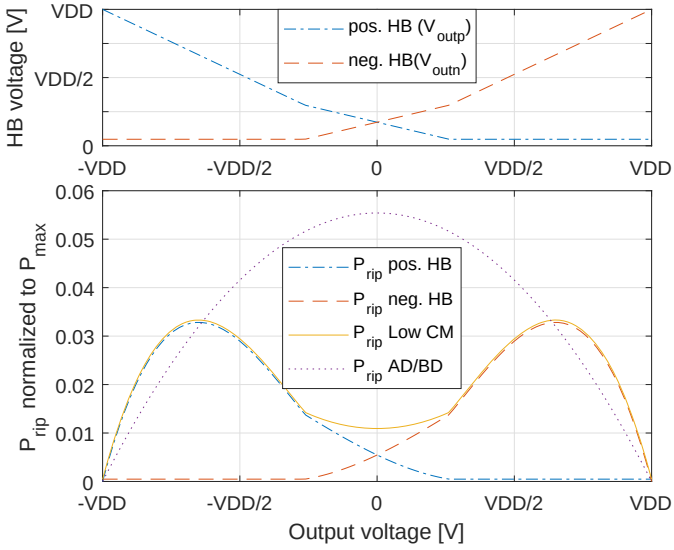

Fig. 7. Contribution of half bridges (HB) to the output voltage (top) and normalized power dissipation due to the ripple reduction.

graph and the ripple reduction power efficiency is up to 4 times better due to low-CM signaling.

III. Loop Design

Technology scaling has led to smart power processes which allow to integrate low-power digital signal processing (DSP) and high-power amplifiers on the same die. This allows the design of Class-D amplifiers with a digital, high-order loop filter [16] and an analog-to-digital converter (ADC) to provide feedback at the switching node [17] or after the output filter [18], [19]. Digital filters have an advantage over analog filters, being unaffected by process and temperature variation, allowing the use of higher order filters.

First, the Class-D amplifier is discussed. Secondly, all the blocks in the ripple reduction part of Fig. 5 will be discussed, as they define design constraints for the digital loop filter that

is to be implemented. After that the loop design method is explained and finally compensation is added to ensure a stable system.

A. Digital Class-D amplifier

To test the ripple reduction, a prototype was built around an AX5689 demo-board [20], as it features a high-performance audio amplifier, multiple ADCs and has a DSP core to implement a loop filter for the ripple reduction.

The core of the amplifier is a fully digital modulator and loop filter as seen in Fig. 5. A digital input signal is applied to the input. The feedback signal is digitized by the ADC and subtracted from the input, and the result is fed to the loop filter. The filter output is fed to the modulator, where the signal is compared to a digital staircase approximation of a triangle wave to obtain the PWM signals for the BTL power stage.

The ADC in the loop is a $\Delta\Sigma$ ADC because of the high accuracy and low latency required in audio applications. Detailed design considerations of such a low-latency ADC (LLADC) and the amplifier are given in [19].

B. Class-A driver

In order to realize the ripple reduction feedback loop, the digital feedback signal needs to be converted to the analog domain. The AX5689 is capable of generating eight PWM outputs, of which two are used for the BTL power stage. Hence the remaining six are distributed to have 3-phase PWM for each Class-A driver to perform digital-to-analog conversion. The schematic of this circuit is shown in Fig. 8.

Analog-to-digital conversion is done using one LLADC [19] per half bridge. The ripple reduction ADC output is fed to the loop filter, of which the output is fed to three PWM modulators. The modulators run at twice the loop filter sample rate, allowing 2 conversions per sample. The three carriers are shifted 120° in phase, and to reduce quantization noise, each carrier cycles through 6 different levels as shown in Fig. 9.

Summation of the PWM outputs is done using a resistive network that also provides level shifting and biasing to drive the MOS transistor. The drain of the MOS transistor is connected after the LC-filter as in Fig. 5, closing the loop.

C. Loop design constraints

The ripple reduction loop consists of several blocks as can be seen in Fig. 5. The LC-filter impedance converts the MOS transistor drain current, which is injected at the output of the LC filter, to a voltage at the output of the LC filter. This impedance has a band-pass characteristic, having 2 poles and 1 zero. Spread in C affects the ripple reduction loop stability because it changes the gain for signals above the LC corner frequency.

The used ADC is also integrated in the AX5689 chip. It has a second order rising slope of 40 dB/dec between 60 kHz and 1 MHz due to the two zeroes at 60 kHz transitioning into -20 dB/dec slope after 1 MHz due to the three poles at 1 MHz. The FIR DAC in the ADC renders the response highly insensitive to mismatch [19].

The RC filter used after the PWM DAC to reduce quantization provides an integrating response for signals at the PWM frequency due to the pole around 100 kHz. Spread in R and C will slightly alter the frequency of this pole and modify the integrator gain, this is however suppressed by the high overall loop gain. Finally the digital circuitry has processing delay, which gives a phase shift at frequencies in the vicinity of $f_{\mathrm{s,loop}}$.

Summarizing, these blocks contribute the following poles and zeros,

- LC-filter (2 poles @30 kHz, 1 zero @DC)
- ADC (3 poles @1 MHz, 2 zeros @60 kHz)
- RC Integrator (1 pole @100 kHz)
- 3 unit delays (3 poles in the origin of the z-plane)

D. Filter Synthesis

The next objective is to design a loop filter that can be put in the ripple reduction feedback loop in Fig. 5. As was mentioned earlier, this filter requires high gain at f_{PWM} and low gain in the audio band. To design such a filter, a method common in $\Delta\Sigma$ loop filter design [21] is used. With this method, a desired closed loop Noise Transfer Function (NTF) can be chosen and used to calculate the open loop transfer function $H_{\mathrm{loop}}(z)$. This is done by rearranging the definition of the NTF in a feedback system as follows,

$$\mathrm{NTF}(z) = \frac{1}{H_{\mathrm{loop}}(z)+1}, \tag{1}$$

$$H_{\mathrm{loop}}(z) = \frac{1}{\mathrm{NTF}(z)} - 1. \tag{2}$$

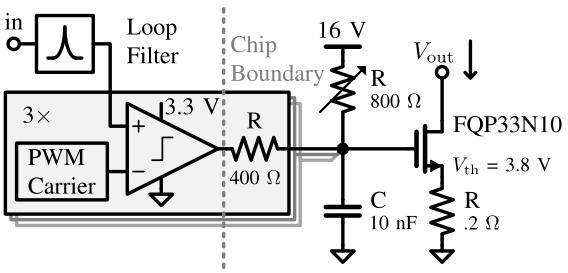

Fig. 8. Architecture of the DAC and Class-A driver.

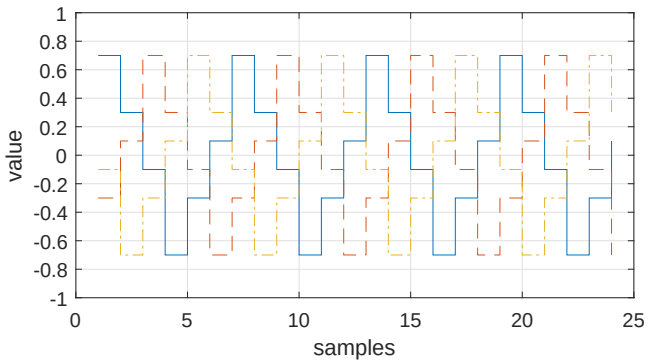

Fig. 9. 3-phase PWM carriers for D/A conversion.

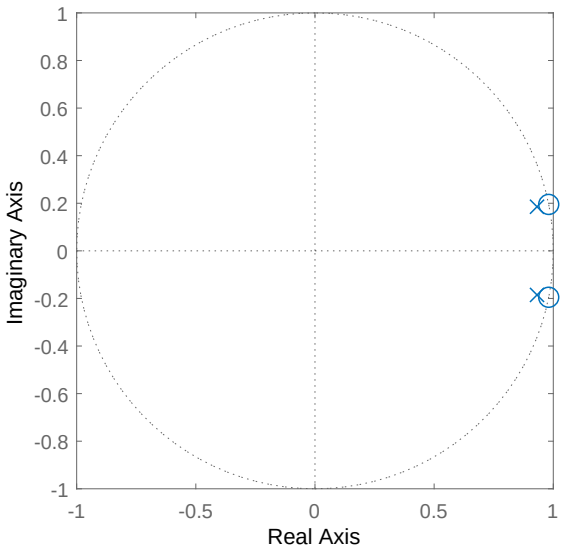

Fig. 10. Poles and zeros of the designed NTF.

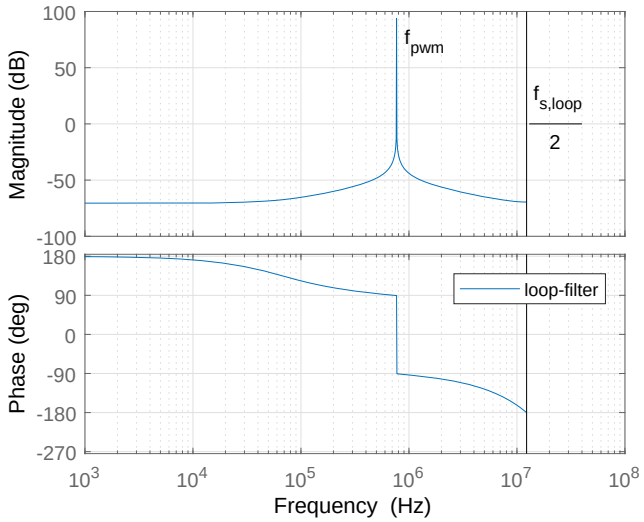

Fig. 11. Bode plot of the designed ideal loop filter.

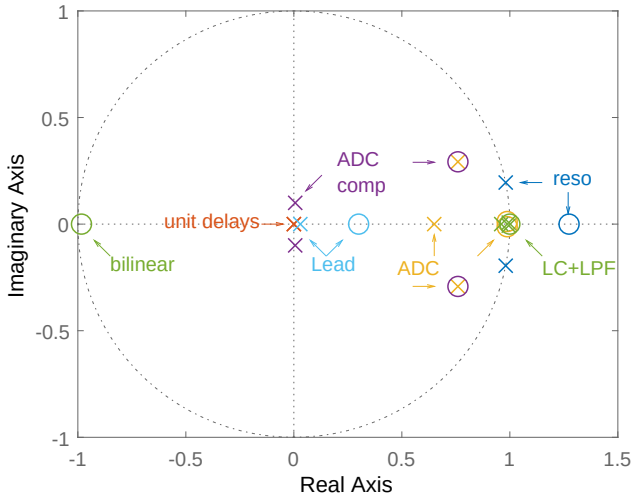

Fig. 12. Pole-zero map of the complete open loop transfer.

In this case, an NTF is chosen which leaves the audio intact and suppresses the PWM ripple. A way to design this is to place a notch at the PWM frequency. To make a notch, a complex zero pair is placed on the unit circle at an angle that is corresponding to the desired frequency. A complex pole pair is then placed inside the unit circle, at the same angle, close to the complex zeros in order to set the notch bandwidth. The angle in radians is calculated as follows,

$$\alpha = 2 \cdot \pi \frac{f_{\mathrm{pwm}}}{f_{\mathrm{s,loop}}}. \tag{3}$$

Now, using the exponential function the zero locations on the unit circle can be obtained as $z_1 = \mathrm{e}^{i\alpha}$ and $z_2 = \mathrm{e}^{-i\alpha}$. The pole locations can be derived by multiplying the zeros with a factor $r < 1$, giving $p_1 = r \cdot z_1$ and $p_2 = r \cdot z_2$. The closer r is to 1, the higher the quality factor and the sharper the notch will be.

To make a visualization of the poles and zeros, values have to be substituted in (3). A demo board with the 'AX5689' [20] is used to implement the filter and the audio amplifier. The default values in the controller are $f_{\mathrm{pwm}} = 768$ kHz and $f_{\mathrm{s,loop}} = 32 \cdot f_{\mathrm{pwm}} \approx 25$ MHz, which is used for the loop filter and ADC. The pole-zero map is shown in Fig. 10. In the actual system r is set to 0.996 but for visualization purposes the value for r is 0.95.

To get from this closed loop NTF description to a loop filter that can be put in the feedback loop in Fig. 5, (2) is applied. The resulting loop filter has a resonator at $f_{\mathrm{pwm}} = 768$ kHz, because of the $1/\mathrm{NTF}$ operation in (2). The loop filter transfer function is shown in Fig. 11. From the phase plot it can be seen that around the resonant frequency, the phase is already $\pm 90°$. Since the actual system consists of more elements than just the loop filter, maintaining stability becomes a challenge.

E. Loop compensation

Several blocks influence the stability of the ripple reduction loop. Hence, compensation has to be added to make the loop robust. All poles and zeros have been plotted in Fig. 12

In order to compensate the ADC poles, a second order lead compensator is added 'ADC comp' in Fig. 12. The complex pole pair of the 3 ADC poles is canceled by placing a complex zero pair on top of them. To maintain causality, two poles are added near $z = 0$. Ideally these could be unit delays.

The additional phase shift that the unit delays create is compensated by moving the zero of the resonator 'reso' more to the right, thereby reducing the phase lag near the resonator. This zero lies outside the unit circle, which is equivalent to a right half plane zero in the s-domain.

The combined continuous time transfer function of the RC-filter and the LC-filter was mapped to the z-domain using the bilinear transform resulting in the poles and zeros denoted with 'LC+LPF'. An extra zero, denoted as 'bilinear' in Fig. 12, got added as result of the continuous to discrete time conversion.

Finally, another first order lead compensator is added providing more phase lead near 1 MHz where the magnitude crosses 0 dB for improved stability.

For comparison, the total open-loop transfer before and after adding the compensation is shown in Fig. 13. It can be

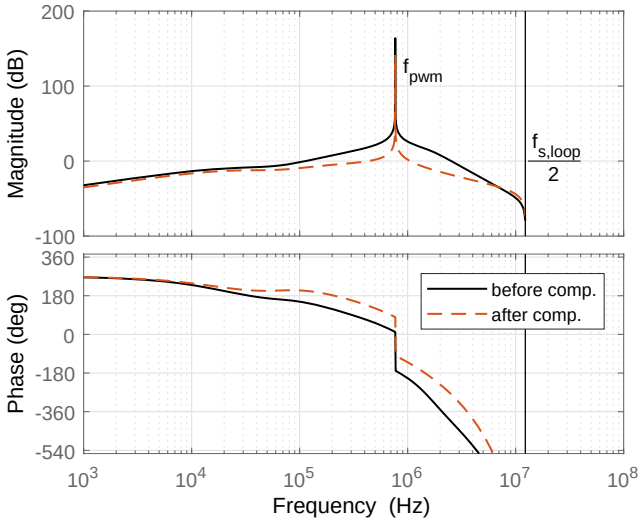

Fig. 13. Full open-loop transfer of the ripple reduction loop before and after compensation.

TABLE I
CM RIPPLE REDUCTION FOR DIFFERENT POWERS AND FREQUENCIES

P_{out}	100 Hz	1 kHz	10 kHz
0 W	29.3 dB	29.2 dB	29.0 dB
1 W	28.2 dB	28.5 dB	28.7 dB
10 W	28.4 dB	28.4 dB	27.1 dB

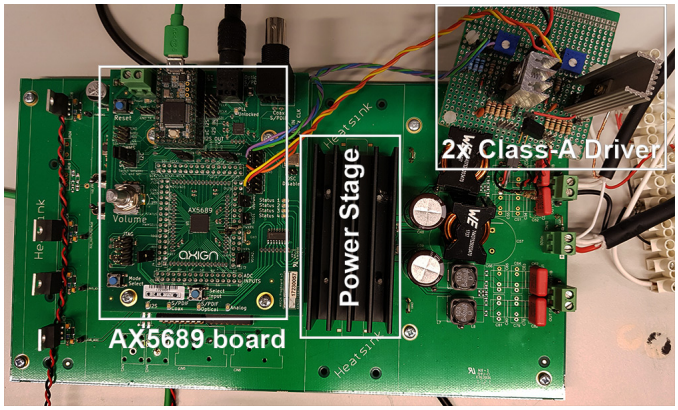

Fig. 14. Experimental setup consisting of the AX5689 demo board and an add-on board with Class-A drivers.

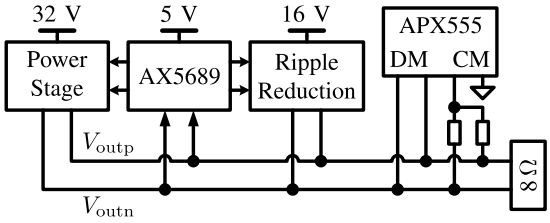

Fig. 15. Measurement setup showing the connections between the circuits and the measurement equipment.

seen that the transfer is flatter around the resonant peak and the phase jump has been moved up providing a larger phase margin. The phase margins around the resonator are 47° on the left side and 44° on the right side of the resonator peak. The 44° is the most critical margin, which translates to a delay margin of 2.8 unit delays or 114 ns.

The spread in L and C has been investigated. Changes in L have hardly any effect on stability because it only influences the transfer below the LC corner frequency of the parallel LC tank seen by the loop. Changes in C do have an effect on stability and the phase margin, which nominally is 44° and remains above 40° for a 10% decrease in capacitance.

Calculations in the on-chip filter are done with limited precision, hence the filter coefficients had to be quantized to fit the on-chip registers. Manual tuning of the filter coefficients' LSBs after quantization was necessary to put the resonator as close as possible to the PWM frequency.

IV. Experimental Results

The amplifier with ripple reduction after the output filter was built using the AX5689 demo board [20] with an additional PCB containing the ripple reduction Class-A drivers as shown Fig. 14. The system was measured using an APX555 audio analyzer setup as in Fig. 15. The measurement bandwidth of 1.2 MHz allows to measure the audio band as well as the PWM ripple.

Spectral analysis has been done to characterize the reduction in PWM ripple after the output filter. Both the differential- and common-mode spectra have been obtained using an f_{PWM} of 768 kHz, an 8 Ω load and a 1 kHz sine stimulus. Both measurements, with and without ripple reduction, were done using the low CM signaling. Just the ripple reduction circuit is turned on and off. The spectra are shown in Fig. 16 and Fig. 17 respectively. The DM spectrum shows the 5th order noise shaping behavior, provided by the loop filter. The CM spectrum doesn't have this behavior, because it is controlled by a different filter [19].

For emissions, the CM ripple is the most important to be reduced [22]. From the spectra it can be seen that both the DM

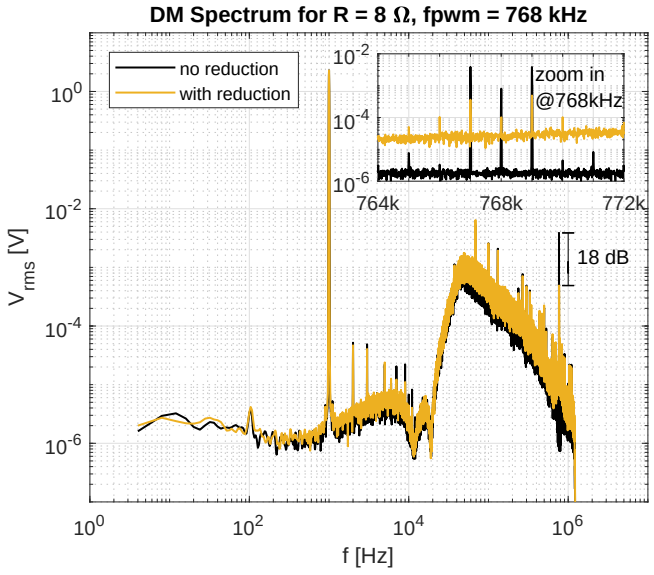

Fig. 16. Differential-mode spectrum, showing the PWM spur reduction. The zoomed inset shows the intermodulation spurs around f_{PWM}.

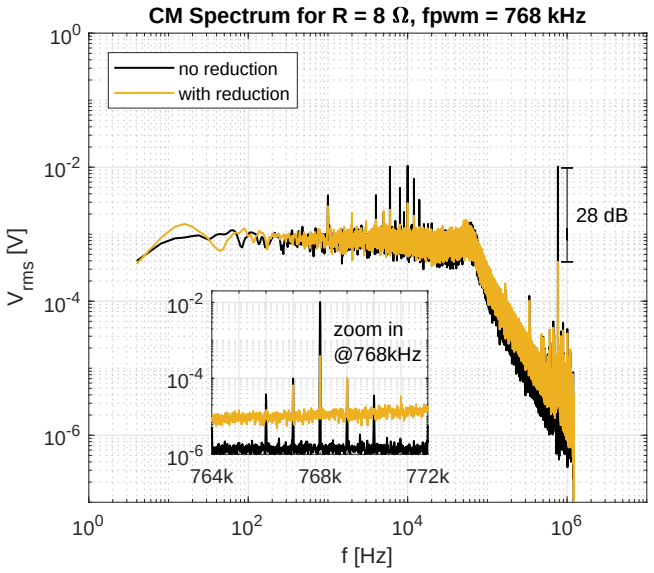

Fig. 17. Common-mode spectrum, showing the PWM spur reduction. The zoomed inset shows the intermodulation spurs around f_{PWM}.

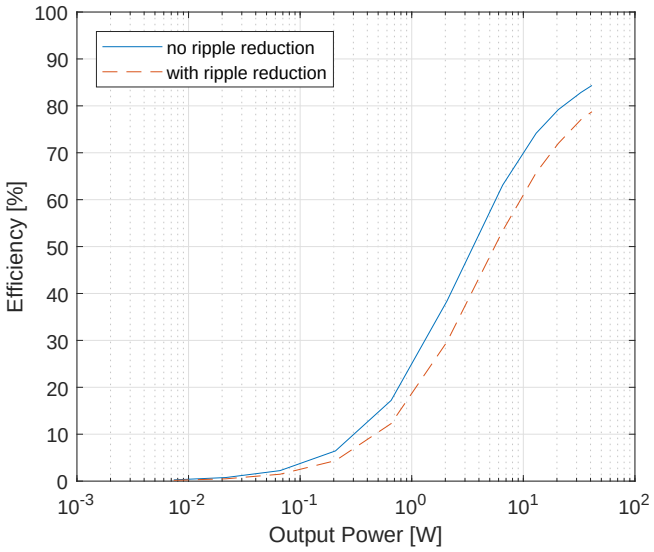

Fig. 19. Amplifier efficiency versus output power with and without ripple reduction with R_{load} = 8 Ω and f_{PWM} = 768 kHz.

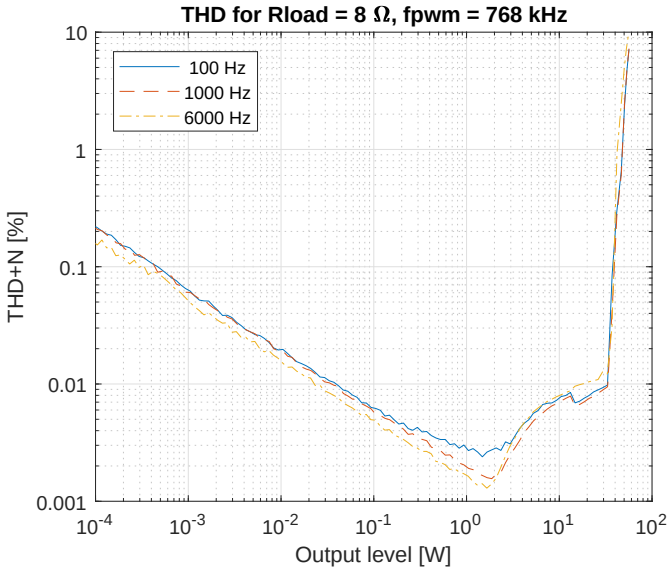

Fig. 18. THD+N plot for three frequencies with ripple reduction enabled.

and CM ripple are reduced by 18 dB and 28 dB respectively.

The ripple reduction has been calculated as the difference in magnitude between the frequency component at f_{PWM} with ripple reduction disabled and the highest frequency component after ripple reduction is enabled. In Table I the results are shown and it can be seen that the reduction is roughly uniform over signal frequency and output power. In case of the 10 W, 10 kHz measurement, the fundamental component of the ripple is reduced to a significantly lower value than the intermodulation tones at $f_{\mathrm{PWM}} \pm f_{\mathrm{in}}$, and hence the reduction is calculated using the intermodulation tones instead of the fundamental.

Audio performance with ripple reduction enabled has been tested by doing a total harmonic distortion plus noise (THD+N) analysis for three different frequencies; 100 Hz, 1 kHz and 6 kHz. The output power was swept from 0.1 mW up to clipping and the result is shown in Fig. 18. Ripple reduction had a minor penalty in THD, being 0.0017% without reduction and 0.0019% with reduction at 1 W 1 kHz. This is due to the slightly increased noise floor when ripple reduction is enabled. THD is below 0.003% at 1 W for all frequencies, the rise in THD above 2 W happens due to the transition from BTL to single-ended (SE) actuation where one half-bridge is clamped to $V_{\mathrm{D},0}$. This is a drawback compared to conventional AD and BD modulated systems. Maximum output power is 50 W at 10% THD+N and the idle noise of this amplifier is 50 µV (Awtd, at 32 V) resulting in a DR of 110 dB.

System efficiency ($P_{\mathrm{out}}/P_{\mathrm{in}}$, where P_{in} includes power consumption of all circuits) is 84% without and 79% with ripple reduction at maximum sinusoidal output power. Both efficiencies are shown in Fig. 19. There are three reasons that limit the efficiency, one being the dissipation in the on resistance of the power stage of 0.2 Ω, another being the dissipation in the bias circuit to provide level shifting for the Class-A driver and finally the bias current in the MOS transistor.

So the proposed technique does have an efficiency penalty, but in many applications were EMI is very important, this seems justifiable. An example is the use in polar RF PAs, where the ripple shows up directly in the spectrum and analog AB/D systems have long been used for this purpose [23]. Another advantage of the proposed technique is that it can be integrated on chip, providing ripple reduction without requiring extra external components.

A comparison to results of other works employing spread spectrum techniques is given in Table II. The listed works are amplifiers used in mobile applications which have attempted to reduce EMI. Spectra that illustrate the effect of switching frequency modulation and CM modulation and a combination of the two are presented in [3]. Apart from [6] the ripple reduction at f_{PWM} of this work is at least 10 dB better.

TABLE II
COMPARISON TO SPREAD SPECTRUM AMPLIFIERS

	Auer [3]	Guanziroli [5]	Ming [4]	Siniscalchi [7]	Balmelli [6]	This work
Architecture	Spread spectrum CM modulation	Spread spectrum	Spread spectrum	3-level	CM modulation	Active ripple reduction
Supply	5V	3.6-5V	2.5-5V	12V	2.7-6.6V	32V
f_{PWM}	390kHz	1296kHz	300kHz	250kHz	960kHz	768kHz
Ripple red. (CM)	17.8dB @390kHz / 7.3dB @10MHz	12dB @1296kHz	12dB @300kHz	HF EMI 20dB (not at f_{pwm})	25dB of AM channel	28dB @768kHz
OOB noise incr.	30+ dB @390kHz	18 dB @1296kHz	20 dB	n/a	up to 30 dB	3-6dB
Extra power	n/a	n/a	n/a	n/a	n/a	1.5W
Efficiency	n/a	81% @5V,8Ω,1W	90% @3.6V 8Ω .4W	90% @12V 8Ω 10W	85% @6.6V 3Ω 3.5W	79% @41W 8Ω
THD+N	0.018% @1W 1kHz	0.006% @4mW 3kHz, 0.2% @0.5W 3kHz	0.03% @.1W 1kHz	0.19% @5W 1kHz	0.05% @1W 1kHz	0.0016% @2W 1kHz

TABLE III
COMPARISON TO AB/D AMPLIFIERS

	Nakagaki [8]	van der Zee [9]	Jung [10]	Walker [12]	Choi [13]	This work
Architecture	BTL AB w/ variable switched supply	SE AB w/ fb hyst. self osc. D	SE AB w/ fb hyst. self osc. D	SE AB w/ fb 2x self osc. Buck	BTL AB w/ fb hyst. self osc. D	BTL D w/ fb A w/ ripple fb
Supply	±10V	±18V	±22V	±20V	12V	32V
P_{o} max	2 × 100W	30W	60W	20W	10W	40W
f_{PWM}	200kHz	550kHz	300kHz	160kHz	180kHz	768kHz
Ripple red. (CM)	n/a	77dB w.r.t. filterless	n/a	n/a	n/a	28dB w.r.t. LC
Quiescent power	10W*	1.8W	10W*	around 1W*	0.5W*	4.3W
Dissipation	75W @P_{o}=75W	3.5W @P_{o}=10W	5.5W @P_{o}=50W	4W @P_{o}=24W	0.7W @P_{o}=10W	10W @P_{o}=40W
Efficiency	53% @100W 4Ω	85% @30W 4Ω	90% @50W 4Ω	85% @24W 7.5Ω	92% @10W 8Ω	79% @ 41W 8Ω
THD+N	0.008% @20W 1kHz	0.007% @1W 1kHz	0.005% @50W	0.003% @1W 0.05% @20W	0.1% @1W 1% @6W	0.0016% @2W 1kHz

* Estimated from graphs in the papers.

Furthermore the presented technique does not increase the out-of-band noise as much as the spread spectrum based solutions. A downside of the proposed technique is the required extra power, whereas the other works don't consume extra power to implement the EMI reduction.

Next up, the proposed amplifier is compared to AB/D solutions listed in Table III. All these works do reduce the ripple at the output, however this cannot be compared quantitatively from the presented data. For quiescent power it is seen that this work consumes more power than [9], [12], [13] but less than [8], [10]. Efficiency could be improved by making a monolithic integrated system. In that system, a current steering DAC tailored for this application will eliminate the biasing losses (0.5%). Furthermore, an integrated power stage will reduce on-resistance losses (2.5%). Finally this work operates from a single ended supply where all but [13] use a symmetric supply rail.

V. CONCLUSION

A ripple reduction technique for Class-D amplifiers has been presented. The proposed technique uses an ADC to measure and digitize the ripple at the load, because in the digital domain loop-filters with high gain at precisely the PWM frequency are easily created and do not suffer from component variability. High loop gain was provided by using a resonant digital loop filter. The CM ripple at 768 kHz is reduced by 27 dB for output power levels up to 10 W. The power penalty of this technique has been reduced by implementation of a low-CM switching scheme.

State-of-the-art audio performance was provided by the AX5689, using feedback after the output filter, powered by the low-latency ADC and a digital fifth-order loop filter.

Compared to the EMI reduction techniques that were evaluated, the disadvantage of this technique is that it consumes additional power, whereas the spread spectrum techniques use digital blocks consuming hardly any additional power. These digital techniques however, do only spread the power over frequency, while the proposed technique reduces the PWM carrier with a minor increase in out-of-band noise.

Compared to the hybrid Class-AB/D amplifiers this solution has better control over the feedback because it is implemented in the digital domain. The efficiency of the presented approach could be improved by making an integrated system.

The final result is an audio amplifier with 28 dB ripple reduction requiring little extra power with 79% peak efficiency. Ripple power is removed instead of spread out over a wider band.

ACKNOWLEDGMENT

The authors would like to thank Tim van Doesum at Axign for his assistance on building the measurement setup.

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