Reduced sidewall effects in SiGe-base bipolar transistors

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Abstract
In small Si bipolar transistors (BJTs) the sidewall effects play an important role. Extensive device simulations on Si/SiGe/Si heterojunction bipolar transistors (HBTs) and Si BJTs show that in the HBTs the sidewall current injection is strongly suppressed. Consequently, the current gain in the HBT keeps constant down to a much smaller emitter width ($W_e \approx 0.20$ μm) than for a conventional Si transistor ($W_e \approx 0.60$ μm). Although the ratio of the charge storage in the sidewall emitter-base region and charge storage in the intrinsic region is also much less in the HBT than it is in the BJT, the effect on the cutoff frequency is about the same just because of the suppressed current spreading.

1 Introduction
Applying SiGe to the traditional Si technology leads to many technical advantages. High cutoff frequencies and high current gains can be reached in Si/SiGe/Si HBTs. Therefore, much research has been done on SiGe HBTs in the last years [1]. Furthermore, one of the most important features in the development of bipolar transistors is the reduction of the device dimensions (downscaling). The two-dimensional nature of the carrier injection into the base region near the sidewall (sidewall current) can strongly affect the device behaviour [2]. In this context we discuss simulations on Si and SiGe NPN transistors for investigating the sidewall effects. It appears that the sidewall effects are smaller in SiGe HBTs than in Si BJTs: the current gain of the HBTs is much less sensitive for downscaling than it is for Si BJTs. The influence of the sidewall on the cutoff frequency of the HBTs is about the same in BJTs, being rather small.

2 Results
A typical device structure of an advanced poly-silicon emitter NPN HBT and BJT and its vertical doping profile are shown in figure 1. The heterojunction interface in the HBT has been placed close to the

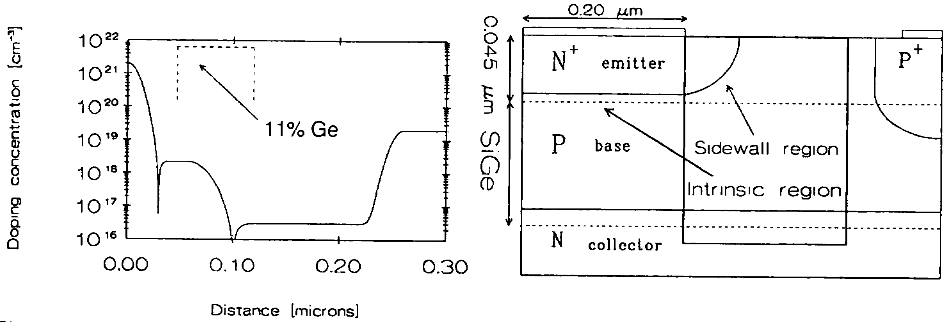

Figure 1: The vertical doping profile and cross-section of the NPN HBT/BJT. The full drawn lines are the emitter and collector junctions. The rectangular area drawn in the figure corresponds to the area used in the simulations shown in figure 2. The SiGe region is indicated with dotted lines. The distance in the vertical doping profile is relative to the poly-Si/mono-Si interface.

emitter-base depletion layer. The optimal position of the heterojunction interface depends on the processing and is still a point of research. The details of this position are not important for the reduction of the sidewall effects.

For the simulations the device simulator MEDICI [3] had to be calibrated for physically correct model parameters of the SiGe strained layer. These parameters are different from Si. For the bandgap narrowing in SiGe $\Delta E_g = 81meV$ was taken. Moreover, the ratio between the product of the effective densities-of-states (DOS) $(N_cN_v)_{SiGe}/(N_cN_v)_{Si} \approx 0.40$ was used, as was determined from temperature dependent collector current measurements [4],[5]. For the mobility in SiGe the same model was taken as in Si [6],[7]. In these simulations the maximum cutoff frequency $f_{t,max}$ of the HBT reaches a value of 51 GHz and the BJT, with the same device dimensions and doping profile, a value of 39 GHz. The differences in cutoff frequencies occur due to the higher intrinsic carrier concentration in the base of the HBT.

In figure 2 the current flow lines are plotted for the BJT and the HBT. As can be seen, the current spreading in the HBT is much less than in the BJT. Due to the presence of the SiGe, the bandgap in the intrinsic region decreases and accordingly the intrinsic carrier concentration n_i increases. The collector current density can be written as:

$$J_c = \frac{q}{\int_0^L \frac{p}{D_n \cdot n_i^2} dx} \cdot \left[e^{qV_{be}/kT} - 1 \right], \quad (1)$$

where L is the device length, D_n the diffusion coefficient, p is the hole concentration in the base and V_{be} the emitter-base voltage. The integral in the denominator of equation (1) can be seen as an effective Gummel number, which is an integral along a current flow line. In the BJT relatively more current flows through the intrinsic region than through the sidewall region because the sidewall currents have a larger effective Gummel number than the intrinsic currents due to the emitterdepth.

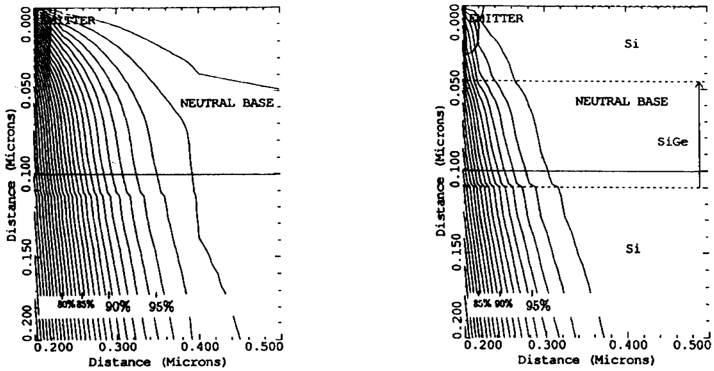

Figure 2: Current spreading at the emitter sidewall in the BJT (left figure) and the HBT (right figure) ($W_e = 0.40 \mu m$, $V_{be} = 0.50V$, $T = 300K$). The area of these figures corresponds with the rectangular area drawn in figure 1. The area between two current flow lines represents 1 % of the total current. The number under the flowlines gives the percentage of the total current that flows between the lines and the axis of symmetry.

However, by placing a SiGe layer in the intrinsic region, the current in the intrinsic region increases, because the effective Gummel number decreases due to the enhanced n_i. Consequently, the sidewall current decreases compared to the intrinsic current because a Si region is present at the emitter edge.

In other words, the SiGe layer causes the HBT to have a more one-dimensional performance. If the Ge percentage is increased the focussing effect would be even more enhanced. Assumed we have a rather low Ge percentage (11 %) in order to get a high quality of the heterojunction interface.

The reduced current spreading results in a nearly geometry independence of the current gain h_{fe} (see figure 3): the h_{fe} is less sensitive for emitter stripe width W_e alteration than in the BJT. Scaling the emitter stripe width from 1.40 μm down to 0.10 μm the h_{fe} in the HBT increases with 23 % and in the BJT with 80 %. The h_{fe} becomes higher with lowering W_e, because the sidewall collector current remains the same, while the sidewall base current is very small in this example.

Current spreading results in charge storage in the sidewall transistor. The storage is caused by the injection of the minority carriers in the sidewall base region which are neutralized by the hole charge. The total transit time τ can be written as:

$$\tau = \frac{dQ}{dI_c} = \frac{dQ_{int} + dQ_{sw}}{dI_{c,int} + dI_{c,sw}} = \frac{dQ_{int}}{dI_{c,int}} \cdot \left(\frac{\frac{dQ_{sw}}{dQ_{int}} + 1}{\frac{dI_{c,sw}}{dI_{c,int}} + 1} \right) \quad (2)$$

where dQ and dI_c are the charge storage and the collector current perturbations, respectively, both for a small change in the applied emitter-base voltage. The subscriptions *int* and *sw* mark the intrinsic and the sidewall region, respectively. Each of the ratios dQ_{sw}/dQ_{int} and $dI_{c,sw}/dI_{c,int}$ are smaller for the HBT than for the BJT which results in a

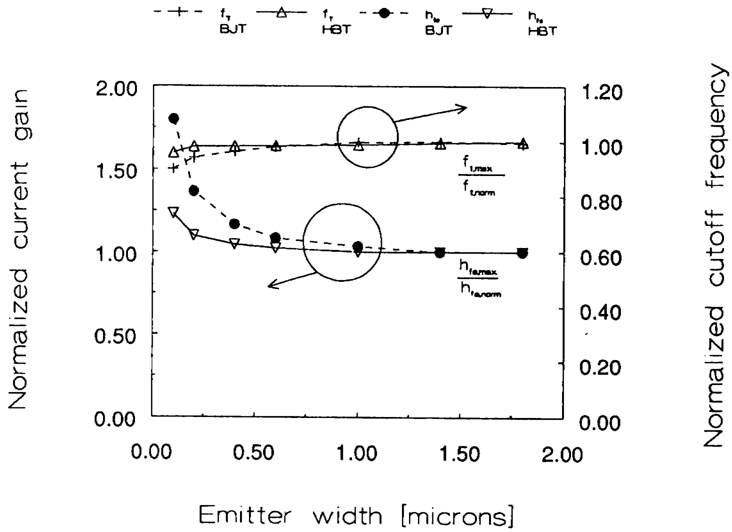

Figure 3: The normalized maximum cutoff frequency $f_{t,max}/f_{t,norm}$ and maximum current gain $h_{fe,max}/h_{fe,norm}$ as a function of the emitter width W_e for both the HBT and BJT simulated with MEDICI (V_{cb} = 1.0 V and T = 300 K). The normalization factors used for the HBT are $h_{fe,norm}$ = 360 and $f_{t,norm}$ = 51 GHz and for the BJT $h_{fe,norm}$ = 60 and $f_{t,norm}$ = 39 GHz.

relatively small sensitivity for the sidewall injection. By narrowing the emitter from 1.80 μm down to 0.10 μm $f_{t,max}$ decreases with approximately 4 % in the HBT and 10 % in the BJT (see figure 3).

3 Conclusion

It appears that for the SiGe HBTs the influence of the sidewall effects are strongly reduced. Particularly the current gain of SiGe HBTs becomes rather insensitive for downscaling than those of Si BJTs. These reduced sidewall effects are important for future downscaling of bipolar transistors.

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