A Mixer-First Receiver with Enhanced Selectivity by Capacitive Positive Feedback Achieving +39dBm IIP3 and <3dB Noise Figure for SAW-Less LTE Radio

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***Abstract*— A mixer-first receiver enhanced with capacitive positive feedback is proposed to obtain a steeper filter roll-off and enhanced linearity, while keeping low noise figure. It covers all sub-6GHz cellular bands and achieves a high IIP3 of +39dBm and blocker 1dB gain compression point of +12dBm for a blocker frequency-offset of 80MHz at f_{LO}=2GHz. The NF ranges from 2.4dB at f_{LO}=1GHz to 5.4dB at f_{LO}=6GHz. The chip has been fabricated in Globalfoundries 45nm SOI technology on a high resistivity substrate.**

***Index Terms*—Mixer-first receiver, BPF, tunable, blocker rejection, high-linearity.**

I. INTRODUCTION

To improve data rate and coverage, cellular phones based on the LTE standard have to support an ever increasing number of bands, now covering much of the spectrum up to 6GHz.The mobile receivers need to deal with large out-of-band (OOB) blockers to prevent degradation in sensitivity. Although high-linearity SAW filters are often adopted for blocker rejection, they cannot be integrated in CMOS and are not tunable, making multi-band 1-6GHz support troublesome. In recent years, the exploitation of N-path filtering in mixer-first receivers showed some promise [1-5]. This paper proposes a higher order RF bandpass filtering mixer-first receiver enhanced with capacitive positive feedback to obtain a steeper filter roll-off, increased frequency range and enhanced linearity, capable of achieving a noise figure below 3dB.

II. RECEIVER ARCHITECTURE

Steeper filter roll-off can be realized using higher order filtering by cascading N-path filter stages coupled by gyrators [2] or *gm-C* filtering [3]. However, in both cases active *gm* cells contribute extra non-linearity and noise. To enhance IIP3 and compression point, OOB signals should preferably be rejected as early as possible by steep filtering immediately at the RF input. We propose to do this by adding a capacitive positive feedback path to the mixer-first architecture of [1], as shown in Figure 1. Whereas [5] adds positive resistive feedback to aid input impedance matching at low noise, our key target is *selectivity enhancement at high linearity and low noise*.

Capacitor C_1 across the negative feedback amplifier $-A_0$ interacts with source impedance R_s and mixer-switches to perform N-path filtering. As a result, a first order low-pass filter is frequency translated to a 2nd order RF bandpass filter around f_{LO}. Due to the Miller effect C_1 contributes $Z_1 = (s(1+A_0)C_1)^{-1}$ to baseband input impedance $Z_{in,BB}$ (see Fig. 1), where A_0 is $gm \cdot r_o$. To achieve higher order filtering, a capacitor C_2 driven by the baseband (BB) signal followed by an attenuator $-A_a$ are added, effectively implementing a positive feedback path. Note that A_0 and A_a are both positive. Assuming that $(2\pi r_o C_o)^{-1} >> f_{3dB,BB}$, impedance of C_2 becomes higher order and is given by $Z_2 = [s^2 r_o C_o C_2 + s(1 - A_0 A_a)C_2]^{-1}$. Z_0 is the real part of the receiver input impedance which is designed to provide 50Ω matching and consists of the mixer output impedance in parallel with the scaled real part of input impedance of the BB amplifier [1]. The combination of the new positive feedback path C_2 and the conventional negative feedback path C_1 synthesizes two complex poles resulting in a theoretical 4th order RF bandpass and 2nd order BB low pass filtering. Note that both BB feedback paths can have *high linearity, better than what is achievable with RF gm blocks*. Moreover, this circuit does not cascade real poles, but rather *realizes a complex pole pair* with quality factor Q. The term $(1 - A_0 A_a)$ associated with the positive feedback path allows for Q tuning and was designed to accomplish a Butterworth filter response.

III. CIRCUIT IMPLEMENTATION

Figure 2 shows the circuit schematic of the proposed

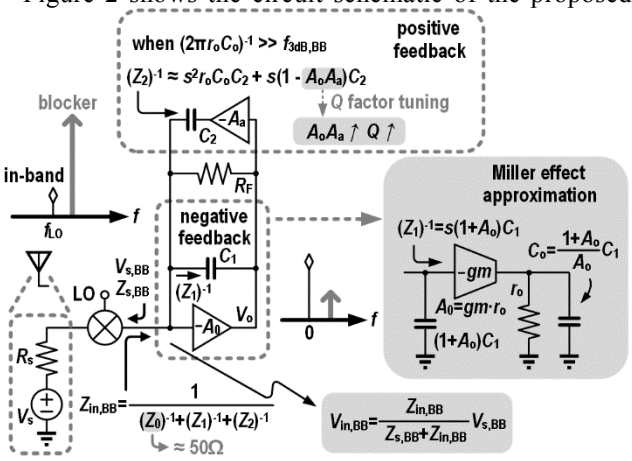

Fig. 1. Conceptual diagram of the proposed receiver.

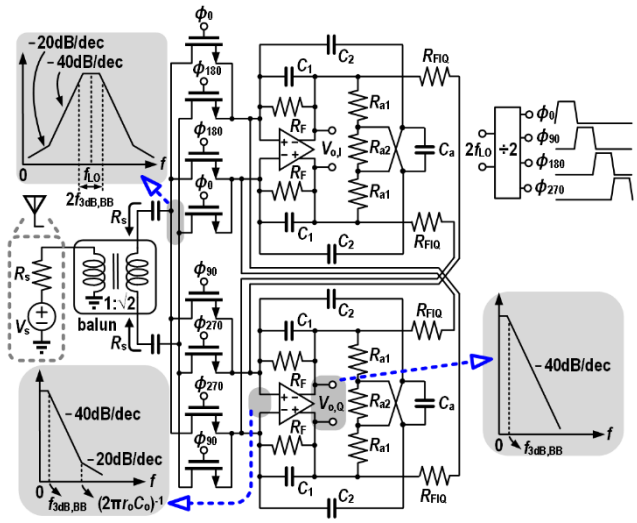

Fig. 2. Circuit details of the proposed receiver.

receiver. It was designed for $f_{3dB,BB}$ =10MHz, using C_1=60pF and C_2=106pF. The passive mixer switches are driven by 4-phase 25% duty-cycle clocks provided by a divide-by-2 circuit. The parasitic capacitors at the RF input cause the frequency of optimum S_{11} to shift towards frequencies lower than f_{LO}, which was solved by introducing complex feedback via resistors R_{FIQ} [1].

A. Higher order RF bandpass filtering realization

Due to the differential architecture, the negative gain $-A_a$ for the attenuator in Fig.1 can simply be implemented by wire-crossing, while passive resistors R_{a1} (45Ω) and R_{a2} (90Ω) realize high linearity attenuation. This hardly degrades NF because the resistor noise is divided by the BB amplifier gain when referred back to the RF input. The positive feedback path via C_2 serves as one of the OOB blocker bypassing paths and hence low impedance is important to maintain good blocker rejection. For this purpose capacitor C_a is added, providing a low impedance for high blocker offset frequencies. Simplified plots of the transfer function at both the RF and BB nodes are added in Fig. 2 to clarify the concept. For frequencies up to $(2\pi r_o C_o)^{-1}$ (which is normally much larger than BB bandwidth $f_{3dB,BB}$) the transfer function is 2nd order low pass at the BB-amplifier input, which is upconverted to a 4th order bandpass filter around f_{LO}. The higher order filter shape provides better selectivity and it is especially beneficial when the OOB signal is close to the desired band. Compared to conventional mixer-first receivers, simulations indeed show 10-15dB improvement in OOB IIP3 for the same mixer switch size, bandwidth and BB amplifier gain.

B. Receiver loop stability

The receiver loop gain $H_l(s)$ is given by:

$$H_l(s) = [-A_0(s)] \cdot [-A_a(s)] \cdot \beta(s) \quad (1)$$

where $A_0(s)=A_0/(1+sR_s(1+A_0)C_1)$ models the gain of the amplifier, and $A_a(s)$ that of the attenuator composed of R_{a1}, R_{a2} and C_a. $\beta(s)$ is the feedback factor from attenuator output to the input of BB amplifier. The loop gain $H_l(s)$ should be kept below 0dB to guarantee stability. At very low frequency, C_2 is a very high impedance and $\beta(0)\approx 0$ so that $H_l(0)\approx 0$. When frequency increases, the impedance of C_1 and C_2 becomes lower resulting in lower $A_0(s)$ and higher $\beta(s)$. $|H_l(s)|$ is kept <–6dB and gain margin is about 6dB for a Butterworth filter realization. In the proposed receiver architecture, $A_0(s)$ and $\beta(s)$ vary with frequency but in opposite direction, which makes both filter shape and loop stability insensitive to PVT variations. Simulations show that the gain margin maintains >6dB for different transistor, *R*, *C*, voltage and temperature corners.

The antenna impedance may change with user proximity in a mobile phone. The proposed receiver remains stable for all passive R_s or complex Z_s. The BW of $A_0(s)$ is determined by R_s and C_1. At a given frequency, higher R_s will cause lower $A_0(s)$ and higher $\beta(s)$ because $\beta(s)$ is roughly proportional to R_s. As $A_0(s)$ and $\beta(s)$ are linked, robust filter shape, loop gain and stability is achieved.

C. Low noise BB amplifier

Inverter-based baseband amplifiers [7] offer low noise with good power efficiency, while loop stability is of less concern in a single-stage amplifier. Figure 3 shows the schematic of the BB amplifier also used in [8]. Higher V_{th} for M_{cm} and low overdrive voltage for M_p ensures all transistors operate in their saturation region. For a differential input signal, a high gain of $(gm_n + gm_p)(r_{on}\|r_{op})$ is achieved where r_{on} and r_{op} are the output impedance of M_n and M_p. For a pure common mode input, gm_p acts as a cascode for M_{cm} offering a low output impedance of $1/gm_{cm}$ and low common-mode voltage-gain gm_n/gm_{cm}. Note that traditional CMFB circuits often use M_{cm} in triode with small gm_{cm}, which does not offer such low common-mode voltage gain.

IV. MEASUREMENT RESULT

The test chip has been fabricated in a GlobalFoundries 45nm SOI technology on high resistivity substrates. The

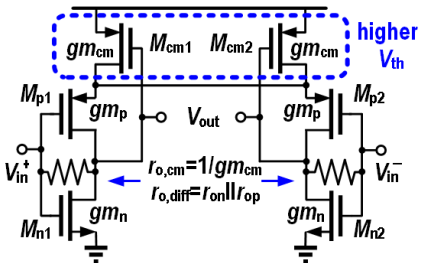

Fig. 3. Circuit schematic of low noise BB amplifier [8].

active area is 1000umx800um and a QFN package was used. The chip photo is shown in Fig. 4. The mixer and clock generator circuits are implemented by using floating body devices while the BB amplifier is built by body contacted devices to avoid the history and kink effect. Wideband off-chip hybrids were used to provide a differential RF signal and impedance match to the 100Ω differential chip input. Figure 5 shows the measured gain and S_{11} as a function of RF input frequency for f_{LO}=2GHz; 21dB gain and 20MHz –3dB BPF bandwidth is achieved. As in simulation, the passband shows a systematic slope induced by *I-Q* cross-coupling resistors R_{FIQ} introduced to center S_{11} [1]. Together with pass-band ripple, this slope can be compensated in the digital domain. The BPF roll-off becomes less steep at higher offset frequency, due to non-ideal properties of the N-path filter implementation such as non-zero switch resistance and imperfect clock duty cycle [9]. As a result, the actual RF BPF rolls off less steeply than the theoretical 4th order one. Figure 5 also shows blocker 1dB gain compression point (B_{1dB}) as a function of the frequency offset Δf for f_{LO}=2GHz and a desired signal at 2.001GHz (f_{BB}=1MHz). Already at Δf>20MHz, B_{1dB}>0dBm, while for Δf>60MHz it is B_{1dB}>+10dBm, while using only a 1.2V supply (other designs like [6] boost B_{1dB} by increasing the supply voltage). IIP3 and IIP2 as a function of Δf are shown in Fig. 6. Note that IIP3 increases to almost 40dBm over less than a decade change in offset-frequency, demonstrating the effectiveness of the higher order filtering. The achieved IIP2 is 88dBm for Δf>80MHz. Two-tone IIP3 and IIP2 measurements were carefully executed using a test-setup with circulators, and the blocker tone frequencies were adjusted to keep the resulting IM3 or IM2 product at a BB frequency of 500kHz. Figure 6 also shows the input referred IM3 as a function of blocker power for f_{LO}=2GHz. Note that P_{IIM3} follows the extrapolation line up to an input power of 0dBm! The extrapolated IIP3 for Δf=80MHz is +39dBm which is about 10-15dB better than for a traditional mixer-first receiver [1]. Figure 7 shows the measured gain and DSB NF as a function of LO frequency. At higher frequency, RF input parasitic capacitance deteriorates the magnitude and shifts the dip in S_{11}. Both R_F and R_{FIQ} are programmed to optimize S_{11} for different LO frequencies. Note that required R_{FIQ} becomes lower and contributes extra noise for higher RF frequency. The NF ranges from 2.4dB at f_{LO}=1GHz to 7.2dB at f_{LO}=8GHz, remaining below 5.4dB up to 6GHz. In order to cover RF-frequencies >6GHz and to achieve low phase noise, the clock generator consumes 30mW/GHz, targeting a phase noise of –171dBc/Hz at 80MHz offset frequency (=duplexer offset). Indeed, the measured blocker NF in Figure 8 degrades only from 2.5dB to 4.7dB at 0dBm blocker power, roughly fitting the target spec. A performance summary and comparison with state-of-the-arts is shown in TABLE I. The comparison clearly shows that this design achieves a significant improvement in LO frequency range, IIP2 and IIP3, while maintaining a competitive noise figure with and without blockers. This confirms the effectiveness of the higher order filtering provided by the proposed mixer-first receiver exploiting positive capacitive feedback.

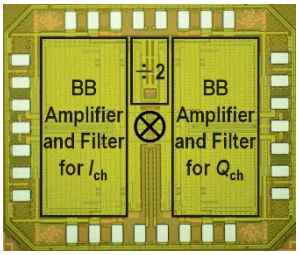

Fig. 4. Chip photo.

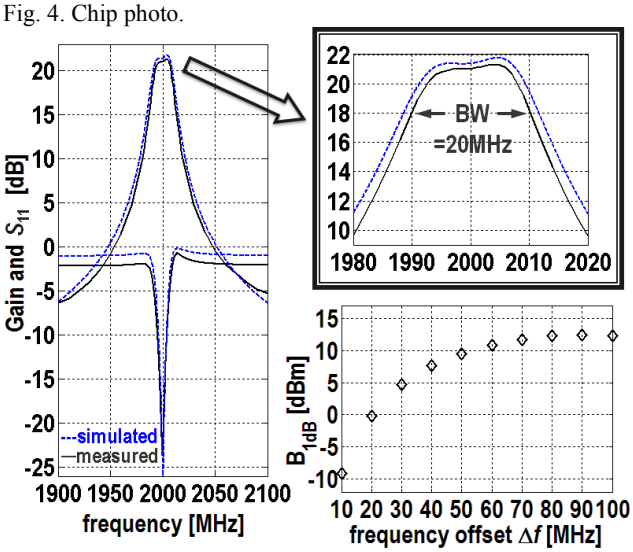

Fig. 5. Measured and simulated gain/S_{11} versus RF frequency and B_{1dB} versus blocker frequency offset Δf (f_{LO}=2GHz).

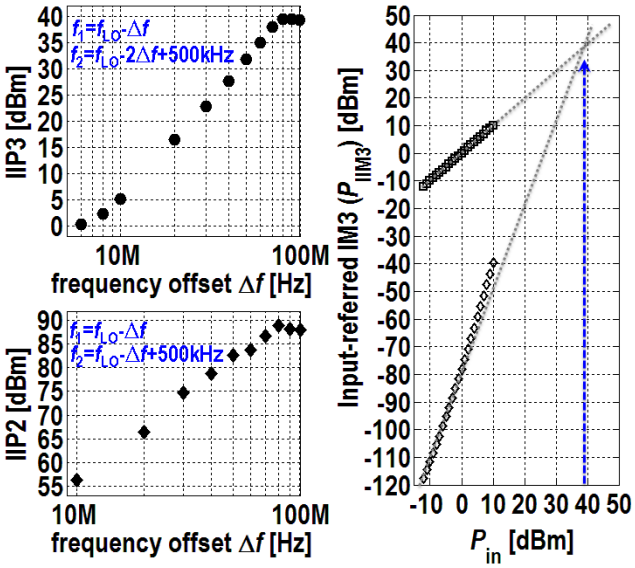

Fig. 6. Measured IIP3 and IIP2 versus blocker frequency offset Δf and P_{IIM3} versus P_{in} for Δf=80MHz (f_{LO}=2GHz).

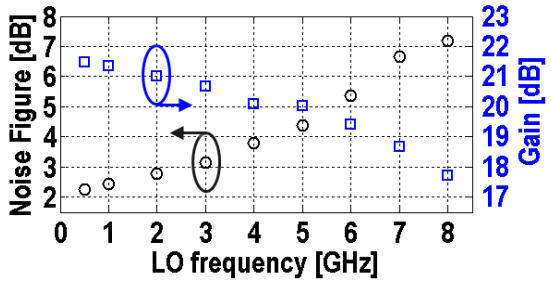

Fig. 7. Measured gain and DSB NF versus LO frequency.

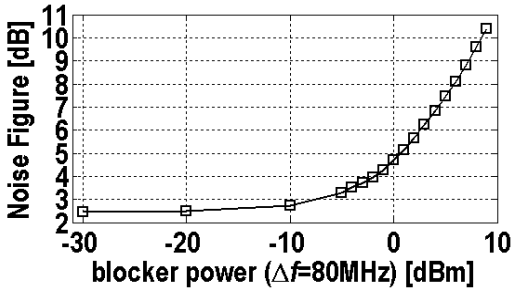

Fig. 8. Measured blocker NF for f_{LO}=1.4GHz. (The highest f_{LO} for blocker NF measurement is 1.4GHz due to the availability of bandpass filters for blocker and clock sources.)

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TABLE I
RESULT SUMMARY AND COMPARISON WITH PRIOR ART.

	*JSSC*10[1]	*JSSC*13[2]	*JSSC*15[3]	*RFIC*15[4]	*RFIC*15[5]	*RFIC*15[6]	*JSSC*12[7]	*ISSCC*17[8]	This Work
Architecture	Mixer first	N-path filter	Mixer first +2nd order baseband	Mixer first with LO leakage suppression	Mixer first with positive resistive feedback	Feedback with N-path filter	Mixer first with Noise Cancelling	N-path filters with bottom -plate mixing	Mixer first with positive capacitive feedback
Circuit type	Receiver	LNA/Filter	Receiver	Receiver	Receiver	LNA/Filter	Receiver	Receiver	Receiver
Technology	65nm	65nm	65nm	28nm	65nm	32nm SOI	40nm	28nm	45nm SOI
f_{RF}[GHz]	0.1-2.4	0.1-1.2	0.5-3	0.4-3.5	0.7-3.8	0.4-6	0.08-2.7	0.1-2.0	0.2-8
Gain[dB]	40-70	25	50	35	40	12	72	16	21
BW[MHz]	20	8	2-60	15-50	20	15	4	13	20
OOB IIP3[dBm]	25 Δ*f*/BW=5	26 Δ*f*/BW=6.3	−4.8 Δ*f*/BW=4	20.5 Δ*f*/BW=3.3	26 Δ*f*/BW=5	36 Δ*f*/BW=3.3	13.5 Δ*f*/BW=20	44 Δ*f*/BW=6.3	39 Δ*f*/BW=4
OOB IIP2[dBm]	56	NA	NA	64	65	NA	55	90	88
B_{1dB}[dBm]	10 Δ*f*/BW=5	7 Δ*f*/BW=6.3	−10 Δ*f*/BW=4	4.6 Δ*f*/BW=3.3	3 Δ*f*/BW=5	>17 Δ*f*/BW=6.7	−2 Δ*f*/BW=20	13 Δ*f*/BW=6.3	12 Δ*f*/BW=4
NF[dB]	4±1	2.8	3.8-4.7	2.4-2.6	2.5-4.5	3.6-4.9	1.9 (2GHz f_{LO})	6.3 (1GHz f_{LO})	2.3-5.4 (0.5-6GHz f_{LO})
0dBm Blocker NF[dB]	NA	NA	NA	6.5 (f_{LO}=2GHz)	NA	NA	4.1 (f_{LO}=1.5GHz)	8.1 (f_{LO}=1.3GHz)	4.7 (f_{LO}=1.4GHz)
LO leakage [dBm]	−65 (f_{LO}=1GHz)	<−64 (f_{LO}=1GHz)	NA	<−62	<−60	<−40	NA	NA	<−65
Supply[V]	1.2/2.5	1.2	1.2/2.5	1/1.5	1.2	2	1.2/2.5	1.2/1.0	1.2
Power[mW]	37-70	15-48	RX:76-168 LO:54-194	38-75	27-75	81-209	27-60	38-96	50mW*+ 30mW/GHz**
Area[mm²]	2.5	0.27	7.8	0.23	0.23	0.28	1.2	0.49	0.8

*power consumption of BB amplifiers=50mW, **clock generator power is 30mW/GHz.

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