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Characterisation of low energy boron implants and electrical results of submicron PMOS transistors.

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Abstract- Low energy boron implants between 200 eV and 10 keV have been characterised for the effect of channelling and of pre-amorphisation on the as-implanted profiles. Suitable rapid thermal anneal conditions for a shallow drain formation compatible with a 0.18 µm CMOS process were determined. One of these conditions was then used to fabricate PMOS transistors with shallow drain extensions using a 0.18 µm flow chart. Transistor characteristics such as threshold voltage, junction leakage and asymmetry were then measured as a function of implanted species and energy, and of gate length.

I. Introduction

Ion implantation has for more than 20 years been the method of choice for doping semiconductor devices in Si. These devices are subject to an ongoing decrease in lateral and vertical dimensions. One obvious and successful way to accommodate for decreasing dimensions has been to lower the implantation energy. For next generation Complementary Metal-Oxide-Semiconductor or CMOS devices the Semiconductor Industries Association (SIA) roadmap [1] gives a projection of the required depth of drain extensions: between 360 Å and 720 Å for 0.18 µm gate length devices and between 260 Å and 520 Å for the 0.13 µm devices. The uniform channel concentration will increase from the mid 10^{17} cm^{-3} to low 10^{18} cm^{-3} range. The spread in junction depth reflects the different requirements for different applications: logic devices at the lower end, and DRAM applications at the higher end. The p-type drain extension formation through B implantation poses a more of a problem than n-type formation with As or P because of the lighter mass of B.
After implantation an anneal treatment is necessary both to activate the implanted species as well as to remove the implantation damage. For shallow drain extension implants Rapid Thermal Processing or RTP is used.

II. Experimental

All of the implants were performed on an Applied Materials xR-LEAP™ ion implanter, using 200 mm (100) n-type Si wafers with a specific resistivity of 2.7-4 Ω.cm. The implant twist angle was 315° and the tilt angle was 7°. For the rapid thermal anneal experiments an Applied Materials Centura™ RTP-tool was used. All anneals were done in a pure nitrogen ambient. The wafers received no specific cleaning steps either before or after implant, or after anneal. Secondary ion mass spectrometry (SIMS) in fig.1 was performed on a Cameca ims4f using a 0.4 µA O_2^+ beam of 3 keV. The beam was rastered over 250×250 µm^2 and secondary ions coming from the central area of 30 µm diameter were analysed. The secondary ions monitored were $^{11}B^+$. SIMS analysis of figs. 2 and 3 was carried out by Evans East on a Physical Electronics 6600 secondary ion mass spectrometer using O_2^+ primary ion bombardment with positive secondary ion detection. A primary ion energy of 1.5 keV was used with a 65° angle of incidence with respect to the surface normal. An oxygen leak was used for all the analyses in order to obtain accurate data in the surface region of the analyses. The spreading resistance measurements (SRP) were performed by Semiconductor Assessment Services Ltd. Four-point probe (FPP) measurements were done in-house using a Prometrix OmniMap® RS55/tc.

III. Results and Discussion

A. As-implanted

A long-standing issue in ion implantation is the channelling behaviour at low implantation energies. Will channelling limit the applicability of ion implantation for ultra-shallow junctions ? In fig. 1 a 5×10^{14} cm^{-2} B implantation at different low energies is shown for three conditions: a 7° tilt angle, a 0° tilt angle and an implant into a 205 nm deep Ge-pre-amorphised Si wafer. The 7° tilt angle is routinely used to suppress channelling. A preamorphised wafer will give no channelling. As can be seen, for 10 keV the 0° tilt angle is significantly deeper than the 7° tilt demonstrating the enhanced channelling at low tilt angles. Strikingly, the 7° tilt implant also shows considerable channelling compared to the amorphous implant. The lower energies display the same behaviour, but the difference in profile between the two tilt angles becomes progressively smaller. At 1 keV there is no measurable difference between the two. For 1 keV, the energy is so low that irrespective of incident angle a major fraction of the ions is moving into the channels. Also, when comparing implants into crystalline and amorphous samples, the relative amount of channelling at 1×10^{18} cm^{-3} stays at least constant for the different energies. It is difficult to say

exactly, because for the lowest energies the the amorphous implant profiles are determines by the SIMS depth resolution.

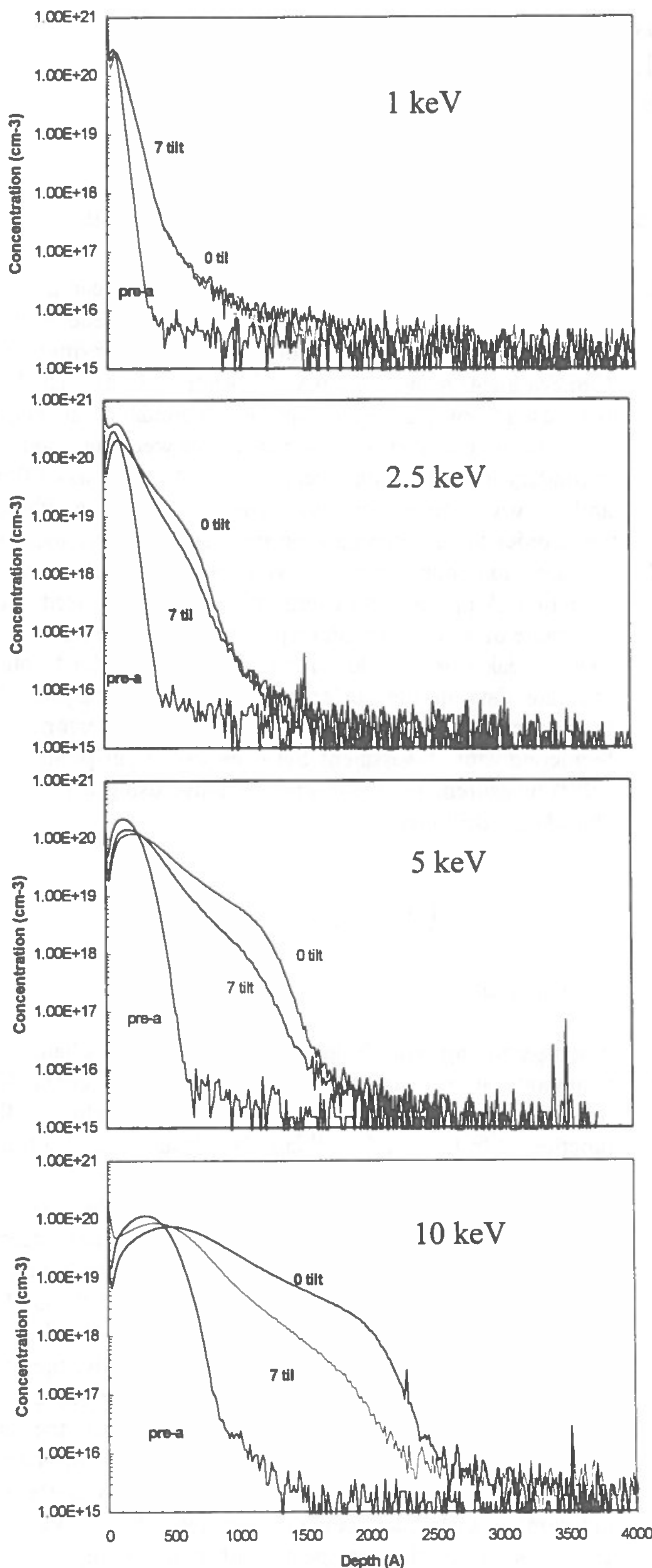

Figure 1: As-implanted profiles of a 5×10^{14} cm^{-2} B implant for three different implant conditions in the 1-10 keV range.

What is clear from these data al least is that the wafer tilting for suppressing channelling is useless at low energies. In fact, high tilt angles will only increase the shadowing effects due to surface topography, responsible for unwanted asymmetric device behaviour. Even though the tilt angle does not prevent channelling for these energies, it is clear

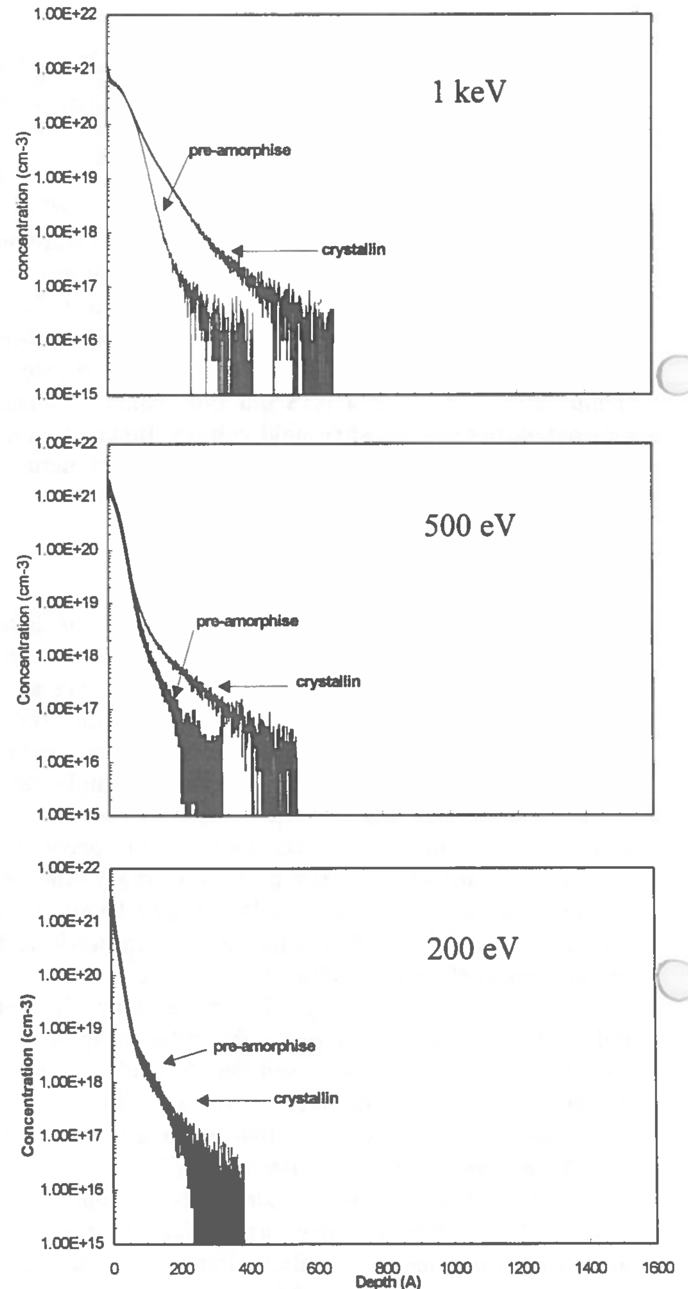

Figure 2: As-implanted profiles of a 5×10^{14} cm^{-2} B implant into crystalline and a Ge-preamophised wafer for energies of 1 keV and below.

that implanting into pre-amorphised wafers does give a much shallower profile, at least as-implanted. Of course it remains to be seen how much of this initial advantage is retained after anneal. A pre-amorphisation implant however does limit throughput, so it is important to assess how much of an advantage it will give as far as junction depth is concerned.

Fig. 2 shows an $^{11}B^+$ implant at a dose of 5×10^{14} cm^{-2} for 1 keV, 500 and 200 eV. The tilt angle for this set of implants was 7° with a 0° twist angle. The pre-amorphisation in this case was with a 5 keV 1×10^{15} cm^{-2} Ge implant. This resulted in an amorphous layer of approximately 250 Å. As in fig. 1 the 1 keV implant shows considerable channelling still, but this becomes less for 500 eV and for 200 eV both implants are nearly identical. There was still a small difference noticeable between the crystalline case and the pre-amorphised. This indicated that the SIMS depth limit was not yet reached. One reason why the difference between crystalline and pre-amorphous tends to disappear at the lowest energies may be that for these energies and doses the boron implant itself amorphises the Si [2]. It can be concluded that for the lowest energies a pre-amorphisation step in order to reduce as-implanted junction depth is not necessary.

B. Annealed

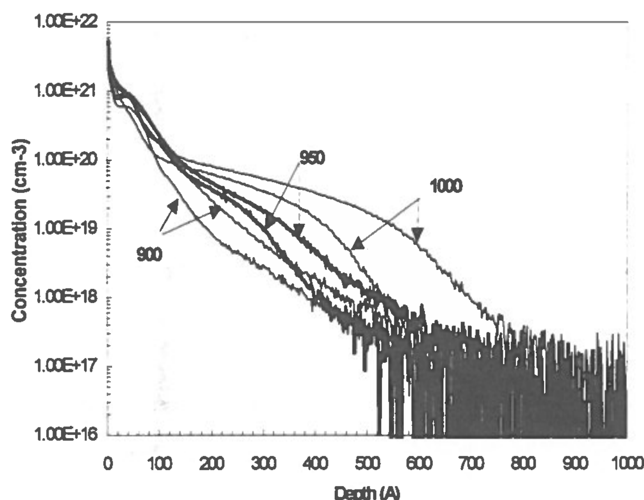

Figure 3: SIMS profiles for a 1 keV, 1×10^{15} cm^{-2} B implant for three different anneal conditions and in crystalline and pre-amorphised wafers. All anneals were for 10 s.

Fig. 3 shows a 1 keV, 1×10^{15} cm^{-2} $^{11}B^+$implant for three different anneal conditions and in crystalline and pre-amorphised wafers. The pre-amorphisation was a 10 keV, 1×10^{15} cm^{-2} Ge implant. The different anneal temperatures were 900, 950, and 1000 °C, all for 10 s. For every anneal temperature the pre-amorphised implant was the shallower one. This may be due to several reasons. As fig.1 and 2 show, at 1 keV there is still considerable channelling. The initial as-implanted profiles will therefore be shallower in the pre-amorphised case The sheet resistance $R_{\square}$ for the different anneals was also measured with four-point probe, and the results are listed in table I. It was found to be consistently higher for the pre-amorphised wafers. This could be due to a difference in as-implanted dose. However, the as-implanted profiles showed a dose of 1×10^{15} cm^{-2} and 9.7×10^{14} cm^{-2} for the crystalline and pre-amorphised wafers respectively. Another

Table I: Sheet resistance measurements for the 1 keV, 1×10^{15} cm^{-2} boron implant and different anneal conditions as shown in figure 3.

Temp (°C)	R- (Ω/□)	R□ (Ω/□) (Ge)
900	809	957
950	496	536
1000	272	375

effect may also influence the $R_{\square}$ data. The amorphous layer will absorb oxygen from the ambient before anneal. Upon annealing, this may then oxidise the surface layer. Boron will segregate into this oxide layer, thereby reducing the amount available for activation and also for diffusion.

The junction requirements for 0.18 μm CMOS are 540 ± 180 Å around 1×10^{18} cm^{-3} uniform channel concentration. All of the anneals shown in fig. 3 qualify for this. Depending on specific device requirements a balance can be struck between junction depth and sheet resistance.

C. Electrical results

The electrical results are obtained from PMOS transistors fabricated using a reference process and an optional shallow drain implant using an xR-LEAP ion implanter. Ten wafers were processed using a stripped 0.18 μm CMOS flow chart with electron beam patterning of the gate poly-silicon. This basic process flow is described elsewhere [3]. The reference process includes an 8 keV BF_2 implant. Additionally, wafers were implanted with 1 and 2 keV $^{11}B^+$, and with 3 keV $^{49}BF_2^+$. All implants were in quad mode, and all in crystalline substrates. The implant dose was 3×10^{14} cm^{-2} with a 10 s 1000 °C anneal, resulting in a 570 Å junction depth around the 1×10^{18} cm^{-3} level.

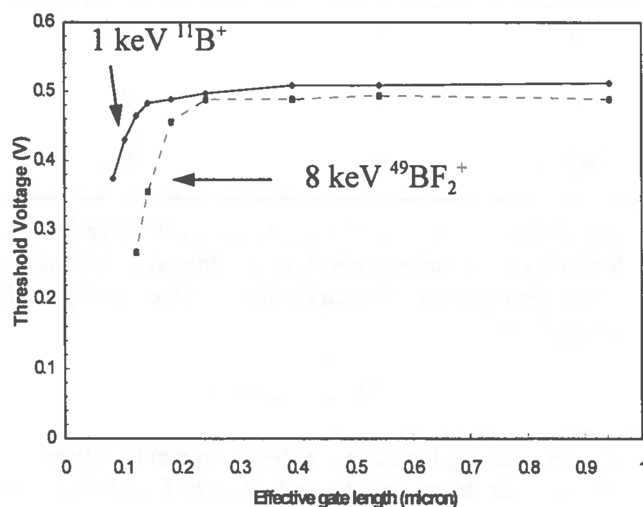

Figure 4: Threshold voltage behaviour for two different implants and effective gate lengths between 1 and 0.1 μm.

All conditions showed working transistors with threshold voltage behaviour and subthreshold characteristics as

expected. Fig. 4 shows the threshold behaviour for two implants: the reference 8 keV $^{49}BF_2^+$ implant and a 1 keV $^{1}B^+$ implant. As can be seen, the 1 keV implant showed much improved roll-off behaviour. Transistor asymmetry was measured by comparing drive current in forward and reverse mode, i.e. source and drain interchanged. The asymmetry is listed in table II.

Table II: Transistor asymmetry for different implanted species and energies.

species	energy (keV)	asymmetry (%)
B	1	1.5
B	2	3.0
BF_2	3	1.0
BF_2	8	4.5

The numbers are averaged over transistors spread across the wafer. It can be seen that the 8 keV $^{49}BF_2^+$ reference process gives the largest asymmetry.There seems to be a tendency for better symmetry with lower boron energy, but additional data is required to confirm this trend. Finally, gated diode structures were used to measure junction leakage. The results

Table III: Junction leakage current for different implanted species and energies measured with gated diode structures.

Species	energy (keV)	Leakage (nA)
B	1	6.2
B	2	2.7
BF_2	8	2.6

are shown in table III. No significant difference in junction leakage was observed indicating that the level of damage and unwanted impurities around the junction were comparable for all implants.

IV. Conclusions

The channelling behaviour of boron implants between 1 and 10 keV has been investigated. It was found that, for the lowest energies, there was little or no difference between a 7° and a 0° tilt implant. This implies that going to normal incidence implants for shallow drain extensions will not adversely effect junction depth. At the same time, shadowing effects will be eliminated. By comparing crystalline to pre-amorphised wafers it was found that considerable channelling was still occurring in this energy range. Decreasing the implant energy to 200 eV showed that for these energies channelling behaviour is similar for crystalline and pre-amorphised Si. This implies that for the lowest energies pre-amorphisation in order to reduce channelling is no longer. Finally, PMOS transistors with low energy boron drain extension implants showed excellent electrical characteristics, proving that this type of implant is a viable option for 0.18 µm CMOS and beyond.

V. References

[1]. Semiconductor Industry Association, "The National Technology Roadmap for Semiconductors", 1997 Edition.

[2]. E.J.H. Collart, M. Heijdra, K. Weemers, Y. Tamminga, J.G.M. van Berkum, and M. Verheijen, "Low energy (0.1-10 keV) $^{11}B^+$ ion implanatation damage characterisation using Rutherford Backscattering Spectrometry", this conference.

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