A high-linearity CMOS receiver achieving +44dBm IIP3 and +13dBm B_{1dB} for SAW-less LTE radio

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LTE-advanced wireless receivers require high-linearity up-front filtering to prevent corruption of the in-band signals by strong out-of-band (OOB) signals and self-interference from the transmitter. SAW duplexer filters are generally used for this purpose, but supporting the plethora of existing and new bands becomes troublesome with separate filters for each band. In this paper we explore the possibility of combining an isolator with on-chip filtering. However, even with 15dB isolation, the on-chip filter needs to deal with up to +10dBm TX leakage and -15dBm OOB blocking which requires an extremely high IIP3 around +50dBm and IIP2 around +90dBm. Recently inductor-less tunable N-path filter based receivers achieved >10dBm compression point and good IIP3 of 20-30dBm. In order to further improve the receiver linearity to approach the extremely high IIP3 requirement for a SAW-less receiver, a high-linearity N-path bandpass/notch filter topology and receiver architecture are proposed in this paper.

Fig. 1 shows the conceptual diagram of the proposed blocker-rejection receiver, where the *LC* tanks are implemented by N-path filters. The *LC* tanks act as high impedance for in-band signal. Input voltage signal is converted to current by mixers with series resistor R_I to reduce voltage swing and realize impedance matching before down conversion. The RF current is down-mixed and delivered directly to the baseband (BB) TIA which simultaneously provides a low ohmic termination of the mixer, *I-V* conversion of the BB

current and first order channel filtering ($R_F//C_F$). The *LC* tanks become low impedance for OOB signals. The strong OOB blockers are first attenuated by the bandpass filter and then converted to current by R_I. The following notch filter blocks in-band signals but passes OOB blockers which are also converted to current by R_N. Due to the differential structure and circuit symmetry, the BB nodes of passive mixers become virtual ground and OOB blockers will circulate in the RF domain without entering the BB TIA. The proposed receiver equivalently performs 1st stage blocker voltage reduction and 2nd stage blocker current bypassing to obtain superior selectivity.

N-path filters implemented with passive switches and capacitors can offer good linearity. A NMOS switch in series with a capacitor can perform mixing if the on time of the switch is much smaller than the RC time constant at the input, or act as a track-and-hold circuit (T&H) while the on time of the switch is much larger than RC time constant at the input. N-path filters make use of this mixing regime and the challenge is now to realize extreme linearity. Bootstrapped NMOS switches with constant V_{GS} and V_{GD} are widely used to push linearity in T&H circuits. However, this technique can't improve the linearity of mixing operation since one terminal of an NMOS mixer switch is RF signal while the other is IF signal. Hence V_{GS} and V_{GD} of the NMOS mixer switch cannot both be constant. N-path filters are composed of simple passive MOS switches in series with capacitors which can offer good linearity. However, the achievable IIP3 in previously published 1-2GHz designs is about 25dBm. The passive NMOS switches in these designs suffer from varying V_{GS}, V_{GD} and large V_{DS} limiting the achievable IIP3. To alleviate this problem, a bottom-plate mixing N-path filter is proposed and shown in Fig. 2. In the first stage bandpass filter design, M_1-M_4 are NMOS switches with large *W*/*L* performing mixing operation while the other NMOS switches with small *W*/*L* are applied to set the DC bias point of the virtual ground D_1-D_4 and S_1-S_4 between the capacitors. When $\Phi_0/\Phi_{90}/\Phi_{180}/\Phi_{270}$ is high, V_D and V_S of the NMOS switch are almost shorted to virtual ground to

simultaneously obtain rather constant V_{GS}, V_{GD} and small V_{DS} while still providing the mixing operation. The linearity of the first bandpass N-path filter is hence greatly improved by the proposed bottom plate mixing. Furthermore, one shared NMOS switch can be used instead of two switches in the traditional architecture and the maximum OOB rejection is hence improved from R_{SW}/R_S to $0.5R_{SW}/R_S$. This bottom-plate mixing technique can also be applied to the N-path notch filter design. For OOB signals, the N-path notch filters offer current bypassing paths. The source (I+/I-/Q+/Q-) of the mixer switches serves as virtual ground due to differential symmetry. Similar to the bandpass case, constant V_{GS}, V_{GD} and small V_{DS} can be achieved, offering mixing with very good linearity. R_I and R_N for V to I conversion are implemented with top-metal resistors (15ohm) to prevent linearity degradation. In the proposed receiver, both bandpass and notch filters are driven by the same 4-phase 25-% duty-cycle clocks. Inverter-based BB TIAs offer low noise with good power efficiency [1]. However, most designs use an extra CMFB circuit to reduce the common-mode gain which consumes extra power and adds noise. In the proposed TIA design, two PMOS transistors operating in the saturation region are added. A high differential gain of $(gm_n+gm_p)(r_{on}||r_{op})$ is achieved where r_{on} and r_{op} are the output impedance of gm_n and gm_p. For common mode input gm_p is degenerated and the TIA output is diode-connected with output impedance of $1/gm_{CM}$ giving a low common mode gain of gm_n/gm_{CM}. Note that normally this type of CMFB operates not in saturation but in triode with small gm_{CM} and cannot offer low common mode gain.

The test chip has been fabricated in TSMC a 1P7M 28nm technology and active area is 0.49mm^2. A 1:1 balun is used to generate a differential RF input. Measurements are done at f_{LO}=1GHz unless otherwise specified. The off-chip balun loss is de-embedded and measurement results are referred to the RF input of chip. Fig. 3 shows the measured gain (BW is 13MHz) and S_{11} as a function of RF frequency for some representative f_{LO}. Measured blocker 1dB gain compression point (B1dB) as a function of frequency offset

Δf from the carrier and B1dB as a function of f_{LO} are also shown. The proposed receiver achieves a high B1dB of 13dBm for Δf=80MHz. IIP3 and IIP2 measurement are performed as two-tone test with IM3 and IM2 products located at a BB frequency of 500kHz. At Δf=80MHz very high IIP3 of 44dBm and IIP2 of 90dBm are achieved as shown in Fig. 4. IIP3 and IIP2 as a function of Δf are also plotted. Receiver linearity increases with Δf due to higher OOB rejection. Fig. 5 shows the measured DSB NF and gain as a function of f_{LO}. The NF and gain degradation at higher f_{LO} is due to parasitic capacitance at the RF input causing attenuation at high frequency. The presence of strong blockers degrades the NF due to reciprocal mixing. At Δf=80MHz measured desensitization is only 0.6dB for a 0dBm blocker and only 3.6dB for a 10dBm blocker at f_{LO}=0.7GHz. A performance summary and comparison with previous work is shown in Fig. 6. Compared to prior art the receiver proposed here achieves significantly higher IIP3 and IIP2 while maintaining comparable NF and power consumption.

Acknowledgement:

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References:

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[3] S. Hameed et al., “A Programmable Receiver Front-End Achieving >17dBm IIP3 at <1.25×BW Frequency Offset,” *ISSCC Dig. Tech Papers,* pp. 446-447, Feb. 2016.

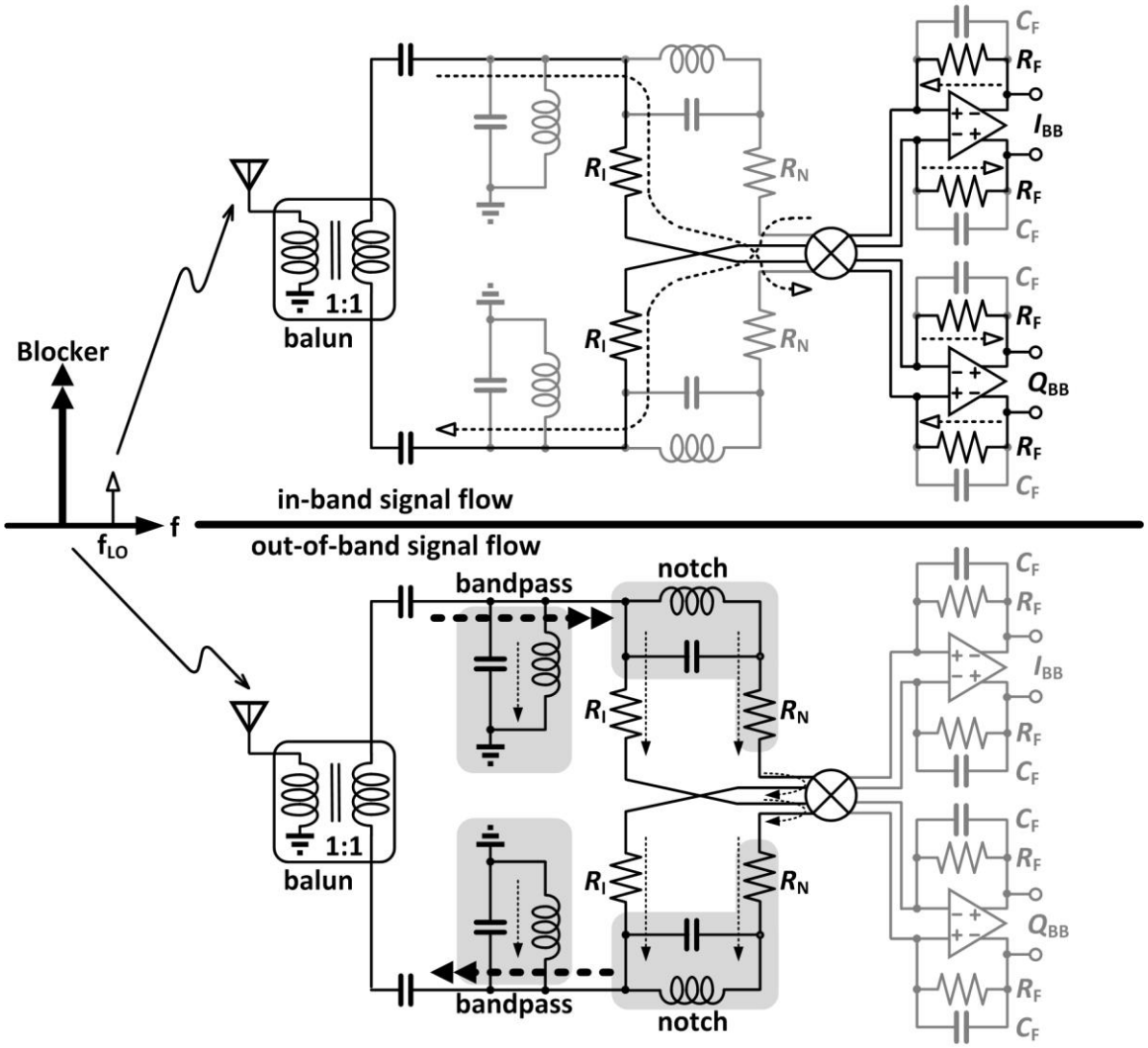

Figure 1: The conceptual diagram of the proposed blocker-rejection receiver.

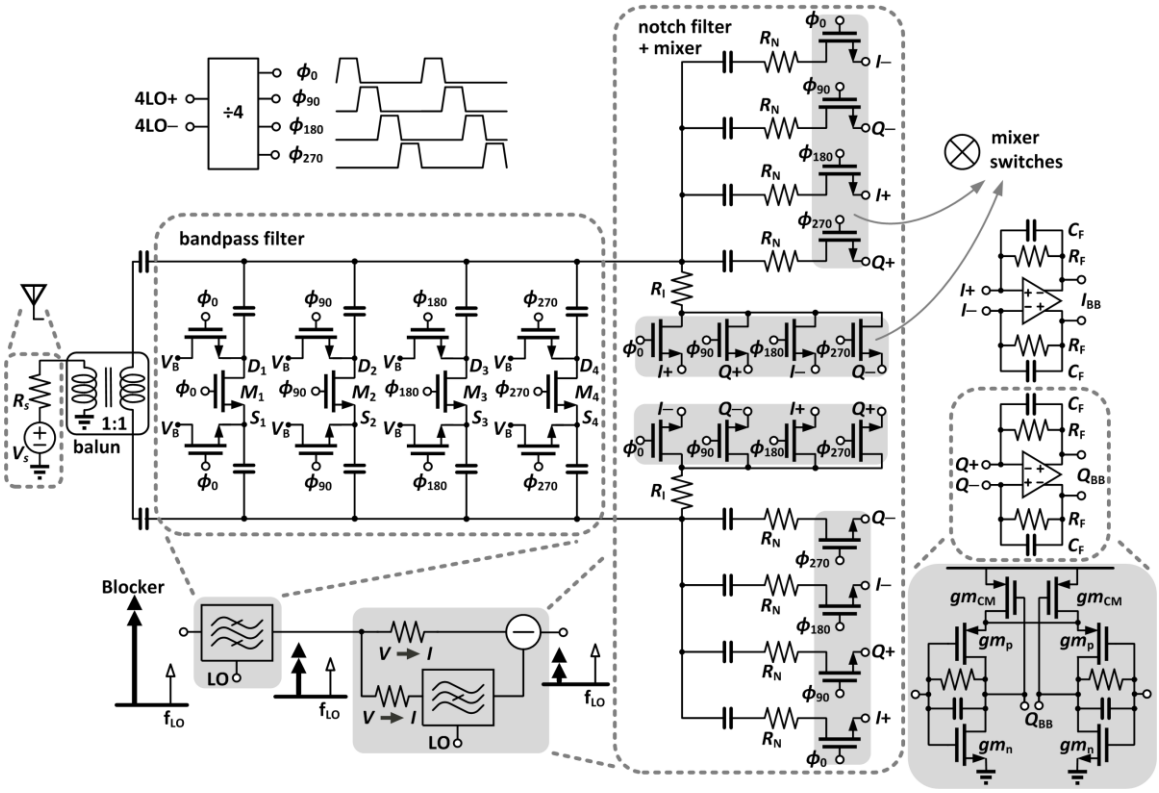

Figure 2: Circuit details of the proposed receiver.

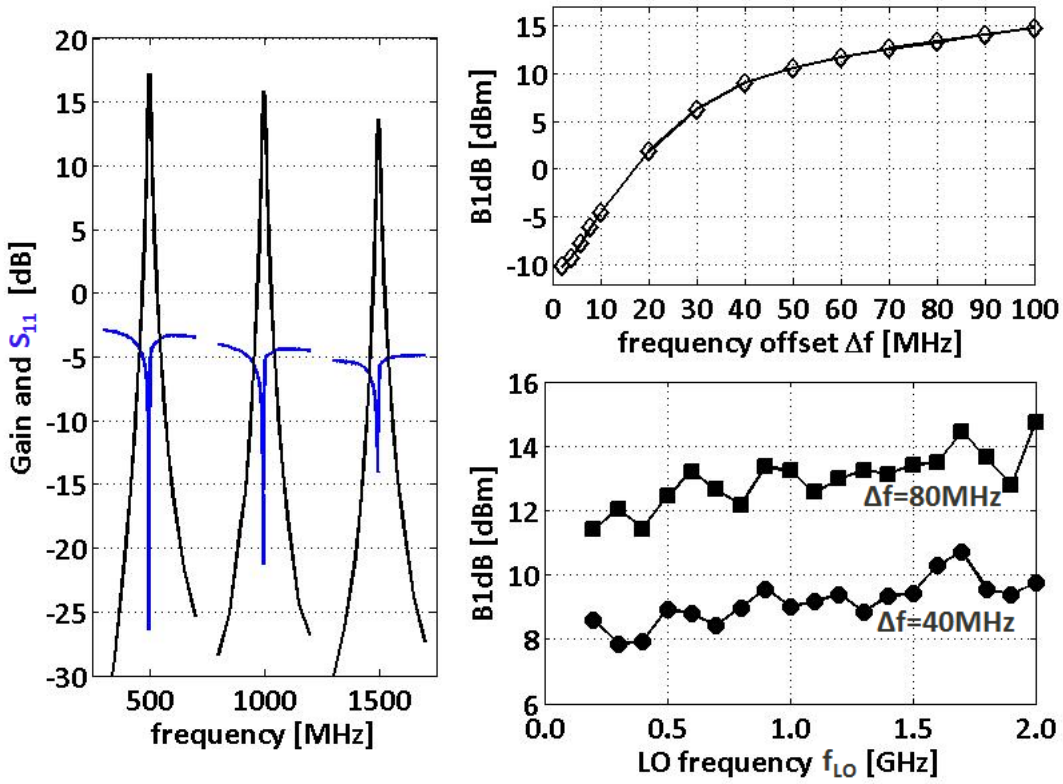

Figure 3: Measured gain and S_{11} for three LO frequencies; Measured B1dB versus blocker frequency offset Δf at f_{LO}=1GHz and B1dB versus f_{LO} for Δf=40MHz and Δf=80MHz (The applied weak in-band tone frequency is f_{LO}+500kHz).

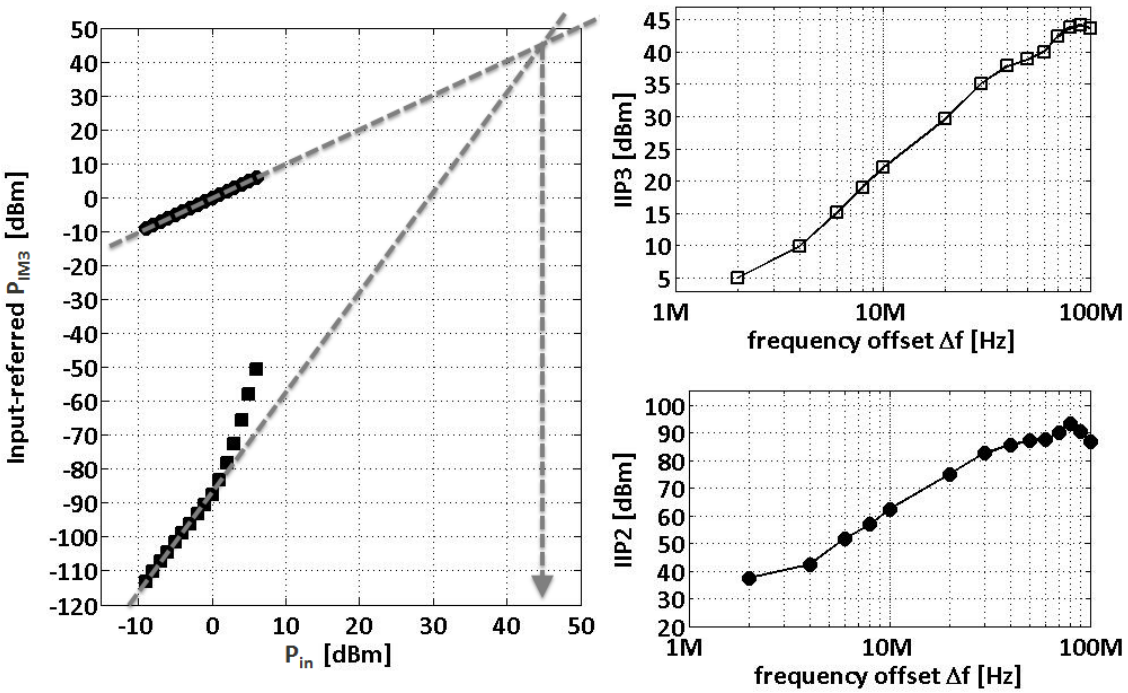

Figure 4: Measured IIP3 for blocker frequency offset Δf=80MHz, IIP3 and IIP2 as a function of blocker frequency offset.

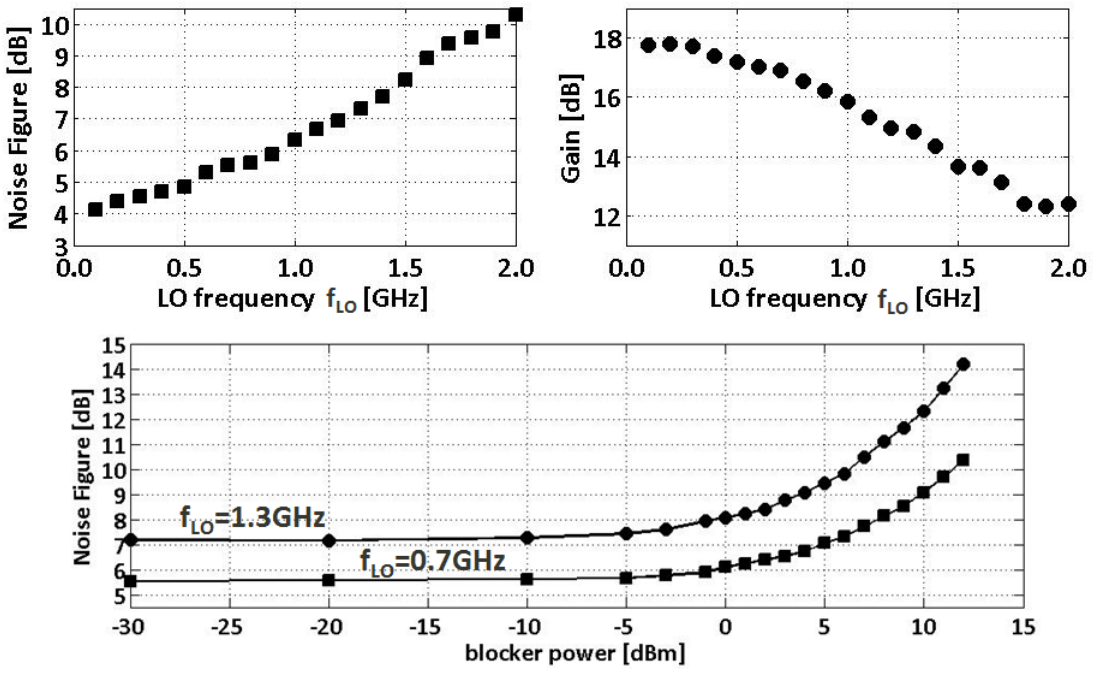

Figure 5: Measured DSB NF and gain as a function of LO frequency f_{LO}, and blocker NF (blocker frequency offset Δf=80MHz) for f_{LO}=0.7GHz, f_{LO}=1.3GHz.

	[2]	[1]	[3]	This Work
Architecture	Mixer first	Mixer first With Noise Cancelling	Filtering by Aliasing	N-path filters with bottom -plate mixing
Technology	65nm	40nm	65nm	28nm
RF frequency [GHz]	0.05-2.4	0.08-2.7	0.1-1	0.1-2.0
Gain[dB]	80	72	18.9	16
BW[MHz]	20	4	2.4-40	13
OOB-IIP3[dBm]	27 (Δf=100MHz)	13.5 (Δf=80MHz)	17 (Δf/BW=1.2)	44 (Δf=80MHz)
OOB-IIP2[dBm]	58	55	60	90
B1dB[dBm]	10 (Δf=100MHz)	-2 (Δf=80MHz)	8 (Δf/BW=4)	13 (Δf=80MHz)
NF[dB]	5.5	1.9	6.5	6.3(f_{LO}=1GHz)
Supply[V]	1.2/2.5	1.2/2.5	1.2/1.0	1.2/1.0*
Power[mW]	60	27-60	56-62	38-96**
Area[mm^2]	2.5	1.2	2	0.49

*1.0V for BB amplifiers, 1.2V for clock generator

**power consumption of BB amplifiers=30mW, clock generator power at 1GHz f_{LO}=36mW

Figure 6: Result summary and comparison with prior art.

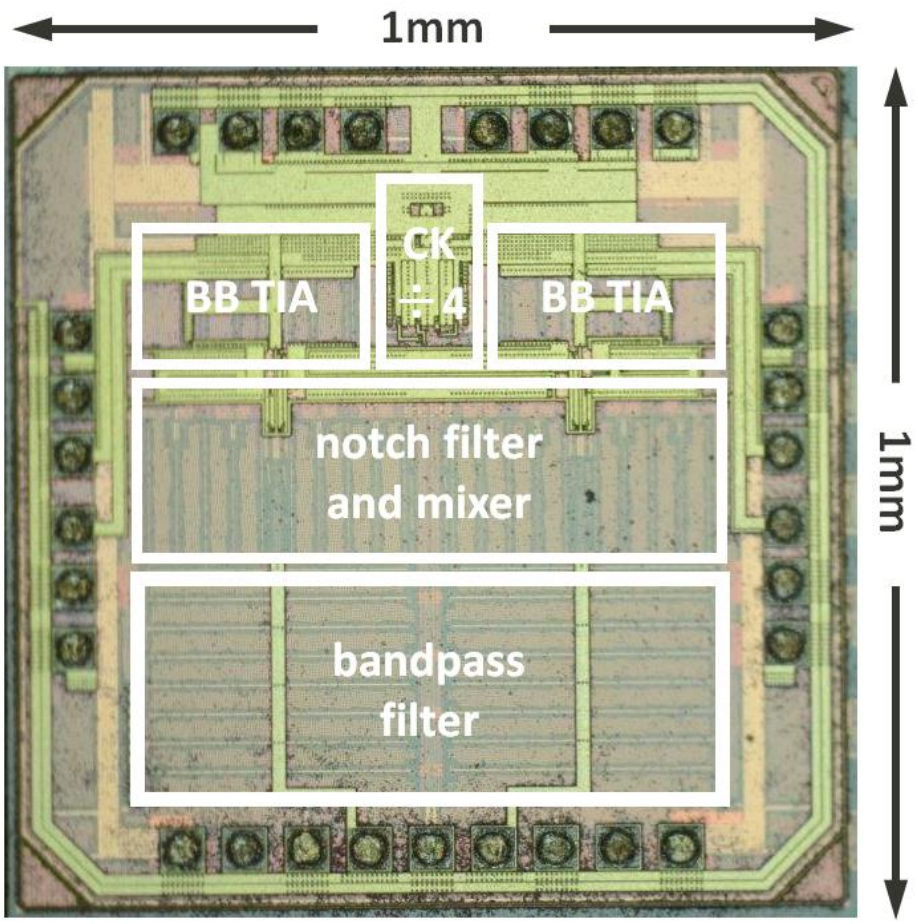

Figure 7: Chip photo