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Effects of Gate Depletion and Boron Penetration on Matching of Deep Submicron CMOS Transistors

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Abstract

This paper presents new insights into the mechanisms of gate depletion and boron penetration in deep submicron CMOS technologies. MOSFET matching measurements show that these effects are stochastic in nature, and are associated with the gate poly-Si grain size distribution. Moreover, this work demonstrates that these effects can strongly degrade transistor matching performance of future CMOS generations.

Introduction

Stochastic variations of microscopic device properties like dopant distribution fluctuations, edge roughness, etc. are major causes for device performance variations in CMOS technologies [1,2,3]. Reduction of parametric differences (mismatch) between identically designed devices is extremely important for high performance analog small signal processing in mixed signal circuits (ADC's, DAC's, PLL's, etc.), as well as for tight control of in-chip variations in ULSI memories [1]. Transistor matching studies are very suitable for investigating statistical differences between supposedly identical -closely spaced- transistors [2]. V_t mismatch is commonly assumed to be predominantly caused by random dopant fluctuations in the channel region [1,2,3].

Gate depletion and boron penetration are notorious process hazards for submicron CMOS processes with their very thin gate oxides, dual flavored poly-Si and low temperature budgets [4,5]. The thermal budget must be sufficient to achieve adequate gate activation to avoid performance loss caused by gate depletion. On the other hand, the temperature budget must be reduced to limit short-channel effects, as well as to avoid PMOST threshold voltage reduction due to boron penetration.

This paper shows that transistor matching degrades strongly when gate depletion or boron penetration occurs. This means that these effects must be interpreted as stochastic effects, associated with the grain size distribution in the poly-Si gate and how the dopant diffuses in the gate and through the gate dielectric (figure 1).

Experimental

Several CMOS and uni-channel process development lots were used for this study. They were based on typical 0.25, 0.18 and 0.13 μm CMOS process flows [6,7]. For these particular experiments the gate oxide thicknesses were 6, 4.5 and 3.5 nm respectively. The poly-Si gates were deposited amorphous (200 nm or 150 nm), lightly phosphorous doped, recrystalized, patterned and finally doped using the Source/Drain implants of 2.5E15 BF_2^+ (20 or 15 keV) or 4E15 As^+ (40 or 25 keV) respectively. The temperature of the 20 seconds RTA step used for gate dopant activation was the main variable for this particular study.

A standard set of matched transistor pairs, ranging from W/L=10/10 down to 10/0.3 and 0.4/10 dimensions, were used to assess the matching performance of deep submicron CMOS technologies. V_t mismatch is characterized by the standard deviation $\sigma_{\Delta Vt}$ of the V_t difference (ΔV_t) between pairs of supposedly identical transistors. Matching of a particular technology is characterized by the so-called area scaling factor A_{Vt}, being the slope of $\sigma_{\Delta Vt}$ vs. $1/\sqrt{(WL)}$ [2].

V_t's were measured using a linear region three-point technique [8] on a high performance semi-automatic DC parametric probe station. The reproducibility of these V_t mismatch measurements is better than 100 μV.

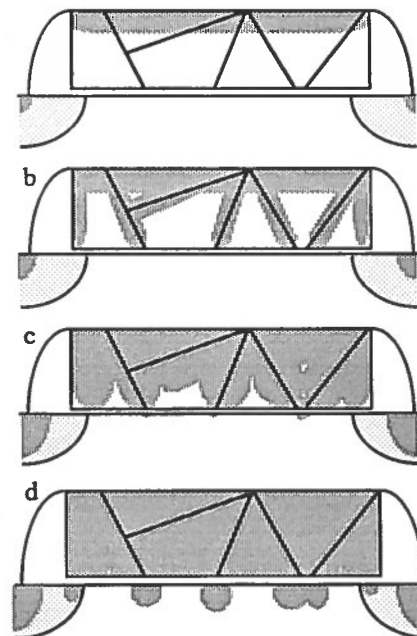

Figure 1. Schematic representation of poly-Si grain doping stages: a: after implant, b: fast diffusion along grain boundaries, c: almost fully doped, d: local boron penetration.

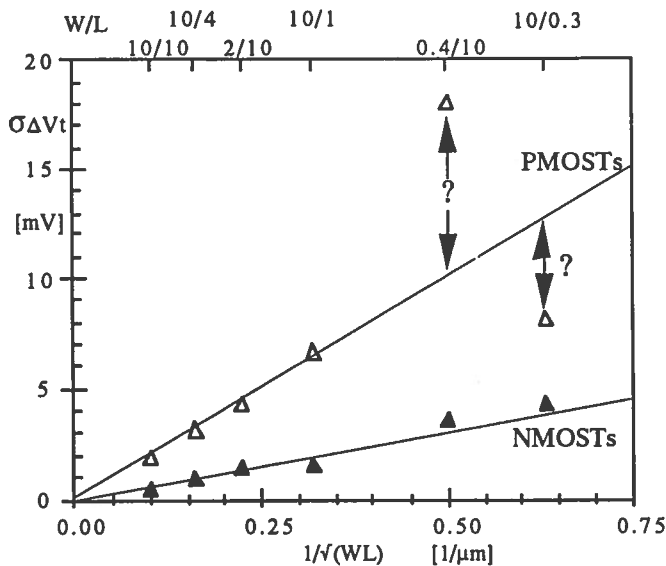

Figure 2. V_t matching area scaling for 0.25 µm CMOS Technology. Lines: NMOSTs (solid triangles) A_{Vt_N} = 6 mVµm, PMOSTs (open triangles) A_{Vt_P} = 20 mVµm. Arrows indicate large deviations from expected behavior for 0.4/10 and 10/0.3 PMOSTs.

Results

Figure 2 gives an example of $\sigma_{\Delta Vt}$ area-scaling for N- and PMOSTs from an 0.25 µm CMOS experiment. The NMOST A_{Vt} of 6 mVµm is close to the expected value for this process generation [2,3]. The PMOST $\sigma_{\Delta Vt}$'s are much higher in this example, also featuring anomalous area-scaling both for the narrowest as well as for the shortest PMOSTs.

Analysis of transfer characteristics of PMOS transistors (e.g. figure 3) reveals that the uncommonly high mismatch $\sigma_{\Delta Vt}$ coincides with an abnormal turn-on behavior of PMOSTs on these wafers. The transconductance characteristic (g_m vs. V_{gs}) demonstrates this anomaly most clearly, showing a double peak in the g_m-V_{gs} curve. These type of characteristics have previously been reported and explained in terms of gate depletion followed by inversion in the gate poly-Si [9,10].

Figure 4 introduces the key experiment of this study: it shows the influence of the dopant activation anneal temperature on $\sigma_{\Delta Vt}$ for large PMOSTs. Strong increases of $\sigma_{\Delta Vt}$ for low as well as for high RTA temperatures are observed. Also indicated in figure 4 are the expected values for $\sigma_{\Delta Vt}$ for W/L=10/10 devices in these technologies as can be derived from [1, 2, 3]. This demonstrates the poor matching performance encountered in these experimental lots: even under the optimum RTA condition the $\sigma_{\Delta Vt}$ is more than 3 times the expected value. This corresponds to a 10 times larger transistor area to reach the theoretical matching performance, since $\sigma_{\Delta Vt}$ scales with $1/\sqrt{(WL)}$.

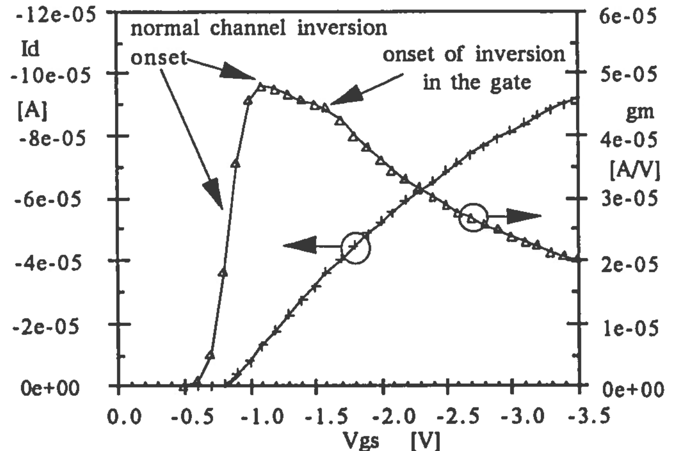

Figure 3. Linear region drain current (+) and transconductance (Δ) for a W/L=10/1 P-channel transistor (0.25 µm technology).

Discussion

Figure 5 shows that major changes of the double peak g_m curve are observed on wafers from this experiment. The magnitude of the gate inversion peak clearly decreases with increasing RTA temperature. This suggests that the transistor matching changes for T≤ 1030°C (figure 4) are related to incomplete gate activation. Note that a change of the mismatch standard deviation as determined using closely spaced, identically designed components, must be interpreted as a change of a mechanism that causes random differences on a microscopic scale. So figures 4 and 5 lead to the conclusion that the observed $\sigma_{\Delta Vt}$ increases for low activation temperatures

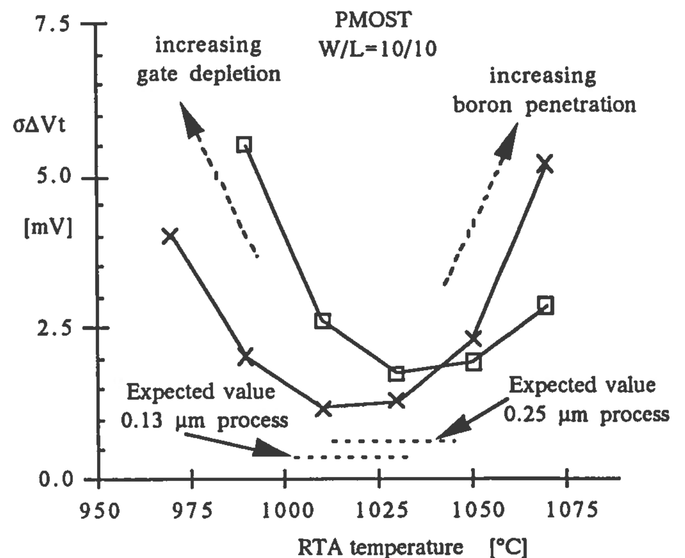

Figure 4. Vt mismatch standard deviations of large PMOSTs as a function of dopant activation RTA temperature. Squares: 0.25 µm technology, crosses: 0.13 µm technology.

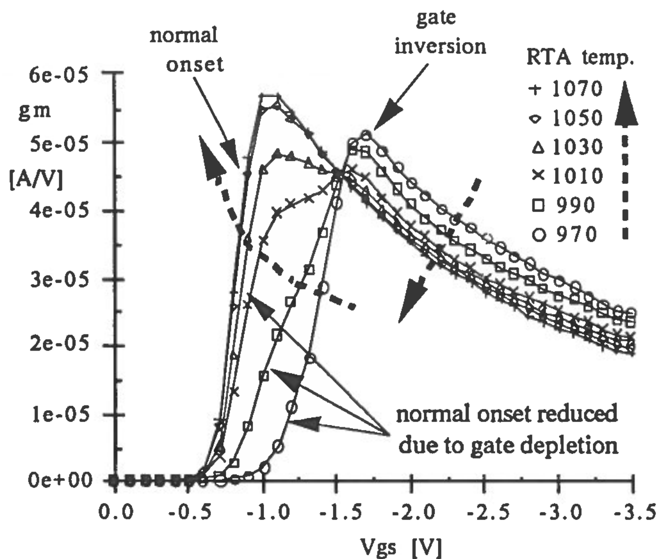

Figure 5. Linear region transconductance graphs for W/L=10/1 PMOSTs (0.25 μm technology) for different RTA temperatures.

are caused by **random microscopic occurrences of gate depletion.** We attribute this to inhomogeneous doping of poly-silicon grains that form the gate electrode.

Figure 1 gives schematic representations of the poly-Si doping that we envisage in our experiments. After the hard drain implant (figure 1a), grain boundaries are very rapidly doped (figure 1b), even at the lowest RTA temperature [11]. Lightly doped regions inside grains lead to very localized gate depletion regions, resulting in local V_t increases. Since the size and number of these non-uniformities vary randomly from transistor to transistor, this is observed as an increased V_t mismatch standard deviation. When a larger temperature budget is applied, the poly-Si will become more homogeneously doped (figure 1c), and hence the non-uniformities in device behavior resulting from gate depletion will be less.
The plausibility of this explanation was confirmed using SUPREM and MEDICI simulations.

Poly-Si grain boundary effects can also be used to explain the increased $\sigma_{\Delta Vt}$'s for higher RTA temperatures in figure 4. We must assume that boron penetration through the gate oxide is again a microscopic random effect. Highly doped grain boundaries serve as the diffusion sources for boron penetration, which will therefore occur preferentially at poly-Si grain boundary locations (figure 1d). Again these small regions with lower V_t's are distributed randomly over large transistors and will hence result in increased $\sigma_{\Delta Vt}$'s.

The occurrence of gate depletion/inversion and boron penetration at low and high RTA temperatures respectively were also confirmed by long channel threshold voltage shifts and large area capacitor C-V measurements. These techniques however, can only confirm the global -averaged- effects and do not show the microscopic -statistical- nature of these effects that is demonstrated so convincingly by our transistor matching measurements.

A mismatch effect will only follow a $1/\sqrt{(WL)}$ relationship when the device dimensions are large compared to the correlation distance of the stochastic disturbance effect [2], in this case the poly-Si grain size. SEM analysis of partially de-processed and preferentially etched wafers indicates that the poly-Si grain sizes in these experiments are of the order of 0.2 to 0.3 μm and independent of the RTA temperature. This explains the disturbed area-scaling behavior for small dimension devices. The disproportionately large $\sigma_{\Delta Vt}$ for narrow P-channel (0.4/10) devices at low RTA temperatures (figure 2) is explained by assuming that some poly-Si grains are wide enough to completely block transistors with lightly doped (high V_t) regions (figure 6). This explanation is supported by additional observations that the double transconductance peaks are even more pronounced for narrow transistors than they are for short transistors. Figure 7 demonstrates that the excessive $\sigma_{\Delta Vt}$ for narrow (0.4/10) devices disappears when a higher RTA temperature is applied. This means that even the largest grains are doped homogeneous.

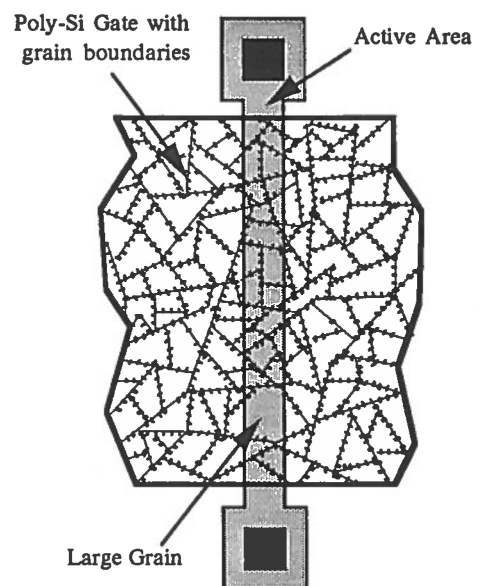

Figure 6. Schematic plan-view of narrow transistor where gate depletion in a large poly-Si grain can 'block' the channel.

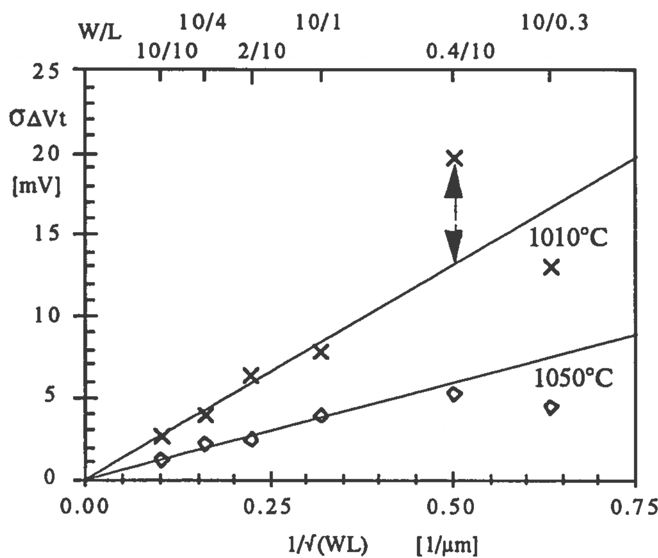

Figure 7. PMOST Vt matching area scaling for 0.18 µm technology crosses RTA@1010 °C; diamonds RTA@1050 °C. Lines : AVt ≈ 27 mVµm and 12 mVµm, respectively. Arrow indicates excessive mismatch for narrow transistor that disappears for higher RTA temperature.

Short (10/0.3) transistors have a more favorable grain boundary orientation since these are by definition aligned along the S/D spacer edge and poly-Si grains can be no wider than the transistor length. This explains the relatively lower $\sigma_{\Delta Vt}$'s for 10/0.3 PMOS transistors in figures 2 and 7.

Finally, figure 8 demonstrates that increased $\sigma_{\Delta Vt}$'s due to gate depletion are also observed for **NMOS transistors** when low RTA temperatures are used, be it that the mismatch levels are much lower. Moreover, the expected theoretical levels [1,2,3] are reached for the optimum RTA conditions. What remains is the observation that the increased $\sigma_{\Delta Vt}$'s for low RTA temperatures again indicates that random microscopical differences also determine the gate depletion effects in these n-channel transistors.

Conclusion

Based on MOSFET matching measurements this paper shows that gate depletion and boron penetration are stochastic effects that are associated with the poly-Si grain size distribution. Moreover, this work demonstrates that these effects can contribute significantly to transistor performance variations in deep submicron CMOS.

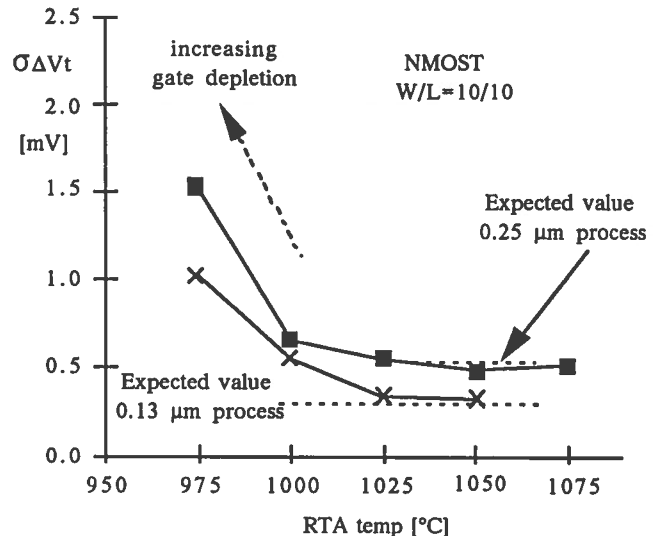

Figure 8. Vt mismatch standard deviations of large NMOSTs as a function of dopant activation RTA temperature. Squares: 0.25 µm technology, Crosses: 0.13 µm technology.

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