Communication

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Localized Heating and Switching in $MoTe_2$-Based Resistive Memory Devices

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ABSTRACT:

Two-dimensional (2D) materials have recently been incorporated into resistive memory devices due to their atomically thin nature, but their switching mechanism is not yet well understood. Here we study bipolar switching in $MoTe_2$-based resistive memory of varying thickness and electrode area. Using scanning thermal microscopy (SThM), we map the surface temperature of the devices under bias, revealing clear evidence of localized

heating at conductive “plugs” formed during switching. The SThM measurements are correlated to electro-thermal simulations, yielding a range of plug diameters (250 to 350 nm) and temperatures at constant bias and during switching. Transmission electron microscopy images reveal these plugs result from atomic migration between electrodes, which is a thermally-activated process. However, the initial forming may be caused by defect generation or Te migration within the $MoTe_2$. This study provides the first thermal and localized switching insights into the operation of such resistive memory, and demonstrates a thermal microscopy technique that can be applied to a wide variety of traditional and emerging memory devices.

Two-dimensional (2D) materials have gained much interest in the last decade for scaled electronics and optoelectronics due to their tunable electrical, optical, and thermal properties.[1-3] More recently, they have been incorporated into memory devices,[4] either as heat confinement layers in phase change memory (PCM),[5-6] or as switching layers in resistive memory devices.[7-12] Transition metal dichalcogenides (TMDs), a class of 2D materials, have been suggested for phase engineering applications because many Group VI TMDs can exist in both semiconducting and metallic phases.[13-14] Molybdenum ditelluride ($MoTe_2$) is particularly interesting for these applications because it was predicted to have the lowest-energy phase boundary between the semiconducting and metallic phases.[14] While some studies have demonstrated switching in TMD-based memory, the switching mechanism remains unclear and could result from a localized phase change, ion migration causing (reversible) conductive regions, or interactions with the electrodes.[7,10-12] The switching mechanism can either be thermal in nature like in PCM, or have a thermally-activated component like in resistive random access memory (RRAM), yet such aspects have not been investigated to date in TMD-based memory devices.

In this work, we use scanning thermal microscopy (SThM) to examine the thermal origins of switching behavior in $MoTe_2$-based resistive memory devices with varying $MoTe_2$ thickness and electrode area. We obtain spatial temperature maps of these devices under electrical bias and find evidence of localized heating due to a conductive plug which forms during switching. Because the SThM measurements only probe the temperature at the surface of the devices, we correlate our measurements to electro-thermal simulations to obtain insight into the size and temperature of the conductive region *within* the $MoTe_2$. We also perform cross-sectional transmission electron microscopy (TEM) of memory devices after switching and find that the conductive plugs likely result from contact metal (here Au) migration between the top and bottom electrodes. However, control experiments on $MoTe_2$ devices with graphite electrodes also show forming, suggesting this is initially triggered by Te or defect migration, rather than only by Au conductive bridge formation.

Figure 1a shows a side-view schematic of the devices, which consist of layered $MoTe_2$ between Au electrodes. The bottom and top electrodes (BE and TE) are patterned by electron beam (e-beam) lithography and deposited by e-beam evaporation with thicknesses of 45 nm and 80 nm, respectively. The $MoTe_2$ is grown by chemical vapor transport (CVT), which yields bulk crystals.[15-16] Thin layers (~10-55 nm thick) of $MoTe_2$ are mechanically exfoliated onto SiO_2/Si substrates and subsequently transferred onto Au BEs by a dry transfer process (see Supporting

Information Section 1 for details). E-beam evaporated SiO_2 (~65 nm) is used to electrically isolate the two electrodes, and ~10 nm Al_2O_3 deposited by atomic layer deposition (ALD) is used as a protective capping layer[17] above the TE, as shown in Figure 1a. The exfoliation, transfer, metal lift-off, and ALD steps are all performed in a N_2 glove box with < 3 ppm O_2 and < 1 ppm H_2O to prevent surface oxidation of the $MoTe_2$.

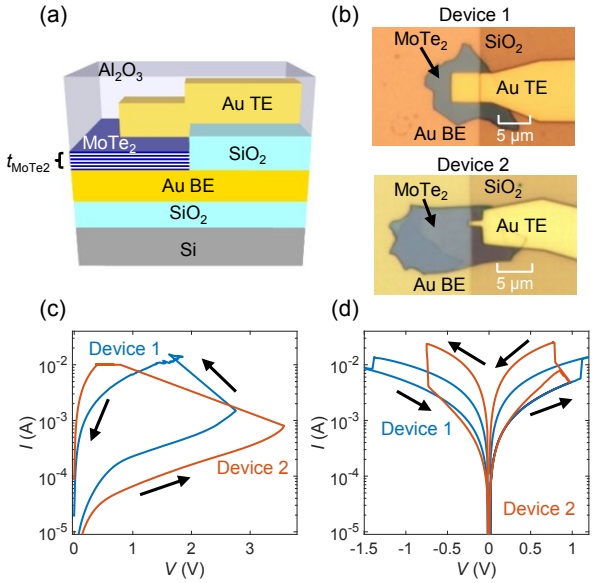

Figure 1. (a) Side-view schematic of $MoTe_2$ devices with a SiO_2 isolation layer between the Au top and bottom electrodes, as well as an Al_2O_3 capping layer. (b) Optical images of two devices, Device 1 (t_{MoTe2} ~ 30 nm) and Device 2 (t_{MoTe2} ~ 55 nm) with top electrode areas of 4.5 × 4.5 μm^2 and 0.7 × 0.4 μm^2, respectively. (c) Measured *I-V* characteristics showing initial forming of Devices 1 and 2, with the arrows corresponding to the voltage sweep direction. (d) Measured *I-V* characteristics showing subsequent bipolar switching of Devices 1 and 2.

Figure 1b displays optical images of two $MoTe_2$ devices (Device 1 and Device 2). Device 1 has Au TE area of 4.5 × 4.5 μm^2 and $MoTe_2$ thickness t_{MoTe2} ~ 30 nm, while Device 2 has Au TE area of 0.7 × 0.4 μm^2 and t_{MoTe2} ~ 55 nm. Figure 1c,d shows measured direct current vs. voltage (*I-V*) curves of the two devices, with the arrows illustrating the direction of the voltage sweep. The devices typically have initial resistances of 1 kΩ to 1 MΩ (depending on TE area and t_{MoTe2}). We use a modified three-dimensional (3D) Poole-Frenkel model[18-20] to fit our *I-V* curves during the forward sweep, as shown in Supporting Information Figure S1. At higher voltages, the devices undergo a "forming" step during a DC *I-V* sweep. We use a current compliance (10 μA to 10 mA)

and external series resistor (0.2 to 1 kΩ) to limit the amount of current. The devices transition to a low resistance state (LRS) with resistances R_{LRS} = 40 to 800 Ω, depending on the current compliance and series resistance used. When a voltage sweep of the opposite polarity is performed, the devices switch to a high resistance state (HRS) (the "RESET" step), and they transition back to the LRS after the polarity of the sweep is reversed again (the "SET" step). Figure 1d shows bipolar switching of Devices 1 and 2. We measured ~20 devices with similar forming and bipolar switching. We also present data on forming current, forming voltage, and R_{LRS} for devices with varying t_{MoTe2} and TE area in Supporting Information Figure S2.

To gain insight into the thermal origins of the device switching behavior, we use scanning thermal microscopy (SThM). SThM is an atomic force microscope (AFM) technique wherein a specialized AFM probe (here a temperature-dependent Pd resistor on a V-shaped SiN tip) is used in physical contact with a device to measure its surface temperature.[21-23] A voltage applied to the device induces Joule heating, which in turn causes the SThM probe to heat up. The electrical resistance of the probe changes with temperature, leading to a change in the output voltage (ΔV_{SThM}) of the SThM. ΔV_{SThM} is proportional to the temperature rise of the device surface (ΔT_S) above the ambient. The spatial resolution of these SThM probes is typically ~100 nm (depending on environmental conditions and calibration),[21-25] making it preferable to other techniques such as gate resistance thermometry, which gives average device temperature,[26] or Raman thermometry, which has good material selectivity but a diffraction-limited spatial resolution of ~0.5 μm.[22,25] (See Section 4 of the Supporting Information for measurement details, a discussion of spatial resolution, and calibration between ΔV_{SThM} and ΔT_S.)

Figure 2a shows a schematic of the setup, with the SThM probe on top of the Al_2O_3 surface. The Al_2O_3 (or some other insulator) is needed to electrically isolate the probe and the TE. Figure 2b displays an AFM image of the TE region of Device 1 (in the LRS), illustrating a bump (~15 nm high) that emerged on the Au TE after the forming step. An SThM image is simultaneously taken with no bias applied to the device and is used to flatten all subsequent images at nonzero bias (see Supporting Information Figure S3 and Section 4 for details). We then apply a voltage to the TE while grounding the BE (without a series resistor), as illustrated in Figure 2a. Figure 2c,d shows SThM images of Device 1 with input power P ~ 1.6 mW and 2.5 mW, respectively, and the color bar shows the ΔT_S range (0-30 K) using a calibration factor $F = \Delta V_{SThM}/\Delta T_S$ = 6.5 ± 0.5 mV/K.[24] The images show a hot spot on the TE, matching the location of the bump in Figure 2b,

becoming larger and hotter as we increase the input power. This localized heating suggests the formation of a conductive plug, and similar results have been observed for ~10 other devices. We point out that this is the first direct observation of localized switching visualized through thermal mapping TMD-based memory devices.

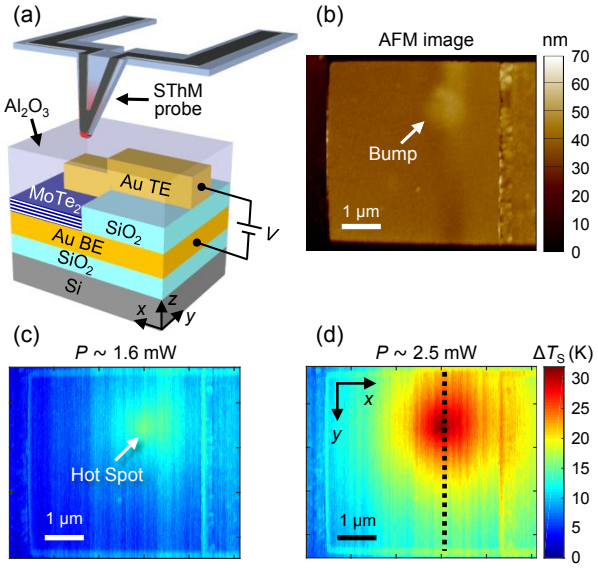

Figure 2. (a) Schematic of SThM setup, showing the probe on the surface of the Al_2O_3 capping layer and above the Au TE region. (b) AFM image of the top electrode region of Device 1, which is in the low resistance state. SThM images of Device 1 at power inputs of (c) $P \sim 1.6$ mW and (d) $P \sim 2.5$ mW. The color bar shows the temperature rise at the surface of the Al_2O_3 (ΔT_S), which was obtained using a calibration factor of 6.5 mV/K. The hot spots seen in (c) and (d) correspond to the bump on the top electrode in (b) and show evidence of localized heating due to a conductive plug in the device. The edges of the TE and SiO_2 can be seen because the SThM signal is affected by the topography of the sample.

Next, we correlate our experimental results to 3D electro-thermal simulations performed using finite element modeling (COMSOL® Multiphysics). These simulations allow us to estimate the temperature of the conductive plug during operation as well as the plug diameter (d_{plug}), based on the surface temperature obtained by SThM. Section 5 of the Supporting Information contains details of the simulations, and Table S1 shows the various parameters used. Figure 3a shows the ΔT_S profile of Device 1 along the black dashed line in Figure 2d. This reveals broad heating of the entire TE, including $\Delta T_S > 15$ K at the edges, due to significant lateral heat spreading.

We find that among the simulation parameters, the thermal boundary resistance (TBR) at the

$MoTe_2$-Au interfaces plays a key role, yet it is among the least well-known inputs (e.g. compared to thermal conductivities of Au or SiO_2). The simulated ΔT_S profiles in Figure 3b show the closest agreement with the SThM data for TBR ≈ 70 m^2KGW^{-1} and d_{plug} from 250 to 350 nm. The estimated TBR is equivalent to a thermal boundary conductance (TBC = 1/TBR) of ~14 $MWm^{-2}K^{-1}$, which is very similar to that found for other 2D materials.[6,25] We note the peak ΔT_S increases with increasing d_{plug}, unlike in metal-oxide RRAM devices.[24] Our simulations suggest this behavior is due to the electrical conductivity of the plug being only ~100× higher than that of the surrounding $MoTe_2$ unlike in metal-oxide RRAM where the conductive filament conductivity is $>10^{10}$ higher than that of the insulating metal-oxide surrounding it.[27-28] Therefore, the film surrounding the conductive plug in our devices also contributes to current conduction (and heating).

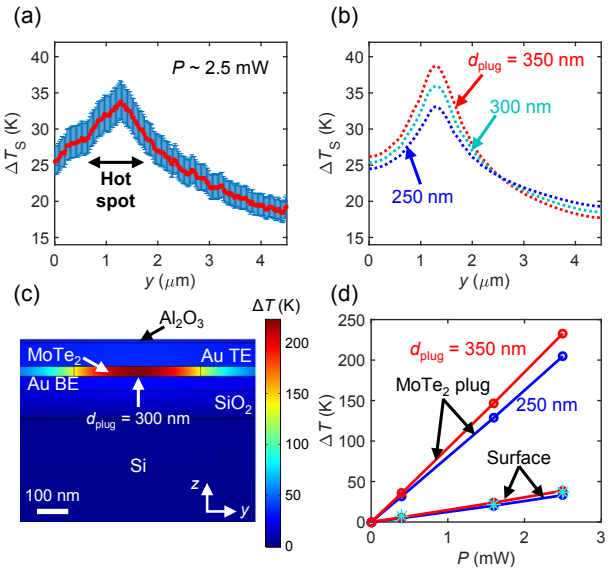

Figure 3. (a) Surface temperature profile from SThM measurement along the black dashed line in Figure 2d, with error bars. (b) Electro-thermal simulations of ΔT_S profiles for conductive plug diameters d_{plug} ranging from 250 to 350 nm at P ~ 2.5 mW. (c) Simulation of ΔT along cross-section of device at P ~ 2.5 mW for d_{plug} = 300 nm. (d) Simulated ΔT vs. P for different d_{plug} inside the $MoTe_2$ plug and at the surface of the device. The cyan stars correspond to ΔT_S from SThM measurements.

Figure 3c shows a cross-sectional view of the simulated temperature distribution within the device for d_{plug} = 300 nm and P = 2.5 mW. The image has been cropped to focus on the conductive plug region (the silicon is actually 20 μm thick in our simulations). As expected, the hottest region

is in the $MoTe_2$ where the conductive plug is formed, with a peak $\Delta T_{plug} \approx 223$ K. There is substantial heat dissipation into the electrodes and the substrate, resulting in much cooler temperatures at the top and bottom surfaces. The simulated surface and $MoTe_2$ plug ΔT for different power inputs is displayed in Figure 3d. At $P = 2.5$ mW, the peak ΔT_S ranges from ~33 K to 39 K (corresponding to the SThM measurements), while the estimated peak ΔT_{plug} ranges from ~200 K to 235 K for the different plug diameters. ΔT_{plug} has a larger range because it is more sensitive to plug diameter than ΔT_S. Heat dissipation in the TE also limits our ability to accurately extract ΔT_{plug}, which could be better estimated by reducing the TE thickness in future work. (The thicknesses of the $MoTe_2$ and top SiO_2 layers should also be reduced, due to required step coverage.)

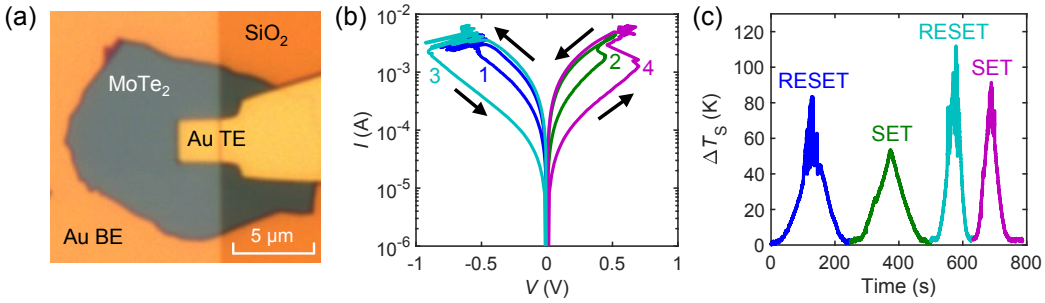

Figure 4. (a) Optical image of Device 3 with $t_{MoTe2} \sim 27$ nm and TE area of 2.5×2.6 μm^2. (b) *I-V* measurements of Device 3 showing 2 switching cycles (with a series resistance of 220 Ω). The number next to each curve corresponds to the order of the measurements. (c) ΔT_S from SThM measurements as a function of time, taken simultaneously with the *I-V* measurements in (b) of the same color. ΔT_S was calculated from ΔV_{SThM} using a calibration factor of 6.5 mV/K.

In addition to steady-state measurements, we also sweep the voltage while holding the SThM probe stationary and in contact with the device surface directly above the conductive plug. This allows us to measure ΔT_S while switching the device between the LRS and HRS. Figure 4a shows an optical image of the device (Device 3) with $t_{MoTe2} \sim 27$ nm and TE area of 2.5×2.6 μm^2. The *I-V* measurements during bipolar switching (using an external series resistance of 220 Ω) and the corresponding ΔT_S from SThM are displayed in Figure 4b,c. The curves in Figure 4b are labeled with "SET" or "RESET," corresponding to a transition to the LRS or HRS, respectively. ΔT_S reaches between 50 and 115 K when the device switches between the two states. Assuming d_{plug} between 250 and 400 nm, we use our simulations to estimate the maximum T_{plug} during the first

RESET and SET measurements to be ~650-750 K and ~530-630 K, respectively. During the second RESET and SET measurements T_{plug} is estimated to be ~700-850 K and 650-800 K, respectively. We note that SThM measurements cannot capture fast temperature transients (the thermal time constant of Pd-based probes is ~300 μs[23] and the sampling time of our SThM system is ~3 ms), so the plug and surface may reach even higher temperatures (and possibly the semiconducting-to-metallic transition temperature[29-31] for $MoTe_2$, ~920-1170 K) during bipolar switching.

To determine the effect of temperature on forming voltage, we also take temperature-dependent electrical measurements of a $MoTe_2$ device with Au electrodes (Device 4, t_{MoTe2} ~ 16 nm and TE area of 0.45 × 0.9 μm^2) using a fixed voltage range of 0 to 2 V and an external series resistance of 1 kΩ. At ambient temperatures of 300 K and 400 K, the device remains in the unformed state following forward-backward *I-V* sweeps. After increasing the temperature to 500 K, we observed device forming at ~1.3 V (see Supporting Information Figure S4). These measurements, in addition to the SThM measurements above, reveal that the forming mechanism has a thermally-activated component.

Next, we perform transmission electron microscopy (TEM) and energy dispersive spectroscopy (EDS) of Device 2 after switching. The device was cross-sectioned at the location of the conductive plug, which was determined by SThM, as shown in Supporting Information Figure S5. Figure 5a shows the TEM image of Device 2 across its active region, which was switched to the HRS before TEM imaging. Figure 5b-d shows EDS elemental intensity maps of Au, Mo, and Te, respectively. These maps reveal Mo and Te vacancies near the edge of the Au TE and Au within the $MoTe_2$ layer, suggesting that Au has migrated from one electrode to the other, displacing Mo and Te atoms. This migration likely results in the bump seen in the AFM image of Figure 2b.

We also see some evidence of O displacing Mo and Te atoms (Supporting Information Figure S6), which could be due to partial oxidation during fabrication. However, we do not expect O migration to be the primary cause of switching due to the low resistances measured in our devices, unlike in metal-oxide RRAM.[24] Switching in metal-oxide RRAM is often attributed to oxygen vacancies that form a conductive filament, which effectively reduces the device resistance.[32] We do not expect oxygen migration to reduce the resistance of our devices, because MoO_x is more resistive than $MoTe_2$.[33]

STHM and TEM images of a different device (Device 5), initially in the LRS before TEM imaging, are shown in Figures S7 and S8, respectively. Mo and Te vacancies in the $MoTe_2$ film and Au diffusion between electrodes are similarly observed in these images. The Au migration, like metal ion migration in conductive bridge random access memory (CBRAM),[34-35] might explain the very low resistances measured (as low as ~40 Ω in some cases) when the devices are switched to the LRS (see Supporting Information Figure S2). During the RESET measurement, the Au bridge between electrodes likely breaks, causing an increase in resistance.

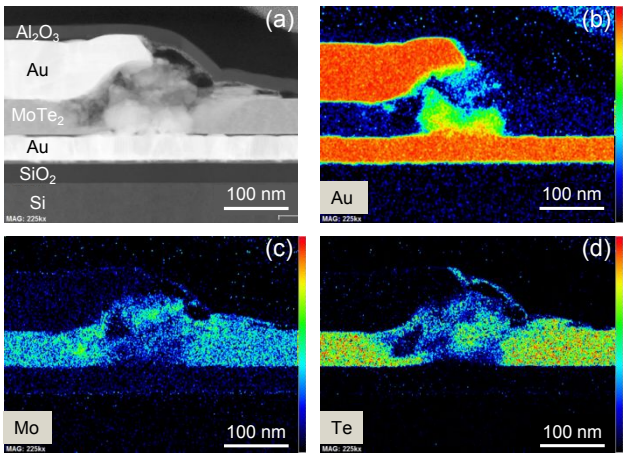

Figure 5. (a) High-angle annular dark-field (HAADF) transmission electron microscopy (TEM) cross-section of Device 2, which was switched to the high resistance state before imaging. The image shows the different layers of the device, including the $MoTe_2$ between the two Au electrodes, the underlying SiO_2/Si, and the Al_2O_3 capping layer. The layers above the Al_2O_3 are Pt and carbon coating layers to protect the samples during TEM preparation. Energy dispersive spectroscopy (EDS) elemental intensity maps showing (b) Au, (c) Mo, and (d) Te atoms. The color bars display the relative concentration of atoms, with red corresponding to the highest and black corresponding to the lowest.

We note that Au migration has been observed in other thin film devices, including memory devices, from thermal stress during operation.[36-37] We estimate current densities over 10^5 A/cm^2 in the Au electrodes during the forming step and even higher during bipolar switching, which are sufficiently high to cause Au migration.[38-39] The Au migration can also occur at defects in the Au or in the $MoTe_2$,[12,40] where local current densities are larger. Though metal ion diffusion from the electrodes has often been reported in other types of devices and is of concern with regard to reliability and endurance in memory, this phenomenon has only recently been reported in TMD-

based resistive memory devices.[11-12] We use Au electrodes in this study because it has often been used as a good contact metal to TMD semiconductors.[41-42] In addition, we find that $MoTe_2$ has good adhesion to Au during the transfer process due to the affinity of Au to chalcogen atoms.[43-44] (We observe that the $MoTe_2$ delaminates from other metals such as Pt or TiN during fabrication.)

To test other conductive (but non-metallic) electrodes, we also fabricate similar devices with graphite, which is an ultra-flat semimetal, as the top and bottom electrodes. Supporting Information Figure S9a,b shows a schematic and optical image of such a device (Device 6) with t_{MoTe2} ~ 29 nm, graphene bottom electrode thickness $t_{Gr,BE}$ ~ 14 nm, graphene top electrode thickness $t_{Gr,TE}$ ~ 5 nm, and TE area of ~40 μm^2. *I-V* measurements shown in Supporting Information Figure S9c reveal that at V = 0.1 V, the device has a resistance of ~15 MΩ, and at ~3.2 V it transitions to the LRS with ~1.6 kΩ. A series resistor with R = 1 kΩ was used for these measurements. We were unable to RESET the device back to the HRS using either voltage polarity, possibly due to the additional series resistance of the graphite. The same behavior (stuck in LRS after forming) was reproduced on another device with graphite electrodes.

Thus, the different behavior between the devices with Au and graphite electrodes suggests, first, that initial forming of the $MoTe_2$ is not triggered by metal ion migration from the electrodes and, second, that further bipolar switching only in devices with Au electrodes is caused by conductive metal bridging, as seen in the TEMs discussed earlier. This mechanism is different from that of ref. [10], which suggested bipolar switching due to localized phase change induced by an electric field. However, different initial forming and switching mechanisms among different studies cannot be ruled out because there may be differences in sample quality (e.g. Te vacancies[45]) and processing (e.g. oxidation[46]). For example, a thin oxide layer on the $MoTe_2$ surface could rupture in a filamentary manner, leading to highly localized electric fields, current flow, and subsequently a phase change in the pristine $MoTe_2$ beneath. Such an effect was recently observed in $Ge_2Sb_2Te_5$-based phase change memory with a thin oxidized electrode, which switched at lower current than control devices due to oxide filament formation.[6] (We do not expect such an oxide and such highly localized electric fields in our devices due to careful processing in a N_2 glove box.) Other potential causes of forming could be defect (i.e. vacancy) generation or Te migration.[46-47] Immediately after forming, the current (and power) density is quite high, leading to significant Joule heating and causing Au migration, which is a thermally-activated process. Subsequent switching between the LRS and HRS is likely caused by the breaking and forming of

these Au conductive plugs between the electrodes, as suggested by our cross-sectional TEMs.

In conclusion, we observed localized heating during operation of $MoTe_2$-based memory devices and measured their surface temperature using SThM for the first time. Together with temperature-dependent electrical data and TEM images, these SThM measurements reveal that both the forming and switching mechanisms have thermally-activated components. While the initial forming process may be caused by defect generation or Te migration, subsequent bipolar switching appears due to Au migration from the electrodes. Nevertheless, simulations suggest that high internal temperatures during switching could also cause localized phase change in the $MoTe_2$. Beyond this study, the SThM technique can also be applied to other traditional or emerging resistive memory devices to determine the location and temperature of switching regions, which is essential for understanding and optimizing such data storage.

ASSOCIATED CONTENT

Supporting Information.

The following file is available free of charge on the ACS Publications website. The 2D material transfer process; measurement and model of devices before forming; forming current and voltage data for all devices; scanning thermal microscopy (SThM) measurement details; 3D finite element modeling; temperature-dependent *I-V* measurements; SThM images, TEM cross-sections, and EDS elemental maps; $MoTe_2$ device with graphite electrodes.

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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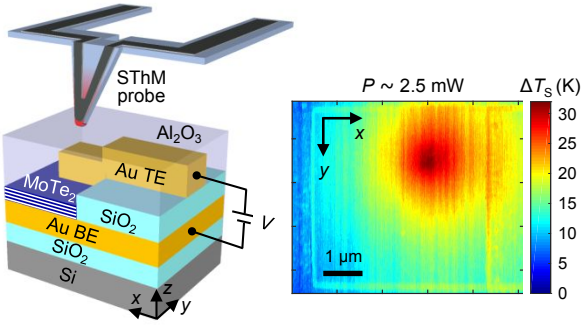

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