FABRICATION OF LARGE-VOLUME RECTANGULAR CHANNELS USING TRENCH-SIDEWALL TECHNOLOGY AND A SOI SUBSTRATE

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ABSTRACT

In this paper we propose an extension of surface channel technology (SCT) which is based on trench side wall technologies from the micro-electronics industry and silicon-on-insulator (SOI) wafers. In this CMOS compatible trench-assisted surface channel technology (TASCT) process, refilled trenches define the outline of the microfluidic channels and chambers in the lateral plane and serve as etch stops during channel etching. This ensures well-defined channel shapes and the possibility to incorporate in-channel pillar structures in order to fabricate large-volume rectangular microfluidic channels, which can be integrated with smaller cross-sectional channels. When a highly-doped device layer is chosen, the possibility arises to add side wall heater structures next to the microfluidic channels as well.

KEYWORDS

Trench-assisted surface channel technology, trench side wall technology, large-volume microfluidics, trench refilling

INTRODUCTION

Conventional SCT[1–3] was initially designed to create a micro mass-flow controller based on the Coriolis effect[4]. The fabricated channels are semi-circular since the channel etch is only limited by the etch mask on top, and the channel side wall only consists of low-stress silicon-rich silicon nitride (SiRN). With the proposed TASCT process, the channels will be rectangular because of refilled trenches, which serve as an etch stop during the isotropic channel etch. This will give a higher accuracy on the control of the final channel shape when compared to conventional SCT. Schematics of both a SCT channel and a TASCT channel are shown in figure 1a and figure 1b, respectively.

These trenches allow in-channel pillar fabrication, which opens the way to fabricate large-volume rectangular surface channels in the lateral dimension of a single silicon-on-insulator (SOI) substrate. This

(a) *(b)*

Figure 1: Schematics of a SCT channel (a) and a TASCT channel (b). Please note that the figure is not on scale. Colours are indicating Silicon, First layer of low-stress SiRN, Second layer of low-stress SiRN, Burried oxide layer.

makes TASCT a very controlled technique to make interconnected surface channels of different shapes. When this approach is combined with the suspended channel technology from the SCT and a highly-doped SOI substrate, it is also possible to fabricate free-hanging, mechanical stable and thermally isolated channels with side wall heating elements, which can serve as large rectangular combustion reaction chambers usable for microscale combustion experiments, as is introduced in the paper submitted to this same conference by Y. Zhao *et al.*, entitled *Design principles and fabrication method for a miniaturized fuel gas combustion reactor*. The described TASCT process will be used in the near-future to realize an improved design on the recently developed Wobbe Index meter[5]. This paper describes the proposed steps of the TASCT process.

TASCT FABRICATION PROCESS

The TASCT process that is proposed to be used as way to fabricate rectangular large-volume microfluidic channels and chambers can be divided into five main parts. The first step is the creation of etch stops, and therewith the channel outline, by etching of high-aspect ratio trenches in a SOI substrate with a notching-free Bosch process, followed by subsequent refilling of those etched trenches with low-stress (SiRN). Then, the microfluidic channels and reaction chambers will be etched by first etching slit patterns into the SiRN layer in between the trenches. Through these slits, the

underlying Si will be etched away, where the SiRN inside the trenches serve as an etch stop. The next step is the formation of the inner wall of the channels and chambers, which also includes the closure of the slits. This will be done via another deposition run of low-stress SiRN. Then, electrical contact pads will be made onto the Si and a metal will be deposited. This metal will serve as electrical circuits, connecting the Si side wall heaters to the outside world, as heater structures, and as temperature sensors. Then, as final step, the surrounding Si will be etched away with a two-step etch process.

The proposed TASCT process combines notching-free high aspect ratio trench-etching in a highly-doped SOI substrate with strategies from the micro-electronics industry, i.e. trench side wall technology[6], with trench refilling technology[7] and SCT[1].

Each part of the TASCT process will be discussed separately. Each subsection will be accompanied by cross-sectional schematics (not on scale) of a channel structure with a pillar inside. The full colour legend is shown in figure 2.

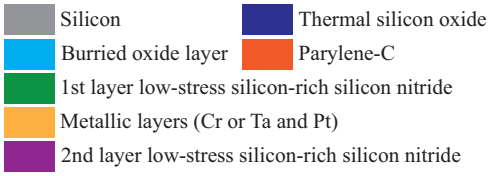

Figure 2: Legend of the used colours in the cross-sectional images in this paper.

Etch stop and channel outline

The fabrication of the etch stops and the channel outline is the first step in the realisation of TASCT channels, and is visualized in figure 3. A highly-doped SOI substrate with a device layer of 50 µm, a BOX layer of 200 nm, and a handle layer of 450 µm will be oxidized via wet thermal oxidation at 1150 °C in a Tempress Systems furnace. This SiO_2 layer will serve as a hard mask during the trench etching. For that, it will be patterned with 3 µm wide trenches via conventional I-line photo-lithography and SiO_2 reactive ion etching (RIE) in a PlasmaTherm-790 plasma etcher. The high aspect ratio trenches of 3 µm wide will be etched completely down to the BOX layer with a notching-free Bosch process with a low frequency (LF) end-step using an Oxford Instruments PlasmaPro 100 Estrelas deep reactive ion etching (DRIE) plasma system.

Then, a layer of 2 µm parylene-C will be deposited conformally via chemical vapour deposition (CVD) in a PDS 2010 system of Specialty Coating Systems. This layer will serve as BOX layer protection during subsequent hard mask stripping[10]. The surface parylene-C will be etched back using an O_2 plasma in a barrel etcher[8]. Here, we will take advantage of the fact that etching on the surface has a higher rate than etching inside the trenches, i.e. the etch rate is limited by the aspect ratio of the trench. Subsequently, the SiO_2 hard mask will be stripped in buffered HF (7:1 NH_4F:HF) and the remaining parylene-C will be stripped away in a piranha solution (3:1 H_2SO_4:H_2O_2) at 90 °C.

The trenches will be refilled with low-stress (50 MPa) SiRN via low pressure chemical vapour deposition (LPCVD) in a Tempress Systems furnace with a SiH_2Cl_2/NH_3/N_2 flow[7]. These refilled trenches will act as etch stops during the channel etch later on.

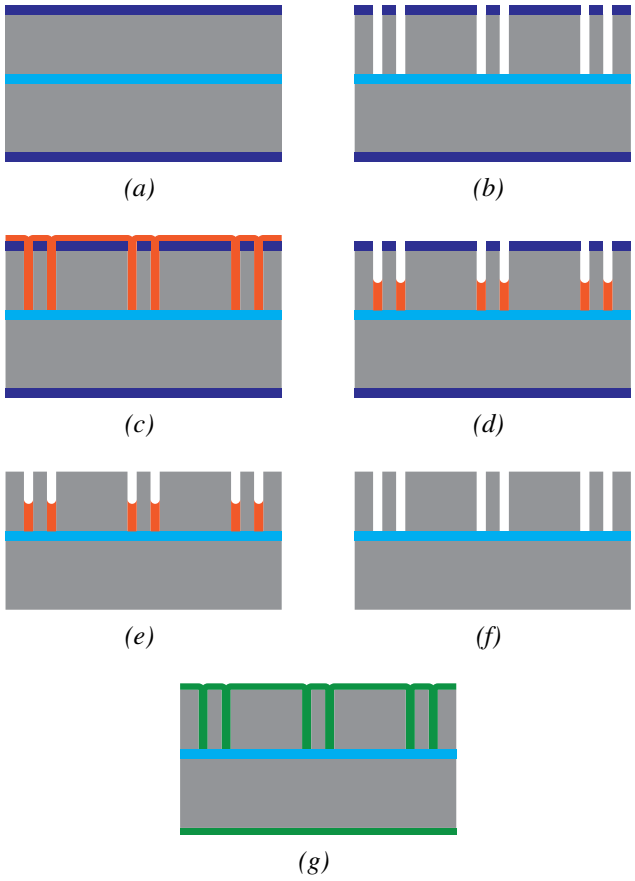

Figure 3: Schematics of the etch stop and channel outline formation in the TASCT process, with the steps (a) thermal oxidation of a SOI wafer, (b) RIE of SiO_2 and notching-free DRIE of Si, (c) CVD of parylene-C, (d) etching of parylene-C in an O_2 plasma, (e) stripping of the SiO_2 hard mask in buffered HF, (f) stripping of the remaining parylene-C in piranha, (g) trench refill with LPCVD of low-stress SiRN.

Channel and chamber etch

Schematics of the microfluidic channel and chamber etch are shown in figure 4. First, a layer of Cr will be sputtered with an home-build sputter machine on top of the low-stress SiRN layer. A slit pattern will be patterned in between two adjacent trenches, which are forming the channel side walls, via I-line photo-lithography and etched with RIE in an Alcatel Adixen AMS100 RIE etcher. These patterned Cr and SiRN layers will be used as etch mask during the isotropic channel etch, like in the conventional SCT process[1,2]. The Cr will act as an etch mask during SiRN and Si etch, preventing the increase of the slit width in the SiRN.

The Si inside the microfluidic channels and chamber structures will be etched away through the slits with a SF_6 plasma in the Oxford Instruments PlasmaPro 100 Estrelas.

After the channel and chamber etch, the Cr layer will be stripped away in wet Cr etchant.

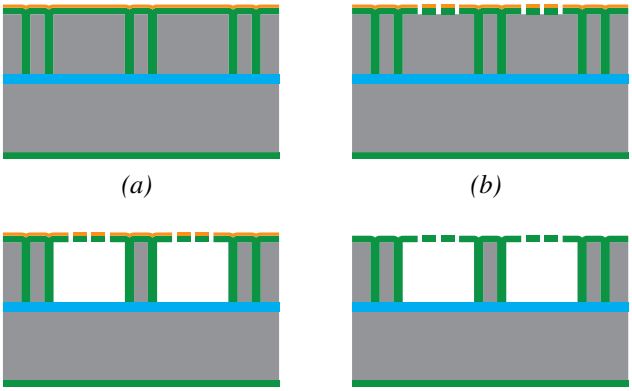

Figure 4: Schematics of the channel and chamber etch, with the steps (a) Sputtering of a Cr layer, (b) RIE of Cr and SiRN in order to create the slit mask, (c) Isotropic channel and chamber etch with SF_6, (d) Stripping of the Cr layer.

Channel wall formation and closure

After etching away the Si, the inner channel and chamber walls will be formed via another LPCVD run of low-stress SiRN, which will be conformally grown to a thickness slightly more than half the slit width (total layer thickness: $\pm$1.5 times the slit width). This way, a full closure of all the slits will be ensured, thus completely closing the channel. A schematic of the channel closure is shown in figure 5. The use of LPCVD to close the channels is the same as in the conventional SCT process[1–3].

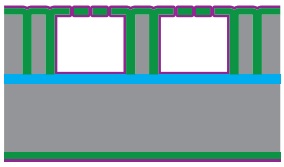

Figure 5: Channel and chamber wall formation via LPCVD of low-stress SiRN, which also ensures full closure of the slits.

Electrical connects and metal deposition

In order to create electrical contacts to the Si side wall heater structures, the two SiRN layers will be patterned via I-line photo-lithography and RIE in the Alcatel Adixen AMS100 plasma etcher. Then, the metallic layers (Pt and an adhesion layer), which serve as both the interfacing between the Si side wall heaters and the macro world, and resistive heaters and temperature sensors will be sputtered.

The adhesion between Pt and the substrate can only withstand elevated temperatures of above 500 °C when a proper adhesion layer is used. From previous work, for example the work by Tiggelaar *et al.*, it is learned that Ti will not survive elevated temperatures and causes delamination, hole formation and agglomeration of the Pt[9]. Therefore, an adhesion layer of Ta will be used, which is known to withstand higher temperatures[9]. First, a thin 5 nm Ta layer will be sputtered in a home-build sputter device, directly followed by a 400 nm Pt layer. The metallic layers will be patterned via ion beam etching in an Oxford Instruments Ionfab 300plus.

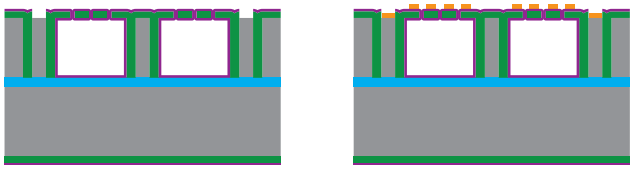

Figure 6: Electrical interfacing, with (a) Opening up electrical pads on the Si side wall heater structures, (b) Sputtering of metallic electrical connects, resistive heater and temperature sensing structures.

Channel release

As final step, the channels and chambers will be released in order to create a suspended system, which is thermally isolated from the bulk Si. This release will be done in two steps. First, a directional etch will be performed with the Bosch process, after which an isotropic etch with SF_6 plasma will be used to remove the remaining Si in all directions, creating cavities of

sufficient size. Both steps will be performed in the Oxford Instruments PlasmaPro 100 Estrelas. The hole etched with the Bosch process will reduce the etch time of the isotropic etch, and therefore limits the exposure time of SiRN to SF_6. The final channel is schematically shown in figure 7.

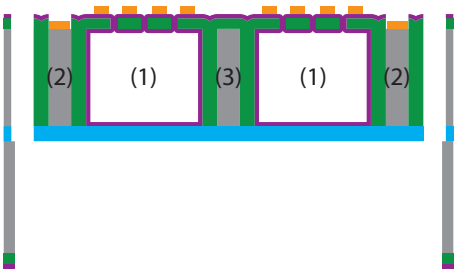

Figure 7: Channel release etch via a combined directional process (Bosch) and isotropic process (SF_6 plasma). In the image, (1) is indicating the channel, (2) is indicating the Si side wall heating structures, and (3) indicates an in-channel pillar.

CONCLUSION

The proposed new trench-assisted surface channel technology fabrication technique combines different well-established micromachining techniques from different industries, like microelectronics and microfluidics, to form a new and elegant approach to surface channel formation. The combination of trench and trench-related technologies with the previously described surface channel technology[1–3] makes that TASCT has potentially more design freedom than SCT and it has the potential to create well-defined large volume channels with a better accuracy than with the SCT technology.

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