METHOD AND CIRCUITRY FOR CMOS TRANSDUCER LINEARIZATION

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ABSTRACT
Third order distortion is reduced in a CMOS transconductor circuit that includes a first N-channel transistor and a first P-channel transistor, gates of the first N-channel transistor and the first P-channel transistor being coupled to receive an input signal. Drains of the first N-channel transistor and first P-channel transistor are coupled to an output conductor. A first degeneration resistor is coupled between a source of the first P-channel transistor and a first supply voltage and a second degeneration resistor is coupled between a source of the first N-channel transistor and a second supply voltage. A first low impedance bypass circuit is coupled between the sources of the first P-channel transistor and the first N-channel transistor. A low impedance bypass circuit re-circulates second order distortion current that is induced by second-order distortion in drain currents of the first P-channel transistor and the first N-channel transistor, through the first N-channel transistor and first P-channel transistor.