A 30fJ/comparison Dynamic Bias comparator

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Abstract— **A dynamic bias pre-amplifier based latch type comparator is designed in a 65nm CMOS process. Its performance is compared with the double-tail latch-type comparator fabricated on the same chip in terms of energy consumption, input referred noise and speed. Measurements demonstrate that the proposed dynamic bias pre-amplifier based comparator consumes 2.8 times less energy per comparator operation with a modest reduction in input referred noise and 40% increase in CLK-Q delay for small differential input voltages.**

Keywords— *Dynamic bias; charge steering; StrongARM latch; double-tail latch-type comparator; Noise; SAR; Offset*

I. Introduction and prior art

StrongARM latch and its variants have been widely used as comparators owing to their strong positive feedback required for fast decisions, zero static power consumption, and full swing outputs [8,9]. However as highlighted in [1,9], they suffer from large required voltage headroom which makes it challenging to design them in low voltage deep-sub-micron technologies. In addition, due to poor isolation between the regeneration latch and the differential input stage, the strong-arm latch suffers from large kickback noise at its inputs, a large common mode dependent offset [9] which is a cause of concern specially for data converters. The double-tail latch-type architecture presented in [1] mitigated these problems by separating the pre-amplification from the latching operation, while simultaneously lowering voltage headroom requirement, allowing operation at lower supply voltages.

The double-tail latch-type architecture [1] has been modified over the years for application in energy efficient ADCs [2,4]. For the application of comparators in data converters, input referred noise must be sufficiently small to make reliable comparisons at any input voltage levels down to sub-LSB sized levels.

In the double-tail latch-type comparator targeted for SAR ADCs [2], as shown in Fig. 1(a), the pre-amplifier is hard-switched into strong inversion. This yields high-speed operation but also (for any input voltage) yields relatively large input referred noise levels that are filtered thanks to the (parasitic) capacitances C_p at the pre-amplifier's output nodes (see Fig 1(a)). The pre-amplifier constitutes 80% of the energy consumption of these comparators [1,2,4]. The minimum achievable energy-per-comparison for a given SNR is thus determined by the value of these C_p's.
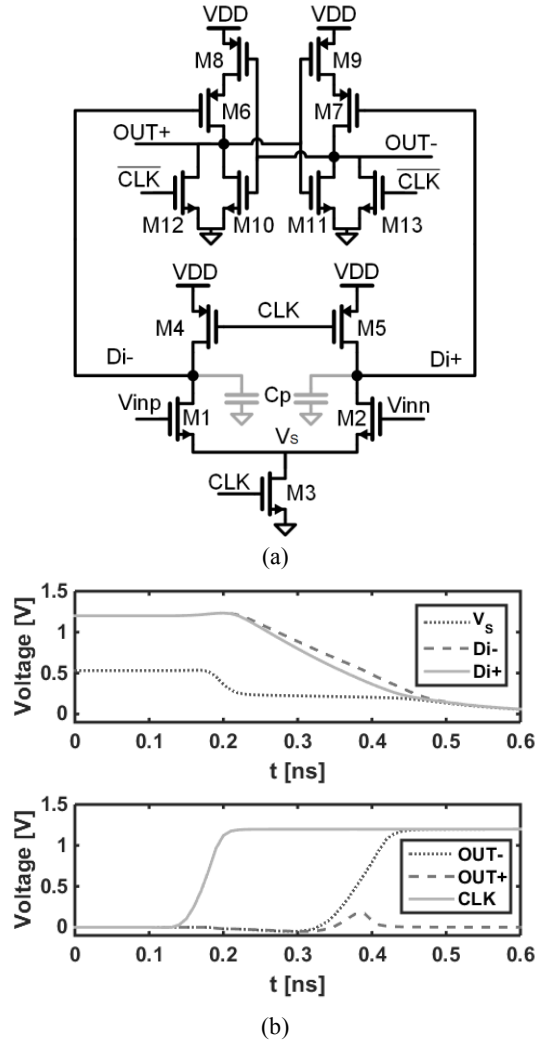

(a)

(b)

Fig. 1 (a) Circuit and (b) timing waveform of a double-tail latch-type comparator [2] for 15mV differential input at common mode voltage, V_{CM} equal to 0.6V.

For applications like SAR ADCs with moderate to high resolution targeted for ultra-low power wireless sensor nodes, 40-60% of the total ADC energy consumption is contributed by the comparator and the rest by DAC switching energy and the delay line controller [2,3,4]. In addition, the comparator's energy consumption per bit comparison does not scale with technology and supply voltage thereby presenting a bottleneck in lowering the energy consumption per conversion for data converters.

Techniques like Data Dependent Noise Reduction (DDNR) [3] and reduced supply bi-directional comparator operation [4] have been used to improve the SNR and energy per comparison respectively of the double-tail latch-type comparator in SAR ADCs. For the bi-directional comparator [4], the energy required by the pre-amplifier per comparison can be reduced to $C_p \cdot VDD^2$ as compared to $2 \cdot C_p \cdot VDD^2$ for the comparator in [2]. However as reported in [4], due to the logic overhead required for reset/latch enable signals and the OR gate to switch from PMOS pair to NMOS pair, the resultant improvement in energy is limited to 33% for the same SNR as in [2]. Another known SNR enhancement technique in SAR ADCs is to employ majority voting for the decisions near LSB resolution [3]. Majority voting has advantages over analog scaling [3,7] as the former needs to be employed only for near LSB decisions and as shown in [3] can result in 40% lower input referred noise voltage. However, the overhead in energy consumption of the LSB detection mechanism for performing majority voting as reported in [3], still leaves a scope for reducing the energy consumption per bit comparison for a given SNR.

In the case of double-tail latch-type comparator [1,3,4], a fixed charge $C_p \cdot VDD$ is required (or lost) at each of Di+/Di- node per comparator operation, thereby presenting a bottleneck for energy optimization for a given SNR. This paper presents a dynamic biased pre-amplifier based latch-type comparator that utilizes the charge lost (transferred) from Di+/Di- nodes to dynamically bias the pre-amplifier during the comparator operation. By controlling the amount of charge transfer (or loss) from Di+/Di- nodes, the energy per comparison is lowered from $2 \cdot C_p \cdot VDD^2$ for a given SNR.

II. Energy or Dynamic Bias

The concept of energy bias or dynamic bias was originally proposed by [5] and has been recently used to make low energy charge steering Current Mode Logic [6]. In this paper the concept of dynamic bias is extended to double tail latch-type comparator to reduce the energy per bit comparison for a given SNR. The dynamic bias comparator is shown in Fig. 2 along with its behavior. In the reset phase, transistors M4 & M5 pre-charge the drain nodes Di+ & Di- to VDD, M12 & M13 reset the latch and the tail capacitor C_{tail} is discharged to ground through M3b. During the comparison phase, M3a turns ON, M3b turns OFF and thus capacitances, C_p's on the drain nodes Di+ & Di- start discharging, thereby charging the tail capacitor C_{tail} and hence increasing the voltage V_{cap} which dynamically bias the input differential pair.

As the voltage V_{cap} on C_{tail} increases, the gate-source voltage of M1/M2 reduces until the source voltage reaches the first quenching point, $V_s = min(Vinp-V_{th1}, Vinn-V_{th2})$. At this point, one of the input transistors M1/M2 turns off and the drain voltage at that transistor freezes. The other transistor continues to discharge its corresponding C_p until the second quenching point, $V_s = max(Vinp-V_{TH1}, Vinn-V_{TH2})$ is reached. This is in contrast with a double-tail latch-type comparator [2], where both the drain nodes are completely discharged to
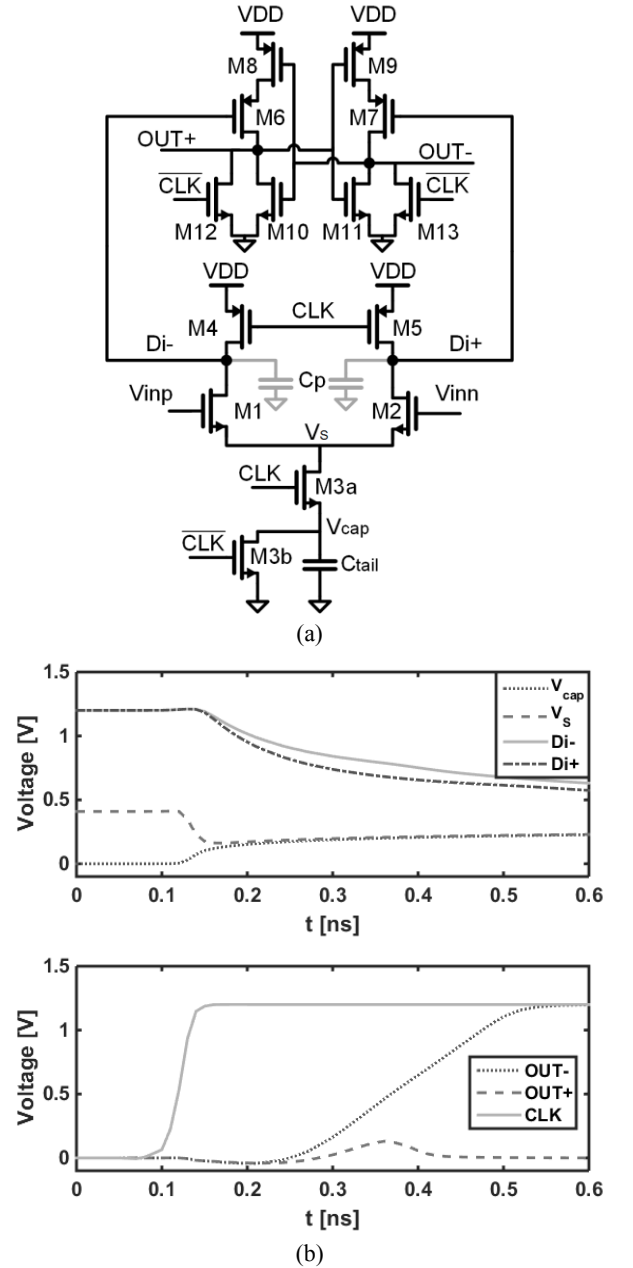

(a)

(b)

Fig. 2. (a) Circuit and (b) Timing waveforms of the proposed Dynamic Bias Comparator for 15mV differential input at $V_{CM} = 0.6V$.

ground at the end of comparison phase. For the dynamic bias comparator, at the end of comparison phase, the voltage V_{D1}/V_{D2} at Di+/Di- nodes depends on the amount of charge transferred to C_{tail} during the comparison time. The energy dissipated by the dynamic bias pre-amplifier is $[2 \cdot C_p \cdot VDD^2 - VDD \cdot C_p \cdot (V_{D1}+V_{D2})]$ which is lower than $2 \cdot C_p \cdot VDD^2$ for a double-tail latch-type comparator.

With dynamic bias, the differential pair starts in the strong inversion region with a large momentary tail current which then continuously decreases with increasing V_{cap} during the comparison phase. Near the first quenching point, at least one of the input transistors M1/M2 enters into the weak inversion

region, which results in a higher voltage gain [5] and lower input referred noise at the cost of a lower GBW compared to the double-tail latch-type comparator, where the input differential pair continuously operates in strong inversion. Along with a higher voltage gain, the continuously decreasing gate-source overdrive voltage V_{GT} of M1 & M2 in weak inversion operation also decreases the effective noise bandwidth, proportional to $I_{M1,M2}/C_p$ [2,5] and hence, improves the noise performance for dynamic bias. In a typical 1.2V supply 10-bit SAR ADC application wherein the differential input voltage to a comparator ranges from near LSB resolution (1mV) to full scale differential (1.2V), the dynamic bias comparator provides an energy efficient charge-biased dynamic pre-amplification mechanism. It operates in the fast strong inversion region of operation for large input differential voltages and in the high gain, low input referred noise weak inversion operation region for near LSB input differential voltages. However, due to a lower GBW in weak inversion operation a higher CLK-Q delay is also observed in the case of dynamic bias for small differential input voltages as compared to the double-tail latch-type comparator operation [2].

For comparing the performances of the two type comparators as depicted in Fig.1 and Fig.2, these were fabricated on the same die in a standard 65nm CMOS process. The size of the input differential pair M1 & M2 were kept the same for both designs to have similar input referred offset. Also the latch stage is kept identical for both designs to ensure similar regeneration times. The small signal gain is given as $2 \cdot C_{tail}/C_p$ [5,6] for a dynamic bias pre-amplifier and C_{tail} was chosen as 35fF for a C_p of approximately 12fF (from extraction) to get approximately the same input referred noise for both designs.

III.   Measurements and Results

Fig. 3 shows the input referred noise for both the comparators obtained by measuring the average number of positive decisions versus ΔV_{in}. Fitting the measurements to a Gaussian cumulative distribution function (CDF) gives an RMS noise voltage of 0.4mV for the double-tail latch-type and 0.45mV for the dynamic bias comparator at their inputs. It can be seen that the standard deviation of the input referred noise is 10% less for the dynamic bias comparator.

Fig. 4 shows the input referred noise voltage for the two types of comparators as a function of V_{CM} derived from the CDF. It can be seen that the input referred noise voltage increases with increasing V_{CM}. This is because with increase in V_{CM} the transistors M1 & M2 spend a comparatively longer time in strong inversion during the comparison phase before they enter into weak inversion. This results in a shorter integration time before the second stage latches, thereby resulting in lower gain and higher noise bandwidth leading to a higher input referred noise voltage [2]. The average energy consumption per comparison for the dynamically bias comparator is approximately 30fJ/comparison whereas it is 84fJ/comparison for the double-tail latch- type comparator
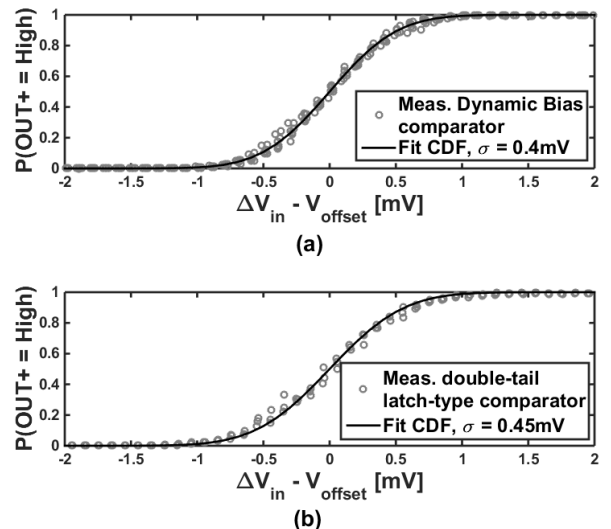

(a)

(b)

Fig. 3. Measured cumulative probability density distribution and fit to Gaussian distribution for (a) the Dynamic Bias Comparator and (b) the Double-tail latch-type comparator; $V_{CM} = 0.6V$.
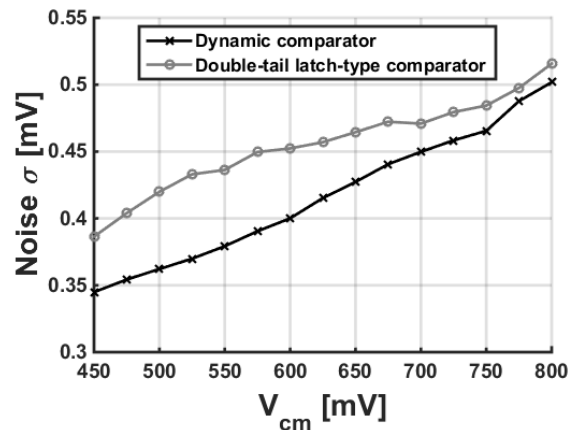

Fig. 4. Input referred noise measured as a function of V_{CM} for the Double-tail latch-type comparator and the Dynamic Bias Comparator.

both measured on the same chip. Fig. 5 shows the energy consumption versus input differential voltage, highlighting the reduction in overall energy consumption. It can be seen that the dynamic bias comparator consumes approximately 2.8 times less energy than the double-tail latch-type comparator throughout the range of input differential voltages. The 1-sigma offset measured on 8 samples for dynamic bias comparator varies approximately from 5.4mV to 6.2mV at V_{CM} ranging from 0.5V to 0.8V. The low common mode-independent offset is crucial for applications with wide common-mode range such as data converters. This is consistent with the measured 1-sigma offset range of 6.5mV to 7mV for the double-tail latch-type comparator for the same 8 samples for the same V_{CM} range. Typically, for applications like SAR ADCs, some input referred offset is acceptable as it just induces a static shift of output codes versus input voltage. Fig. 6 shows the measured relative CLK-Q delay for the dynamic bias comparator and the double-tail latch-type

comparator versus ΔV_{in} (the absolute delay is not measurable due to additional delay from on-chip output buffers). The CLK-Q delay indicates the time between the CLK edge and the instant |(OUT+)-(OUT-)| crosses ½ VDD. It can be seen that for small differential input voltages, the dynamic bias comparator has approximately 40% larger CLK-Q delay. This is due to the fact that for smaller input differential voltages both the transistors M1/M2 spend more time in the weak inversion region before reaching the two quenching points. Also note that the positive feedback of the second stage latch results in logarithmic relation between the relative CLK-Q delay and ΔV_{in} which is quite similar for both the comparators: -75ps/decade for the double-tail latch-type comparator and -85ps/decade for the Dynamic bias comparator.
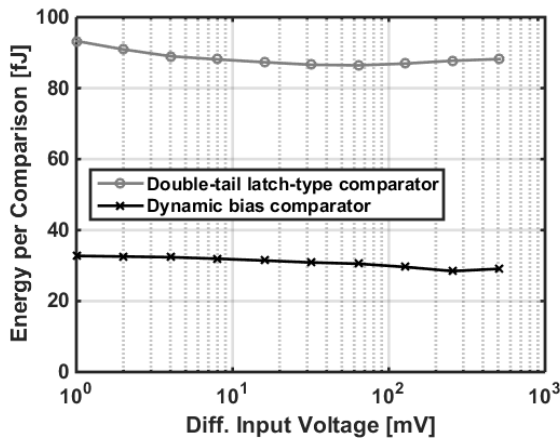

Fig. 5. Energy consumption of Dynamic Bias and Double-tail latch-type Comparator across differential input voltage range at V_{CM} = 0.7V for 1.2V supply and 25MHz clock.
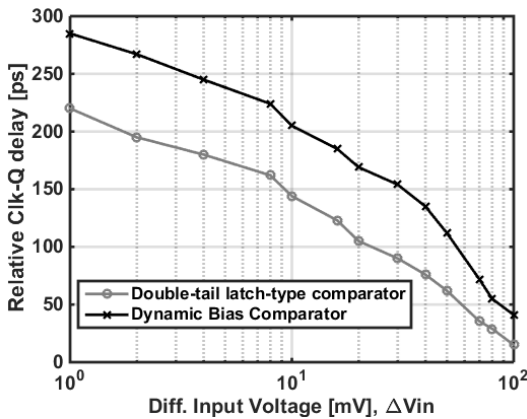

Fig. 6. Relative Clk-Q delay measured for the Double-tail latch-type based comparator [2] and the Dynamic bias comparator for 1.2V supply and 25MHz clock at V_{CM}=0.7V.

Fig. 7 shows a die micrograph for both the Dynamic Bias and double-tail latch-type comparators, with the inset showing the sizes. The Dynamic bias comparator occupies 20% more area than the double-tail latch-type comparator.
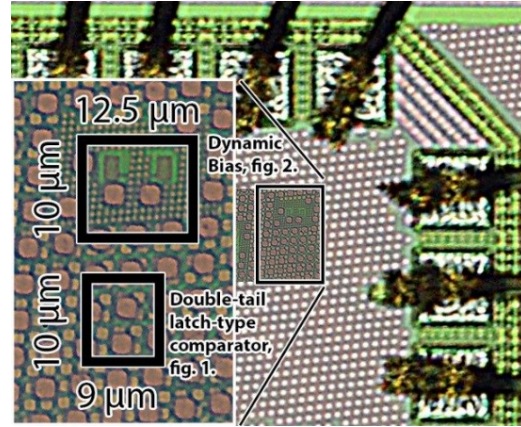

Fig. 7 . Die micrograph : The inset shows the zoomed in region for both the dynamic bias comparator and double-tail latch-type comparator. The sizes are 12.5μmx10μm for dynamic bias comparator and 10μmx9μm for the double-tail latch-type comparator.

IV.   Conclusion

In conclusion the dynamic bias comparator presented here achieves about 2.8 times lower energy per comparison as compared to the widely used double-tail latch-type comparator [2], dimensioned for the same input referred noise and speed. This is achieved by inherently only partially discharging the internal nodes in the pre-amplifier, and by automatically using longer integration times and weak inversion operation for small input signals. These properties make the dynamic bias comparator an interesting choice as a building block in many applications such as ultra-low power ADCs (especially SAR) in IoT, sense amplifier.

References

[1] D. Schinkel et. al, "A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time", ISSCC 2007.
[2] M. van Elzakker et.al, "A 10-bit Charge-Redistribution ADC Consuming 1.9μW at 1MS/s", JSSC 2010, pp. 1007-1015.
[3] P. Harpe, E. Cantatore, Arthur van Roermund, "A 2.2/2.7fJ/conversion-step 10/12b 40kS/s SAR ADC with Data-Driven Noise Reduction", ISSCC 2013.
[4] M. Liu et. al, "A 0.8V 10b 80kS/s SAR ADC with Duty-Cycled Reference Generation", ISSCC 2015.
[5] B. J. Hosticka, "Dynamic CMOS amplifiers", in JSSC 1980 vol. 15, no. 5, pp. 881-886.
[6] J.W. Jung, B. Razavi, "A 25-Gb/s 5-mW CDR/deserializer", JSSC 2013, pp. 684–69.
[7] D. Schinkel, "On-chip data communication : analysis, optimization and circuit design", PhD Thesis, Dept of EEMCS, University of Twente, Enschede, 2011.
[8] T. Kobayashi, K. Nogami, T. Shirotori, and Y. Fujimoto, "A current-mode latch sense amplifier and a static power saving input buffer for low-power architecture", VLSI Symposium, June 1992, pp. 28–29.
[9] B. Razavi, "The StrongARM Latch [A Circuit for All Seasons]", in *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12-17, Spring 2015.