1995 IEEE-EMBC and CMBEC
Theme 5: Neuromuscular Systems/Biomechanics

Control electronics for a neuro-electronic interface implemented in a Gate Array

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Abstract – **We present a Gate Array for implementing electronic circuitry to control multi-electrode arrays, which consist of 128 microelectrodes. The chip contains multiplexers, current sources and buffer amplifiers in CMOS technology.**

INTRODUCTION

For selective intraneural stimulation we intend to use a three-dimensional array of 128 electrodes [1,2]. A major step in the development of the device is the contacting technology. Because the electrode contacts at the backside measure only 55x55 μm and have a heart-to-heart spacing of 120 μm, standard technologies such as Ultrasonic Wire Bonding cannot be used. As a solution to this problem we developed a flip-chip technique to connect the 3D device to a CMOS chip (described in a separate abstract). Figure 1 shows a schematic overview of the resulting structure. At the center, the chip contains a 4x32 array of metal pads to which the multi electrode can be connected. In this paper we present the design of a suitable CMOS chip.

Because designing and realizing a full custom CMOS chip is a costly and time-consuming process, we used a gate array for implementation of the electronic circuitry. The gate array (GA2001) contains 1074 cells of 4 PMOS and 4 NMOS transistors each. The aluminum interconnect layer is designed specifically for the application, all other layers are already present. Designing an application chip is merely defining the necessary connections between transistors within the basic cells, and the connections between the cells.

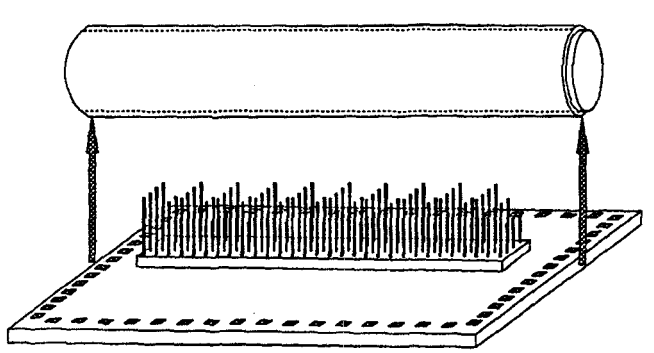

Figure 1: Schematic overview of a CMOS chip carrying a three-dimensional array of 128 microelectrodes, which can be inserted into a nerve

METHODS

The CMOS chip in our application should meet the following demands:

- provide multiplexing possibilities
- provide current sources for stimulation with biphasic current pulses
- provide buffer amplifiers for recording of neural signals
- minimize number of leads
- provide possibility of solder bumping
- be sufficiently small for implantation
- allow implementation in a Gate Array

The Gate Array is primarily designed to contain digital electronic circuitry. The main problems in the design therefore occur in the analog parts (current sources and amplifiers).

The current sources should be able to produce a biphasic current pulse, with either amplitude or duration adjustable. Pulse width modulation is easier to implement in the gate array, because (digital) switches can be used. The (constant) current amplitude should be several tens of microamperes, while the duration should range from 0 to approximately 100 μs, in steps of 1 μs.

The amplifiers should primarily buffer the measured neural signals. The output impedance should be lower than 1 kΩ. Amplification of the signals is of lesser concern. For neural action potentials the power spectrum ranges to at most 10 kHz, which should thus be the bandwidth of the amplifiers. Taking the bandwidth too high will increase the Total Harmonic Distortion and increase the output noise level. The noise level should be less than 1 μV rms over the full bandwidth.

The Gate Array measures 6x6 mm, and will need 15-20 connections to the outer world. For acute experiments this is acceptable, but for long-term implantations a smaller number of leads is desirable.

Because only a limited number of transistors is available, limitations are imposed on the design. The 128 electrodes are split into 8 sections of 16 electrodes each. Every section has its own control electronics. A layout of the design for one group is shown in figure 2.

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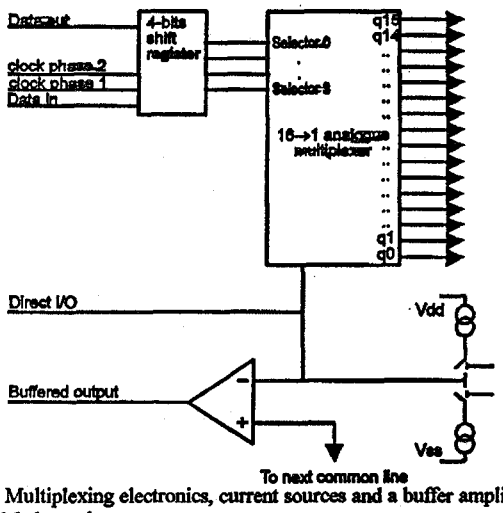

Figure 2: Multiplexing electronics, current sources and a buffer amplifier for a group of 16 electrodes

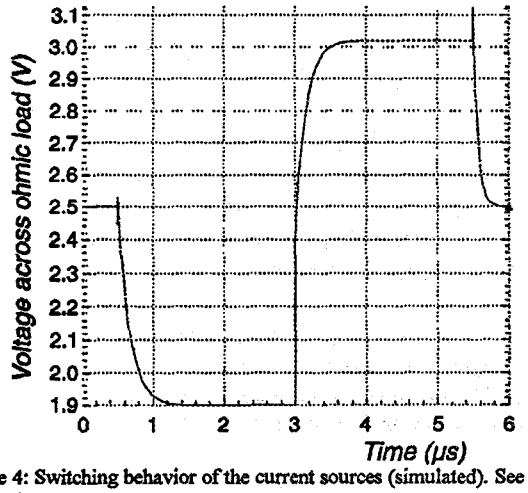

Figure 4: Switching behavior of the current sources (simulated). See text for a description

RESULTS

Because the Gate Array was designed primarily for digital purposes, implementing the multiplexers and switch control registers is straightforward. NANDS and INVERTORS were used to construct a 16 to 1-decoder, one for each of the 8 groups in the design. From testing, these proved to work up to clock frequencies of at least 20 MHz, which should be sufficient for our application. A control register for the switches of the current sources also works very well.

Less common is the use of analog elements in the Gate array, such as our amplifier and current source. The problems here arise not only from the arrangement in basic cells (with some transistors already connected), but also from lack of accurate model parameters for simulation of the analog circuits. Further complications arise from the limited supply voltage (0-5 V) and especially the long polysilicon connection lines that must frequently be used.

Figure 3 shows the design of the current sources in CMOS technology. First note that the electrodes are always halfway between Vdd (5 V) and Ground, because otherwise no biphasic stimulation pulses would be possible. These biphasic stimulation pulses are preferable because of the lower *reversible charge injection limit* [3] as compared to monophasic stimulation pulses.

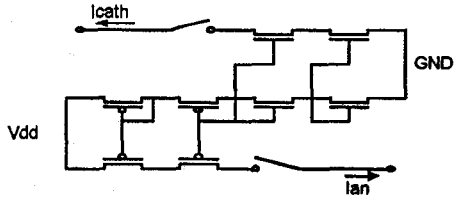

Figure 3: Current sources in CMOS technology. Note that the electrode potential is halfway between Vdd and Ground, in order to allow biphasic stimulation patterns. Icath: cathodic current; Ian: anodic current

In figure 4, the simulated switching behavior of the current sources is shown. The voltage over a load of 50 kΩ was calculated as a function of time. At t=0, the 'electrode' is at 2.5 V, halfway Vdd and Ground. From t=0.5 µs until t=3.0 µs the cathodic source is switched on, from t=3 µs until t=5.5 µs the anodic source is switched on. The nominal current values are 10.4 µA (anodic) and 11.9 µA (cathodic); source impedance was 35.7 MΩ and 166 MΩ resp. The maximum switching delay was 0.78 µs. For a larger load (i.e. a larger electrode impedance) the switching delay becomes larger: at a load of 100 kΩ it is 2.30 µs.

The combination of a Gate Array for realization of the electronics with a flip-chip technique (accompanying paper) provides a widely applicable contacting technique. We feel it might be of use in many other applications where electrode arrays must be contacted.

ACKNOWLEDGMENT

The authors wish to thank J.W.A. van Dorsten and T.H. Hummel for designing the Gate Array layout, and the IC Technology and Electronics group at MESA for realization of the Gate Arrays.

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