Diode design for studying material defect distributions with avalanche-mode light emission

M. Krakers[1*], T. Knezevic[1,2], K.M. Batenburg[1], X. Liu[1], L.K. Nanver[1]
[1] MESA+ Institute, Faculty of EEMCS, University of Twente, Enschede, The Netherlands
[2] Micro and Nano Electronics Laboratory, Faculty of Electrical Engineering and Computing, University of Zagreb, Croatia
*Email: m.krakers@utwente.nl

***Abstract*— Avalanche-mode visual light emission in Si diodes is shown to be useful for rapid assessment of the origin of non-ideal currents. In the test structure design, it was important to consider the breakdown-voltage distribution, diode size and contact positioning to obtain light-spot appearances at positions related to bulk defect distributions.**

I. INTRODUCTION

In silicon single-photon avalanche diodes (SPADs), the presence of defects in and near the photo-sensitive diode depletion region is an undesirable source of dark counts [1], [2]. Such defects are also known to cause localized reduction of the diode breakdown voltage that, when operating the diodes as avalanche-mode light-emitting diodes (AMLEDs), may result in the early appearance of light-emission spots [3]. Optical on-chip data transmission has been demonstrated with AMLEDs as light source and SPADs as detectors, both integrated with the same basic design of the active diode region [4]. It was found that reducing defects in the active region was not only an advantage for reducing the SPAD dark count rate (DCR) but also for increasing the light-emission efficiency of the AMLED [5], [6]. The advantage for light emission was because defect-related localized early breakdown causes current-hogging, often resulting in spot-wise light emission, which inhibits a more efficient light emission from the whole photodiode surface.

In this paper we present an investigation of sets of PureB photodiodes that were originally designed as test structures for optimizing the operation as SPADs. The anode of the PureB diodes was formed by depositing nanometer-thin layers of pure boron on n-type silicon. This resulted in junction formation with low saturation currents resembling that of ideal deep p^+n junctions. Together with an exceptional robustness of both the PureB interface to the Si and the bulk boron layer itself, these properties have led an early commercialization of the photodiodes for high-dose beams with low-penetration depths in Si, such as vacuum-ultraviolet light and low-energy electrons [7], [8].

The PureB SPADs studied here were processed in two different runs that resulted in a number of abnormalities in the *I-V* characteristics. The electrical measurements were compared to light-emission patterns to help identify the origin of the abnormalities. In addition, material defects were sought by applying optical, scanning-electron (SEM), and atomic-force microscopy (AFM) to inspect the anode surface after different wet-etch treatments. The results of the material analysis gave useful extra information, but, in itself, the combination of *I-V* characterization and light-emission data gave insightful information on the position and distribution of undesirable defects and their relationship to the process flow.

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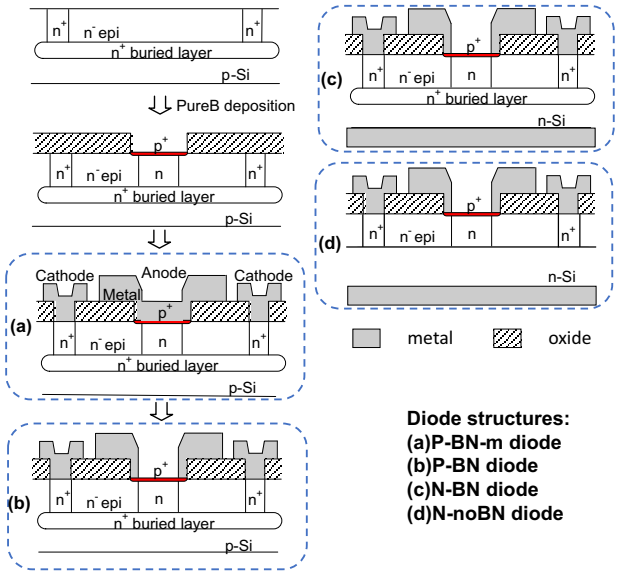

Fig. 1. Schematics of the 4 different diode structures under investigation. Left: The basic process flow for the fabrication of PureB SPADs with n^+ plugs to a buried n^+-layer on a p-type Si substrate, with the diode before (a) and after (b) metal removal. Right: Diodes fabricated on an n-type Si substrate with (c) and without (d) a buried n^+ layer.[5]

II. EXPERIMENTAL PROCEDURES

A. Design of diode test structures

Arrays of PureB diodes with variations in geometry and contacting method were fabricated. The basic process flow is shown in Fig. 1 for 4 different ways of fabricating the anode and cathode contacts. Two different runs were studied. The P-BN-m and P-BN devices were processed on the same p-type wafer and the N-noBN and N-BN devices on the same n-type wafer. Both wafers were (100) silicon with a resistivity of 2-5 Ω-cm. The cathode was formed by epitaxially growing a 1-µm-thick intrinsically-doped n-layer above n^+ buried layers. For the N-noBN diodes, the buried layer was omitted. To ensure low series resistance on the p-type substrates, the buried layers were contacted using n^+ plugs. To obtain avalanche breakdown away from the diode perimeter, the breakdown voltage was set by an n-enrichment region created by implanting phosphorus through a 30-nm-thick thermal silicon oxide, first at 40 keV to a dose of 10^{12} cm^{-2} and then at 300 keV to a dose of 5×10^{12} cm^{-2}. A 300-nm low-pressure chemical-vapor deposited silicon oxide was then deposited and the implants were annealed at 950°C for 20

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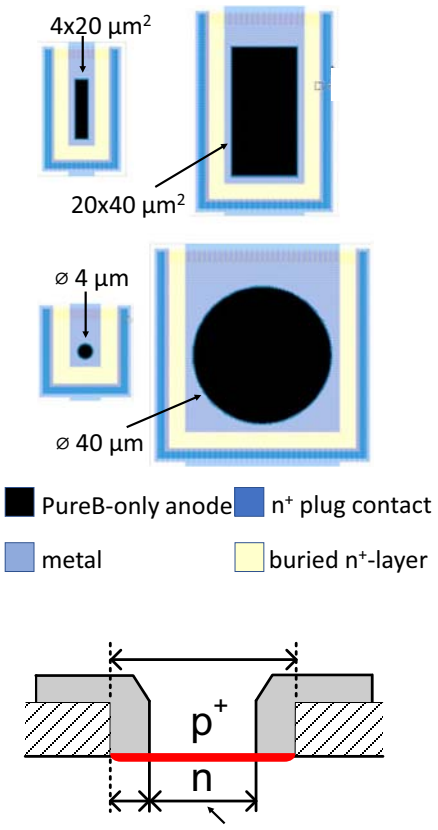

Fig. 2. Top: Examples of the PureB diode layouts for rectangular and circular light-entrance windows. Below: A schematic cross section of the metal contacting scheme of PureB diodes with an n-enrichment implantation. The L and W indicate the length and width, respectively, of the light entrance windows. For all the available anodes sizes, a $\Delta L = \Delta W = 0.5$ µm, 1.0 µm and 1.5 µm was implemented.

min. The windows to the Si defining the anode area were opened and covered with a PureB layer to a thickness of about 3 nm as described in [9]. The deposition temperature was 700°C, and followed by a drive-in for 1 min at 850°C. This resulted in doping of the surface Si giving a junction depth of about 15 nm and a sheet resistance of the p-type anode region of 1. 7 kΩ/sq. Finally, aluminum layers were deposited on both sides of the wafer and patterned to form the interconnect contacts to the cathode and the perimeter of the anode.

On the P-BN-m devices the metal covered the whole anode region while on the P-BN, N-noBN, and N-BN diodes the metal was removed to leave the central anode region with a PureB-only light-entrance window. The N-BN and N-noBN devices were processed on the same wafer but for the latter the BN was omitted. The most critical steps in the process flow were the window opening for the PureB deposition, and the removal of the Al metallization on the PureB surface.

The basic design of the test diodes is shown in Fig. 2 for circular and rectangular diodes. The circular diodes had light-entrance windows with 16 different diameters going from 2 µm to 40 µm. Likewise, sets of square and rectangular devices were also available with dimensions from 1 × 1 µm² up to 40 × 40 µm².

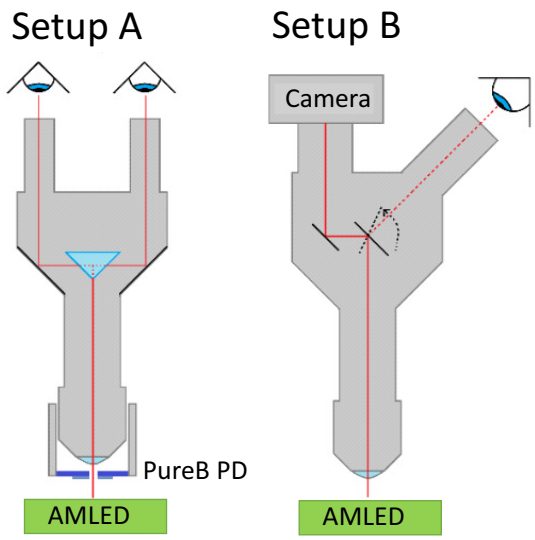

Fig. 3. Schematics of the 2 setups used for on-wafer biasing and monitoring of light emission from the diodes-under-test. Setup A: a PureB photodiode was mounted on the objective of the probe-station microscope to measure AM light emission; setup B: a camera is mounted on the microscope ocular for imaging of light emission across the diode surface.

B. Optoelectronic measurements

The diode *I-V* characteristics were measured on-wafer while monitoring AM light-emission in 2 different ways as shown in Fig. 3. The intensity of the emitted light was monitored using a ring-shaped PureB Si photodiode (PD) attached to the objective of the microscope as illustrated in Setup A. In AM, the light emission falls predominantly in the 400 nm to 800 nm wavelength range [10] which overlaps with the near-ideal responsivity of the PureB PD. Details of the setup are described in [5], [6].

Setup B was used to image the light emission over the surface of the diodes which allowed the identification of localized light spots and the voltage/current at which they appeared. The images were registered with a Nikon camera as a function of bias voltage. To avoid permanent damage to the devices, the reverse current levels were limited to 1 mA and only a few representative diodes were monitored through to breakdown current levels.

C. Surface analysis

Our material analysis techniques were limited to analysis of the surface morphology before and after wet etch removal of (parts of) the surface layers. Imaging of the diode surface was performed using optical microscopy, and AFM and SEM scans. The Al and B layers were removed using standard Al-etchant (80% POH, 16% acetic acid, 4% HNO_3) at 45°C for 4 min. PureB is resistant to TMAH (tetramethyl ammonium hydroxide) which is an effective Si wet etchant. Therefore, TMAH etch tests were performed on all diode designs to detect possible pinholes and weak spots in the PureB layers. The solution was 25% TMAH used at 85°C for 6 min, which, on a clean, lightly-doped Si (100) surface, would remove several micron of Si.

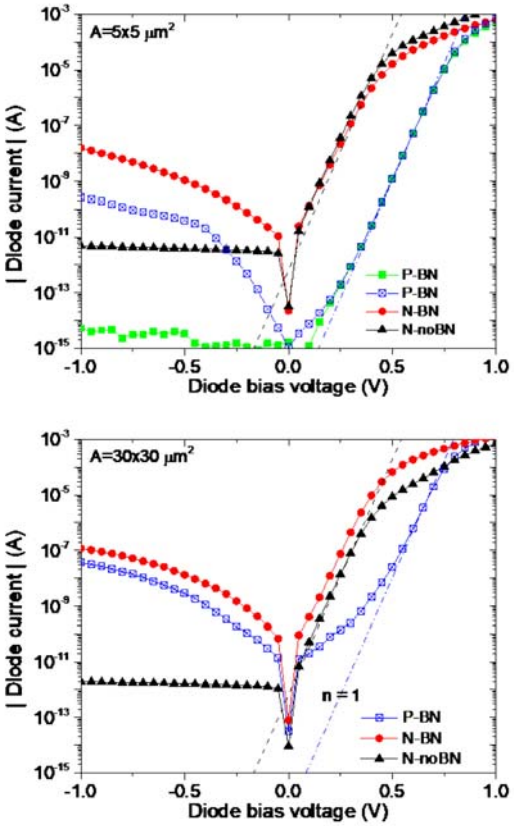

Fig. 4. Typical *I-V* characteristics measured on P-BN, N-noBN and N-BN diodes with sizes 5 × 5 μm^2 (top) and 30 × 30 μm^2 (bottom). Dashed lines indicate the ideality factor n = 1 relationship.

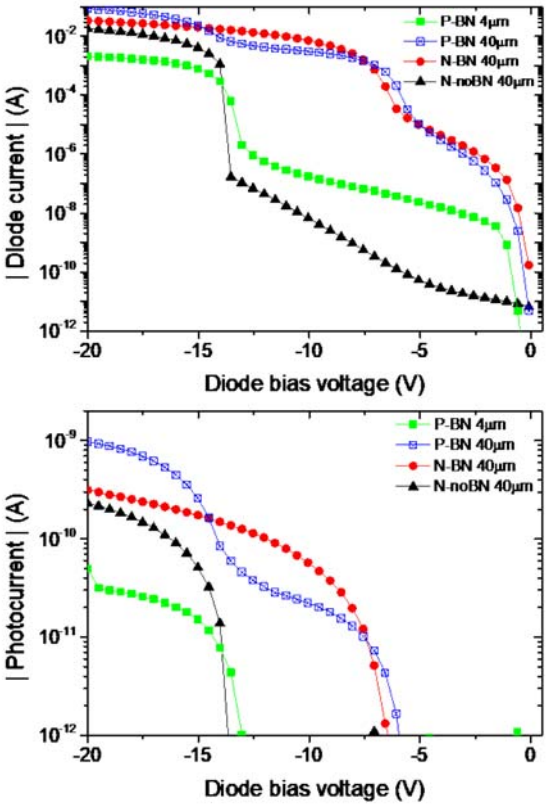

Fig. 5. Typical reverse *I-V* characteristics for P-BN, N-BN, and N-noBN diodes (top), and the photocurrents simultaneously measured using Setup A (bottom).

III. Results and Discussion

The low-voltage *I-V* characteristics of the 3 different types of diodes, P-BN, N-noBN and N-BN devices, are shown in Fig. 4 for representative devices. The P-BN have *I-V* characteristics that are typical of PureB diodes: the saturation currents, I_{sat}, are low, all below 10^{-16} A when extracted from the ideal part of the forward characteristics. Some of the small devices have ideal reverse currents with a flat curve that remains in the femto-ampere range all the way to 1 V reverse bias. In contrast, a number of small devices and all of the ones with anode areas larger than about 8 × 8 μm^2 have high non-ideal currents that strongly increase with reverse bias, reaching the nano-ampere range already at 1 V reverse bias. All the n-substrate diodes had decades higher saturation currents than the P-BN diodes. The N-noBN diodes had ideal characteristics with I_{sat} of about 10^{-12} A and a flat reverse current going to a few pico-amperes at 1 V reverse bias.

The N-BN devices had the same forward current levels as the N-noBN devices but in reverse they resembled the large P-BN devices, having high reverse currents that increased rapidly as the reverse voltage was increased. Typical breakdown characteristics for P-BN diodes are shown in Fig. 5. The ideal breakdown voltage, *BV*, set by the n-enhancement implant, was ~ 14 V for all devices. Most of the N-noBN diodes and small ideal P-BN had low reverse currents up to an abrupt breakdown at the ideal *BV*. This is the behavior that is needed for operation in Geiger mode. Most of the large devices and all the N-BN devices, exhibited signs of early impact ionization events seen as jumps in the reverse current levels that occurred once or twice in the course of the whole reverse bias sweep. Such jumps are presumably related to charge carriers emitted from defects in or near the high electric-field region of the diode depletion region that cause impact ionization events. The light-emission intensity, I_{PD}, measured with Setup A is also shown in Fig. 5. The impact ionization related to the current jumps around 7 V are seen to be sufficiently high for measurable light emission that otherwise was only detected beyond the breakdown voltage.

From the images taken with Setup B, the presence of AM light spots in the P-BN an N-BN devices became evident Examples are shown in Fig. 6 for a N-BN device with a large current jump at 7 V reverse biasing. The light intensity from each spot became higher and the number of visible spots increased as the reverse voltage was increased. Finally, the spots at the outer edge of the anode would join to form a bright ring. This was a result of the current crowding at the perimeter due to the voltage drop over the p^+ anode region at high currents. As opposed to this, the N-noBN devices did not display any visible spots but had a uniform, very slightly granular, ring-wise emission that appeared for biasing above the *BV*. Also, the small P-BN diodes with low reverse currents did not display any pre-*BV* light spots.

To summarize, 2 main abnormalities were identified in the optoelectronic voltage-dependent characteristics:

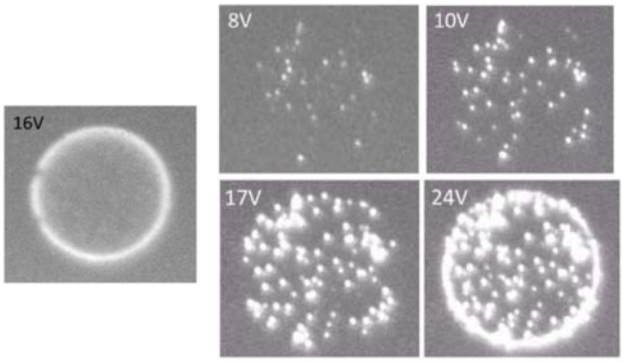

Fig. 6. Camera images of the light emission from reverse-biased circular N-noBN (left) and N-BN (right) diodes with a diameter of 40 µm. The applied bias voltage is given in each image.

- high, rapidly increasing reverse currents in the low-voltage region, and voltage jumps, particularly at about 7 V, in the high-voltage region, seen for some small P-BN, all large P-BN, and all N-BN diodes. The current jumps were correlated to spot-wise light emission.
- forward currents that were decades too high, seen for all N-noBN and N-BN diodes. In the N-noBN devices no spot-wise light emission was found.

To identify the origin of these optoelectrical abnormalities, a series of material analysis experiments were performed. Finally we were able to identify 3 types of defects, one type on the surface of the anode, one at the anode perimeter, and one in the bulk Si. The position of these defects is illustrated in Fig. 7, and the influence that each defect type had on the measurements will be briefly described in the following subsections.

A. Surface defects related to metal removal

As shown in Fig. 8, SEM and AFM imaging of the surface of the P-BN devices revealed small pits in the central anode region. Otherwise the surface was flat. TMAH etching increased the depth of these pits, whereas, in the P-BN-m devices no pits were seen on the central anode surface after removal of the Al with TMAH. This indicated that the PureB layer was damaged in the Al-removal step which first involved a plasma etch step to remove all but about 100 nm of Al. Any excessive plasma etching is known to result in etching through the Al grain boundaries and that can damage the underlying PureB-layer [11].

The remaining Al was removed by wet-etching with diluted HF. The damage pattern seen in Fig. 8 corresponded well with the granular pattern of the Al-metallization that can be seen on the interconnect at the anode perimeter. In support of this explanation, the shouldering effect during Al deposition also appears to have protected the surface from this damage at the anode perimeter as well as in the center of small devices.

Electrically this surface defect could not be related to the high reverse currents in the p-substrate devices because the frequency of this abnormality was similar for diodes both with and without metal removal. This is clear from the statistical analysis of *I-V* measurements shown in Fig. 9. In Fig. 9a the

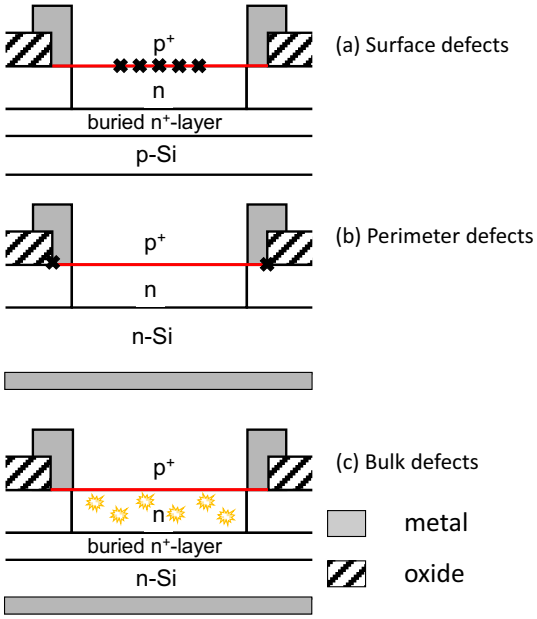

Fig. 7. Illustration of the three types of defects identified in the investigated PureB diodes. (a) Surface pitting seen on some diodes before treatment with wet-etch steps, and enhanced by TMAH etching, (b) perimeter pits seen on all diodes but only after TMAH etching, (c) bulk defects that were related to extra surface roughness but identified as bulk defects only through optoelectrical measurements.

differential forward current at 0. 6 V bias voltage for complete rows of P-BN and P-BN-m devices is plotted in order to extract the laterally uniform area current component, I_A, using the method described in [12]. The increase in current with differential diode size is regular and the same for both diode types, yielding a slope $I_A \sim 3 \cdot 10^{-10}$ A/µm^2. Therefore, the Al over-etching in the P-BN diodes was so limited that the actual p^+-Si anode-junction was not directly damaged. Moreover, the overlay of light-spot patterns with the AFM images of one P-BN diode, as shown in Figs. 8b and 8c, revealed no direct correlation to this surface damage.

B. Perimeter defects related to thin B coverage

The TMAH etching of all types of devices resulted in large irregular pitting at many positions along of the perimeter of the anode region, an example of which is shown in Fig. 10. This is not an unexpected effect since the PureB coverage of the Si at the perimeter is a critical step in the processing that depends on the exact morphology of the oxide window edges and the exact treatment of the Al metallization. If the separation that the PureB offers between the Al and the underlying Si becomes too small, high saturations currents may occur [14], [13]. The TMAH-induced perimeter pits were pronounced, and equally large, for

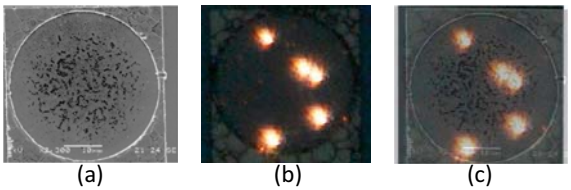

Fig. 8. Images of a circular P-BN diode with diameter 40 µm, taken with (a) the SEM, and (b) setup B during a reverse biasing of 15 V. In (c) an overlay is shown of (a) and (b).

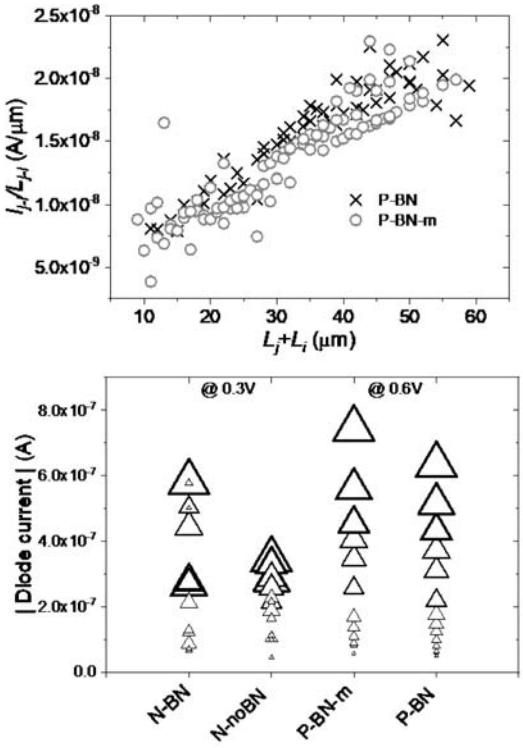

Fig. 9. (a) The differential forward current at 0.3 V for all the 16 sizes of square P-BN and P-BN-m devices as a function of the sum of light-entrance window lengths L_j+L_i. (b) The forward diode current measured on 16 square diodes with L = 1 µm to 40 µm, at 0.3 V for N-BN and N-noBN diodes, and at 0.6 V for P-BN and P-BN-m diodes. The symbol sizes are directly proportional to L.

both the N-noBN and N-BN diodes. Therefore, we concluded that the window processing in this run was responsible for the high forward current levels. This was supported by the light emission measurements that showed the same behavior as for the P-BN devices that had ideally low forward currents and therefore could be assumed to have the desired good PureB coverage of the oxide window perimeter. The excessively high perimeter currents were limited to the region outside the n-enhancement region and did therefore not influence the current/voltage distribution in the rest of the device. The forward *I-V* characteristics of N-BN and N-noBN devices were dominated by irregular perimeter currents that were about 3 decades higher than the laterally uniform area currents so I_A could not be extracted as for the P-BN devices. This can be concluded from Fig. 9b where the distribution of the diode current is plotted for square devices. While the P-BN and P-BN-m devices show a regular increase with device area, the N-BN and N-noBN devices do not show this at all.

C. Bulk defects related to n⁺-buried-layer processing

The abnormally high reverse currents and spot-wise light emission had only been found in devices with an n⁺-buried layer, while the high forward currents in the n-substrate devices could only be related to perimeter defects. Therefore, more evidence was sought to confirm that the processing of buried layer was indeed the source of the high reverse leakage. As shown in Fig. 11a, measurements using 12 p-substrate devices for each of the areas from 1 × 1 µm² to 6 × 6 µm², revealed that the frequency

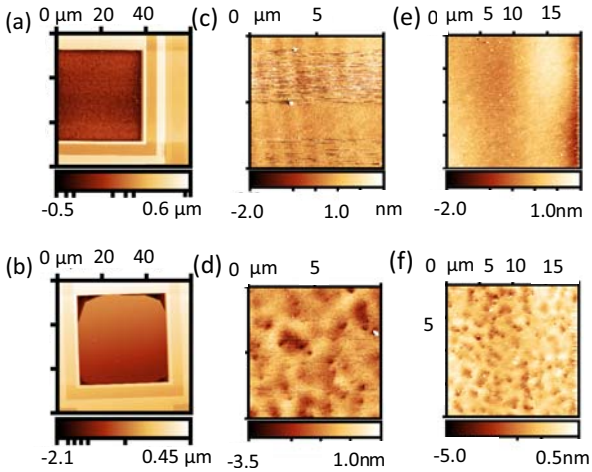

Fig. 10. AFM scans of n-type diode surfaces before and after etch tests. An N-BN diode before (a) and after (b) TMAH etching upon which etch pits appear in the corners. Anode surface scans for an N-noBN (c) and an N-BN (d) diode after TMAH-etching, and an N-noBN (e) and an N-BN (f) diode after PureB removal.

of non-defected devices increased as the area decreased. For example, for the 1 × 1 µm² devices, only 2 of the twelve measured devices were defect while this number was 10 for the 6 × 6 µm² devices. The results suggest that these bulk defects were discrete with a density of about 1 per µm², i.e., 10^8 cm^{-2}. This defect density corresponded well with the density of light spots seen in the camera images. In addition, AFM surface analysis of diodes with a buried layer revealed a clear surface roughness pattern that was very different from the smooth

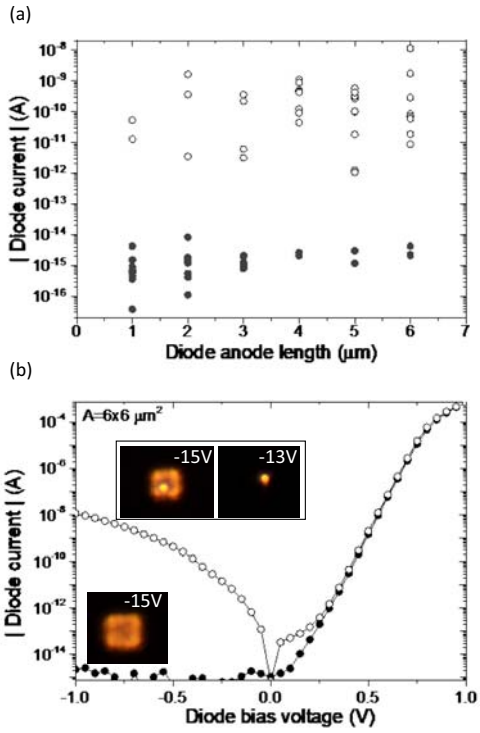

Fig. 11. (a) The current measured at 1 V reverse bias for sets of 12 diodes (6 P-BN and 6 P-BN-m) as a function of diode length, grouped in closed circles for ideally low currents and open circles for high reverse currents. (b) *I-V* characteristics of two P-BN devices and images of their AM light emission patterns.

surface of the N-noBN devices, examples of which are shown in Fig. 10. This buried-layer-related surface roughness did not influence the PureB coverage: after TMAH etching the central diode areas did not change morphology indicating a complete B-layer protection of the Si as also seen for the N-noBN devices. Since the forward currents of the P-BN devices were all ideally low, and abnormally high currents were only seen as the voltage approached reverse values, increasing considerably with increasing reverse bias, it was concluded that the responsible defects were located in the bulk epitaxially-grown Si layer above the buried layer. In later transistor experiments it was confirmed that a contamination of the Si surface before the buried layer processing was causing stacking faults in the epitaxial layer.

IV. Conclusions

The optoelectrical study of the PureB diode *I-V* characteristics in relationship to light-emission spots was useful for gaining information on the distribution and origin of defects that were causing non-ideal currents detrimental for the application as SPADs. In particular, we were able to relate bulk Si defect distributions of about 10^8 cm^{-2} to a contamination problem in the n^+-buried-layer processing, and non-optimal oxide window processing was found to have caused very high perimeter leakage without effecting the desired current flows in the central anode region responsible for making Geiger-mode operation possible. Material analysis gave support of these conclusions. The investigation profited from the availability of test-diodes with many sizes from a single to tens of micron, and it was important that the diode breakdown was removed from perimeter so that light emission over the whole diode surface could be generated. The minimum size of the diodes needed for observing light spots increases as the density of defects decreases. If light-emitting defects are present, more and more spots will appear as the reverse voltage is increased but current hogging due to series resistance and/or light spots will eventually lead to light-emission predominantly near the anode contacts. Therefore, in the design of the test structures, the position of the contacts should be considered as well as the breakdown voltage distribution across the diode. Compared to the material analysis techniques that required extra processing to remove surface layers, the imaging of light emission offers a fast screening method for identifying possible problems in the diode processing.

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