A CMOS Four-Quadrant Analog Multiplier

KLAAS BULT AND HANS WALLINGA, MEMBER, IEEE

Abstract—A new circuit configuration for an MOS four-quadrant analog multiplier circuit is presented. It is based on the square-law characteristics of the MOS transistor. Two versions have been realized. The first has a linearity better than 0.14 percent for an output current swing of 36 percent of the supply current and a bandwidth from dc to 1 MHz. The second version has floating inputs, a linearity of 0.4 percent at an output current swing of 40 percent of the supply current and a bandwidth from dc to above 4.5 MHz.

I. Introduction

FOUR-QUADRANT analog multipliers are very useful building blocks in many circuits such as adaptive filters, frequency-shifters, and modulators. Analog multipliers have received severe attention in bipolar technology [1]. Even in CMOS technology, multipliers using (lateral) bipolar transistors have been reported [2]. Until now only a few CMOS multiplier designs have been published. Single-quadrant multipliers have been reported in [3] and [4]. In [5] and [6] four-quadrant multipliers using switched-capacitor techniques have been described. A continuous-time CMOS multiplier has been presented by Soo and Meyer [7]. Their circuit approach is based on the well-known bipolar circuit concept described by Gilbert [1]. In this paper we report on a new approach for a four-quadrant analog multiplier which has been realized in CMOS technology. This multiplier relies on the quadratic drain-current/gate-voltage characteristics of MOS transistors operated in saturation. First a novel voltage-controlled linear $V-I$ convertor is explained (Section II). Combining two of these circuits results in a two-quadrant multiplier, and again duplicating this circuit results in the four-quadrant multiplier (Section III). Then in Section IV a distortion analysis is presented. Section V describes the design of a second version of the multiplier with floating inputs and Section VI shows the results of the measurements.

II. The Basic Voltage-Controlled $V-I$ Convertor

In this section all devices have the same geometry and operate in the saturation region. The simple square-law characteristic is assumed

$$I_d = K(V_{gs} - V_t)^2 \tag{1}$$

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The authors are with the Department of Electrical Engineering, IC Technology and Electronics Group, Twente University of Technology, 7500 AE Enschede, The Netherlands.

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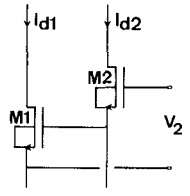

Fig. 1. The basic circuit.

with

$K = \mu \cdot C_{ox} \cdot W/L$,

μ = carrier mobility,

C_{ox} = gate oxide capacitance per unit area,

W = channel width, and

L = channel length.

Consider the circuit of Fig. 1. The gate–source voltages of the two identical MOS transistors $M1$ and $M2$ are, respectively, V_{gs1} and V_{gs2}. The sum of the gate–source voltages is kept at a constant voltage V_2:

$$V_{gs1} + V_{gs2} = V_2. \tag{2}$$

Furthermore

$$I_{d1} = K(V_{gs1} - V_t)^2$$

and

$$I_{d2} = K(V_{gs2} - V_t)^2. \tag{3}$$

Applying $A^2 - B^2 = (A+B)(A-B)$ to (2) and (3), the output current difference $(I_{d1} - I_{d2})$ may be written as

$$I_{d1} - I_{d2} = K(V_2 - 2V_t)(V_{gs1} - V_{gs2}). \tag{4}$$

Because

$$V_{gs1} - V_{gs2} = V_2 - 2V_{gs2} = 2V_{gs1} - V_2 \tag{5}$$

we may, for constant V_2, conclude that the output current $(I_{d1} - I_{d2})$ is linearly dependent on V_{gs1} or V_{gs2} (only one of the two parameters can be chosen independently). Extension of the circuit in Fig. 1 with another identical transistor $M3$ as shown in Fig. 2 enables us to control V_{gs2} via V_{gs3}. Because $M2$ and $M3$ have the same drain current and both devices have the same geometry, the gate–source voltages V_{gs2} and V_{gs3} are equal:

$$V_{gs2} = V_{gs3} = V_{\text{in}}. \tag{6}$$

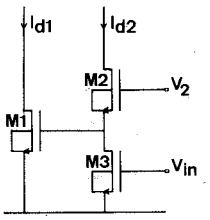

Fig. 2. The voltage-controlled $V-I$ convertor.

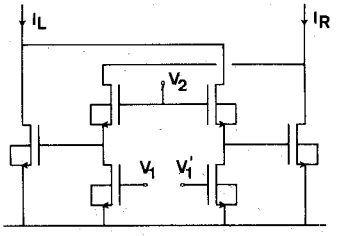

Fig. 3. Two-quadrant multiplier.

Substitution of (6) and (5) into (4) yields

$$I_{d1} - I_{d2} = K(V_2 - 2V_t)(V_2 - 2V_{\text{in}}). \tag{7}$$

Apart from the term $(V_2 - 2V_t)V_2$, (7) shows a linear relationship between $(I_{d1} - I_{d2})$ and V_{in}. The conversion factor can be controlled by means of V_2. For proper operation it is required that all three transistors operate in the saturation region, i.e.,

$$V_{\text{in}} > V_t$$

and

$$V_2 > 2V_{\text{in}} - V_t. \tag{8}$$

III. The Multiplier

Equation (7) may be rewritten as

$$I_{d1} - I_{d2} = K\left(V_2^2 - 2V_tV_2 + 4V_tV_{\text{in}} - 2V_2V_{\text{in}}\right). \tag{9}$$

The last term of (9) represents a one-quadrant multiplication. The first term, however, is a nonlinear function of the terminal voltage V_2 and the second and third term turn up as offset terms. Duplication of the circuit of Fig. 2 and cross coupling of the output currents results in the circuit of Fig. 3 in which the same voltage is applied to both V_2 terminals. The input voltages V_{in} are termed V_1 and V_1', respectively. Now the output current difference of the overall circuit may be written as

$$I_L - I_R = 2K(V_2 - 2V_t)(V_1' - V_1). \tag{10}$$

This represents a two-quadrant multiplier. Note the disappearance of the nonlinear quadratic term of V_2 and of the offset term for the V_1 input. By again duplicating this circuit and cross coupling the output currents (Fig. 4), a four-quadrant multiplier is obtained. Current mirrors have been added to obtain a single-ended output. The output current is now given by

$$I_{\text{out}} = 2K(V_2 - V_2')(V_1' - V_1). \tag{11}$$

The offset term for the V_2 input has disappeared too.

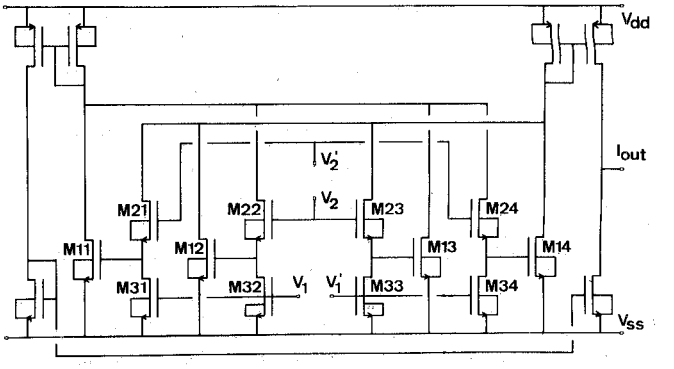

Fig. 4. Four-quadrant multiplier.

IV. Second-Order Effects

There are two major effects causing deviations from the ideal square-law behavior of (1): channel-length modulation and mobility reduction.

a) *Channel-length modulation* causes the drain current to be dependent on the drain voltage. In first-order approximation, this may be modeled by

$$I_d = I_{d,\text{sat}}\left(1 + \lambda\left(V_{ds} - V_{ds,\text{sat}}\right)\right) \tag{12}$$

with

$$I_{d,\text{sat}} = K\left(V_{gs} - V_t\right)^2$$

$$V_{ds,\text{sat}} = \left(V_{gs} - V_t\right)$$

$$\lambda = \frac{1}{L}\sqrt{2\epsilon_0\epsilon_{\text{Si}}/qN_d}.$$

Substitution of these terms in (12) yields

$$I_d = K\left(V_{gs} - V_t\right)^2 + \lambda K V_{ds}\left(V_{gs} - V_t\right)^2 - \frac{\lambda K}{A}\left(V_{gs} - V_t\right)^3. \tag{13}$$

The first term is the well-known and wanted quadratic term. The last term is a third-order term which will cause first and third harmonics of the input gate voltage in the drain output current. The second term is quadratic in $(V_{gs} - V_t)$ but also depends on V_{ds}.

The effect of channel-length modulation can be reduced by using long-channel MOS transistors. Before going into the effect of channel-length modulation on the performance of the multiplier we will consider the mobility reduction.

b) *Mobility reduction* in an MOS transistor may be modeled by

$$\mu = \mu_o/\left(1 + \theta\left(V_{gs} - V_t\right)\right) \tag{14}$$

with

μ_o = zero field mobility,

$\theta = 1/(d_{ox} \cdot E_{cr})$,

d_{ox} = oxide thickness, and

E_{cr} = critical field.

The mobility reduction parameter θ is process dependent and may have values ranging from 0.01 to 0.25 V^{-1}. This means a deviation from the nominal value of K in (1) ranging from 1 to 20 percent for 1-V change in V_{gs}. With the use of (14), (1) may be developed into a Taylor series

$$I_d = K_0(V_{gs}-V_t)^2\left[1-\theta(V_{gs}-V_t)+\theta^2(V_{gs}-V_t)^2 - \theta^3(V_{gs}-V_t)^3\cdots\right] \quad (15)$$

with

$$K_0 = \mu_o \cdot C_{ox} \cdot W/L.$$

For $\theta(V_{gs}-V_t)<1$, higher order terms become less important. As θ is a process-dependent parameter it cannot be made small by optimizing the geometries of the devices.

The following analysis shows that in the circuit configuration of Fig. 4 some of the distortion terms cancel. In this analysis, ideal matching of the transistors is assumed and I_d is supposed to be a function of the gate–source voltage only. The second term in (13) is made small by using long devices.

Irrespective of the origins of the deviations from the ideal square–law characteristic, one can develop a Taylor series for the expression of the drain current as a function of the gate–source voltage

$$I_d = K_0\left[a_0 + a_1(V_{gs}-V_t)+a_2(V_{gs}-V_t)^2 + a_3(V_{gs}-V_t)^3+\cdots\right]. \quad (16)$$

We define the following common-mode and differential voltages:

$$\begin{aligned} V_{1c} &= (V_1+V_1'-2V_t)/2 \\ V_{2c} &= (V_2+V_2'-2V_t)/2 \\ V_{1d} &= (V_1-V_1')/2 \\ V_{2d} &= (V_2-V_2')/2. \end{aligned} \quad (17)$$

With a straightforward calculation up to the fifth-order expansion of I_d it can be shown that with the aforementioned assumptions, the output current I_{out} of the circuit of Fig. 4 can be written as

$$\begin{aligned} I_{\text{out}} = K_0\Big[& V_{2d}\cdot V_{1d}\left\{2a_2+6a_3(V_{2c}-V_{1c}) \right. \\ & \left. +12a_4(V_{2c}-V_{1c})^2+20a_5(V_{2c}-V_{1c})^3\right\} \\ & + V_{2d}^3\cdot V_{1d}\cdot\left\{a_4+5a_5\cdot(V_{2c}-V_{1c})\right\} \\ & + V_{1d}^3\cdot V_{2d}\cdot\left\{a_4+5a_5(V_{2c}-V_{1c})\right\}\Big]. \end{aligned} \quad (18)$$

For purely differential input voltages the common-mode voltages V_{1c} and V_{2c} are constant and the terms in (18) between braces are constant. In that case the expression for I_{out} may be abbreviated to

$$I_{\text{out}} = C_1\cdot V_{2d}\cdot V_{1d} + C_2\cdot V_{2d}^3\cdot V_{1d} + C_3\cdot V_{1d}^3\cdot V_{2d}. \quad (19)$$

From (18) it becomes clear that only fourth and higher order terms in (16) give rise to distortion. As mentioned above, channel–length modulation can be reduced by using long devices. The mobility reduction, however, is geometry independent and is a much more serious cause of distortion. If mobility reduction is assumed to be the only origin of distortion, the constants a_i $(i=0,1,\cdots)$ in (16) can be determined by comparison with (15). This results in

$$\begin{aligned} a_0 &= a_1 = 0 \\ a_2 &= 1 \\ a_3 &= -\theta \\ a_4 &= \theta^2 \\ a_5 &= -\theta^3 \quad \text{etc.} \end{aligned} \quad (20)$$

This means that the most important distortion terms in (19), i.e., $C_2\cdot V_{1d}^3\cdot V_{2d}$ and $C_3\cdot V_{2d}^3\cdot V_{1d}$, are proportional to θ^2, which indicates the order of magnitude of the distortion.

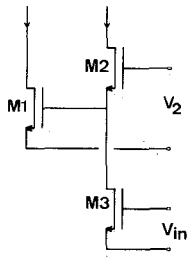

Fig. 5. The voltage-controlled $V-I$ convertor with independent control of the dc levels of both inputs.

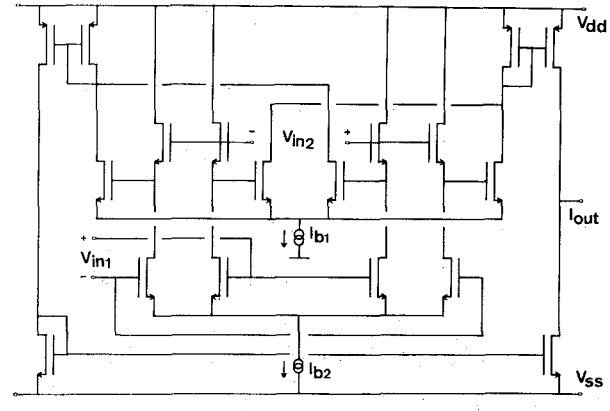

Fig. 6. Four-quadrant multiplier with floating inputs.

V. The Multiplier with Floating Inputs

A disadvantage of the circuit of Fig. 4 is that the common-mode voltage of the inputs are simultaneously bias voltages. A way to circumvent this problem is introduced in this section. Fig. 5 shows again the subcircuit of three transistors as shown in Fig. 2, but with one modification: the sources of $M1$ and $M3$ are disconnected. This does not influence the function of the circuit: (2)–(9) still hold for this version. The result, however, is independent control over the common-mode levels of both inputs. The next step is to quadruple this circuit in the same way as in the circuit of Fig. 4 and to connect the common sources to

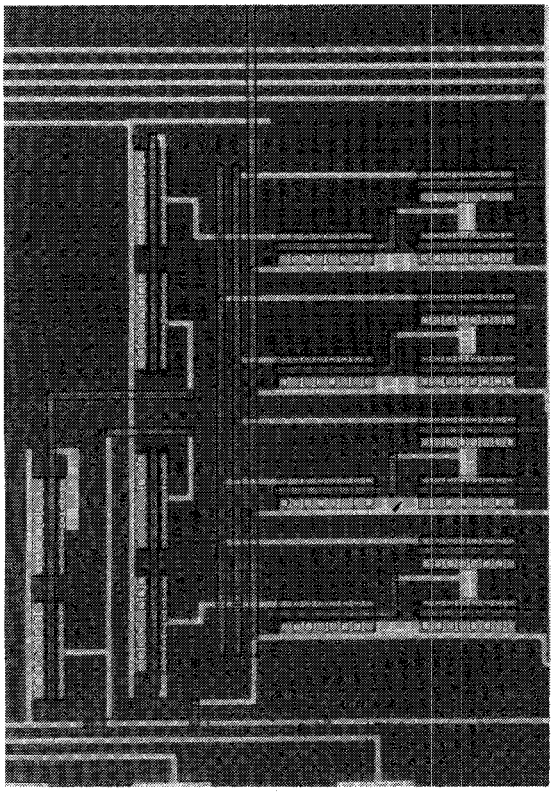

Fig. 7. Die photograph of the circuit of Fig. 4.

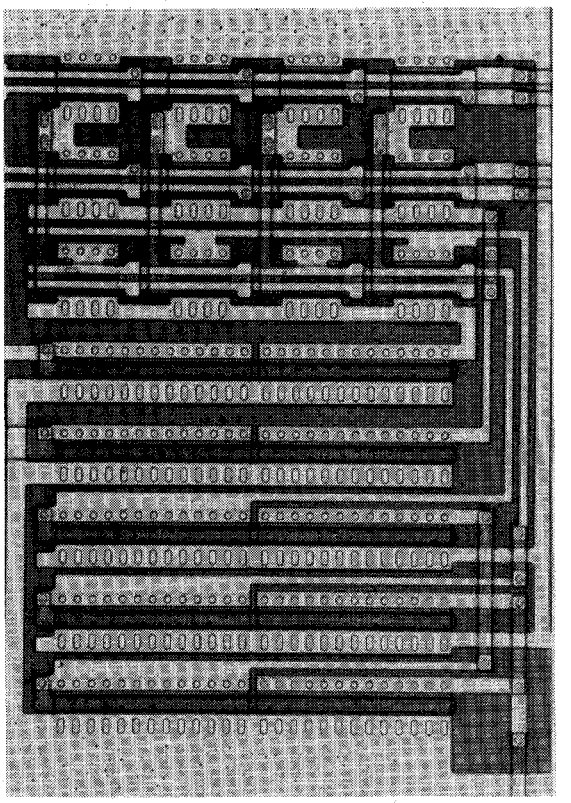

Fig. 8. Die photograph of the circuit of Fig. 6.

current sources as shown in Fig. 6. Furthermore, current mirrors have been added to obtain a single-ended output.

Fig. 6 shows another difference with the circuit of Fig. 4: the drains of the transistors at the V_2 input are connected to V_{dd} instead of to the output current mirrors. As is seen in Fig. 4, the branches with $M31$ and $M32$ conduct the same current because their gate–source voltages are equal. However, the currents in these branches cancel as they are connected to opposite current mirrors. The same holds for the branches with $M33$ and $M34$. As these currents do not contribute to the final output signal they are directly drained to the supply, which is advantageous for the discrimination of noise. We now have a four-quadrant multiplier with independently floating inputs. There is one restriction: conditions (8) have to be fulfilled for each of the basic subcircuits of three transistors.

Unfortunately, for this second version of the multiplier, the terms between braces in (18) are not constant and the distortion analysis becomes much more complicated. This is due to the fact that now V_{2c} and V_{1c} are not referenced to ground but to the common-source nodes. A detailed distortion analysis is beyond the scope of this paper and we refer to the experimental results in the next section.

VI. Experimental Results

Both versions of the multiplier (Figs. 4 and 6) have been realized. Figs. 7 and 8 show the die photographs of the circuits of Figs. 4 and 6. These IC's have been fabricated in the IC processing facility of Twente University of Technology using a retrograde twin-well CMOS process

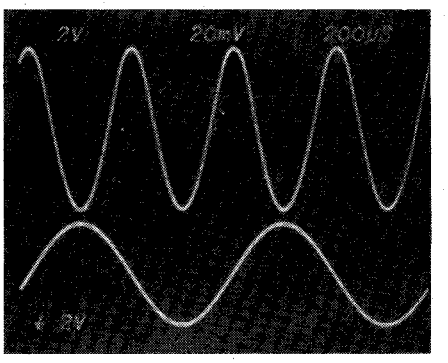

Fig. 9. Multiplication of two sine waves of the same frequency (circuit of Fig. 4).

[8], [9]. As this process has isolated n-wells, both circuits have been realized with p-channel transistors because the body effect may be reduced by connecting the well substrates to the sources of the p-channel MOST's. N-channel transistors have only been used as current mirrors to obtain a single-ended output current.

The circuit of Fig. 4 was processed with a threshold voltage of -0.6 V for the p-channel transistors and an oxide thickness of 50 nm. All devices of this design have the same geometry: $W=120$ μm, $L=10$ μm. The active area, including current mirrors, is about 86 400 μm^2.

Fig. 9 shows the performance of the multiplier as a frequency doubler; the input signals are two in-phase 1-kHz sine waves of 3.5 V_{p-p}. The output is a sine wave of twice the input signal frequency and has a magnitude of 44 mV_{p-p} measured over a 100-Ω load resistor, i.e., an output

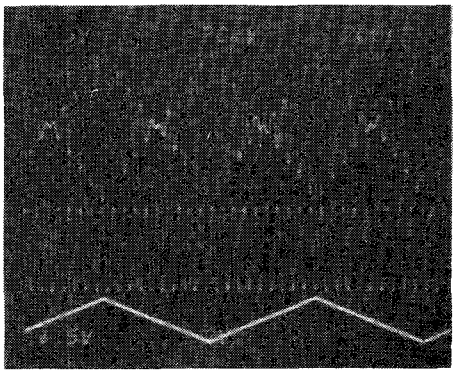

Fig. 10. Modulated triangle wave (circuit of Fig. 4).

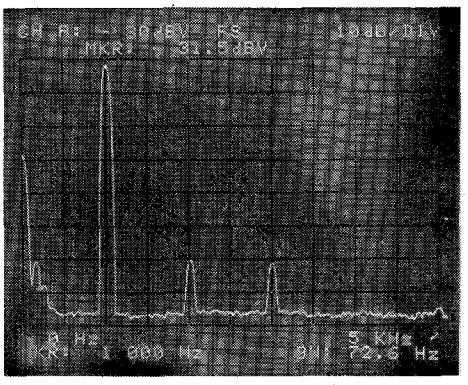

Fig. 11. Spectral contents of a sine wave at the output of the multiplier of Fig. 4.

current of 0.44 mA_{p-p}. The total supply current was 2.0 mA.

Fig. 10 shows the multiplier performance as a modulator. A 3.5-V_{p-p} triangle wave was applied to the V_1 inputs and a 3.8-V_{p-p} sine wave was applied to the V_2 input. The output current amplitude measured in a 100-Ω load resistor was 0.9 mA_{p-p}. The total supply current was 1.0 mA.

With a 3-V dc voltage applied to the V_1 input, the multiplier was used as a linear control circuit. Fig. 11 shows the spectrum of the output signal with a 1-kHz sine wave of magnitude 1.7 V_{p-p} at the input. The output current was 0.6 mA_{p-p} in a 100-Ω load resistor. The second and third harmonics are both 60 dB below the fundamental.

The total harmonic distortion was measured as a function of the current efficiency $I_{out,p-p}/I_{supply}$ by varying the magnitude of a 1-kHz sine wave applied to the V_2 input. Fig. 12 shows the result. The bandwidth of this circuit measured with a load resistor of 100 Ω and a load capacitor of 50 pF is from dc to above 1 MHz.

The circuit of Fig. 6 was realized with a threshold voltage of −0.2 V for the p-channel transistors and an oxide thickness of 25 nm. The transistors used in the core of the multiplier all have the same geometry: $W = 40$ μm, $L = 20$ μm. The transistors used in the current mirrors have been designed much larger: $W = 130$ μm, $L = 10$ μm. The active area including current mirrors is about 76 000 μm^2.

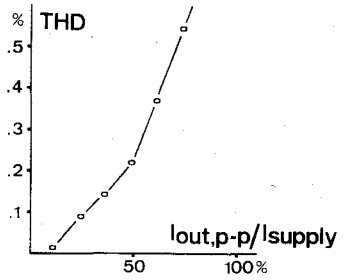

Fig. 12. The total harmonic distortion as a function of the current efficiency $I_{out,p-p}/I_{supply}$ (circuit of Fig. 4). $I_{supply} = 1.65$ mA.

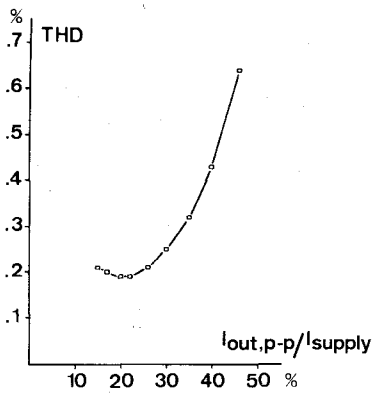

Fig. 13. The total harmonic distortion as a function of the current efficiency $I_{out,p-p}/I_{supply}$ (circuit of Fig. 6). $I_{supply} = 1.88$ mA.

The measured bandwidth of this circuit was from dc to 4.5 MHz. The total harmonic distortion as a function of the current efficiency is shown in Fig. 13. A dc voltage of 5.3 V was applied to the V_1 input and a 1-kHz sine wave of variable magnitude was applied to the V_2 input.

VII. Discussion

The experimental results show an excellent performance for both versions of the multiplier. However, the total harmonic distortion of the first version is essentially lower than the total harmonic distortion of the second version (Figs. 12 and 13), even though the channel length of the devices in the second version was larger. First, it has to be pointed out that the circuits have been fabricated with different oxide thicknesses. The oxide thickness of the first version was twice as large as that of the second version. Referring to (14) we note that the mobility reduction parameter θ in the second version is twice as large as in the first version. Moreover, as mentioned in Section V, the common-mode voltages V_{2c} and V_{1c} in the distortion analysis of Section IV are not constant for the second version. It can be shown that for this version

$$V_{1c} = \frac{1}{2}\sqrt{\frac{I_{b2}}{K} - 4V_{1d}^2}. \tag{21}$$

Now (18) predicts distortion terms caused by third-order terms in (16) and according to (20) this means that these terms are proportional to θ instead of θ^2.

The dominant poles in both designs are determined by the nodes at the sources of the input devices of the V_2 input. The bandwidth can be improved by increasing the current in these branches. Measured input offset voltages were typically less than 15 mV. No statistical analysis could be performed because only a few devices were available.

VIII. Conclusions

An extremely simple and compact design for a CMOS four-quadrant multiplier circuit has been presented. The design is based on the square-law characteristics of the MOS transistor in saturation. Two versions have been realized of which the second version has floating inputs. The first version has a measured total harmonic distortion of 0.14 percent at a current efficiency $I_{\text{out,p-p}}/I_{\text{supply}}$ of 36 percent, a bandwidth, measured with a load resistor of 100 Ω and a load capacitor of 50 pF, from dc to 1 MHz, and a supply current I_{supply} of 1.65 mA. The second version has a measured total harmonic distortion of 0.3 percent at a current efficiency of 40 percent, a bandwidth, measured with a load resistor of 100 Ω and a load capacitor of 50 pf, from dc to 4.5 MHz, and a supply current of 1.88 mA.

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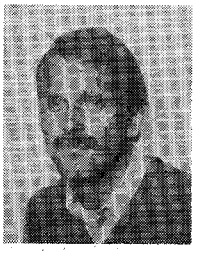

Klaas Bult was born in Mariënberg, The Netherlands, on June 26, 1959. He received the M.S. degree in electrical engineering from Twente University of Technology, Enschede, The Netherlands, in 1984, on the subject of a design method for CMOS op amps. He is now working towards the Ph.D. degree on the subject of analog computational circuits for applications in analog adaptive filters.

Hans Wallinga (M'81) received the M.S. degree in physics from the State University of Utrecht, The Netherlands, in 1967 and the Ph.D. degree in technical sciences from Twente University of Technology, Enschede, The Netherlands, in 1980.

In 1967 he joined Twente University of Technology, where he initially was involved in device physics and device characterization of MOST's and CCD's. Since 1975 he has been working on CCD filters and electrically programmable CCD filters. His present interest is mainly in the design of sampled data analog signal-processing circuits. He teaches courses on semiconductor devices and sampled data circuits. He was Visiting Research Fellow at General Electric Research Corporate, Schenectady, NY, from August 1980 to February 1981.