Design and Analysis of CMOS Analog Signal Processing Circuits by Means of a Graphical MOST Model

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Abstract — **A graphical representation of a simple MOST model is given for the analysis of analog MOS circuits operating in strong inversion. It visualizes the principles of signal processing techniques depending on the characteristics of an MOS transistor. Several linearization techniques as well as a multiplying principle become transparent at the hand of the graphical representation. In the examples special attention is focused on continuous-time filter techniques. The basics of MOSFET-C continuous-time filters and CMOS square-law circuits are explained using the graphical MOST characteristics representation.**

I. Introduction

RECENTLY a number of papers have been published on continuous-time analog CMOS signal processing [1]–[9]. In contrast to discrete-time analog signal processing circuits, such circuits are free from Nyquist constraints, have no switching noise (as in switched capacitor circuits), have no noise aliasing into the baseband, and do not need antialiasing or smoothing filters.

There is a special need for linear conductances and/or transconductances in continuous-time filter applications. Realization of these basic devices in CMOS demands linearization techniques. The design of such circuits requires a good understanding of the operation of an MOS transistor. Good simulation tools are needed for an accurate quantitative analysis, but a handy MOST model is indispensable for creative circuit design and qualitative analysis. A graphical representation of the relationships between voltages and currents in an MOS transistor or circuit can be of great help.

The graphical representation method which will be used here has been described more comprehensively in [11]. It was developed at the University of Twente and has been used successfully for more than ten years in teaching courses in Twente as well as at the Université Catholique de Louvain (Belgium). At the latter university considerable effort has been expended in applying the model to static and dynamic logic circuits [11]. It has now been adopted by several European universities. In this paper we will show how the graphical representation method can be used for the analysis of recently published continuous-time analog CMOS signal processing circuits [1]–[9].

In continuous-time CMOS filters, linearization techniques can be roughly divided into two categories. One way is linearization of the MOST channel conduction in the linear mode, leading to the so-called MOSFET-C filters [1]. The other involves CMOS square-law circuits, in which the quadratic dependence of the drain current on the gate–source voltage is used [2]. First, in Section II, we will explain the graphical representation method, and in Section III its merits and shortcomings are discussed. Then in Section IV a number of examples are given of the application of the graphical representation method to MOSFET-C filter circuits and to square-law circuits. Section V presents the conclusions.

II. Simple MOST Model and the Graphical Representation

In this section we explain briefly a graphical representation method for the operation of the MOS transistor, based on a simple MOST model. The model describes the drain current of an MOS transistor operating in strong inversion as a function of the four terminal voltages. In the model all voltages are referred to the substrate potential instead of the source potential, yielding a more integrated circuit oriented model. Moreover, in this way the symmetry between source and drain is emphasized, both in the expressions and in the graphical representation.

Consider Fig. 1, which shows a cross section of an MOS transistor. For purposes of clarity, we will confine the explanation to n-channel MOS transistors, but the model applies equally well for p-channel MOST's. We will start by defining the *channel voltage* $V_C(x)$ at a certain position x in the channel. This channel voltage $V_C(x)$ is an imaginary voltage which varies along the channel from the source voltage V_S $(x = 0)$ to the drain voltage V_D $(x = L)$. It can be seen as the voltage in the channel at position x as it would be *measured externally* via a silicon probe with a similar doping profile and metal contacts as the source and

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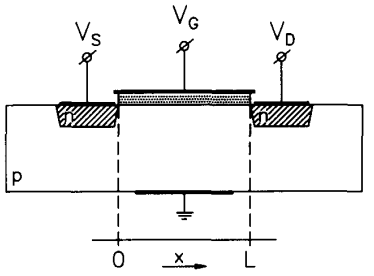

Fig. 1. Cross section of an n-channel MOS transistor.

drain diffused regions. As all internal contact potentials are included in the probe construction, we can describe the voltage–charge relations in the MOST with *external* terminal voltages.

The threshold voltage V_T, referred to the substrate, defines the gate voltage at the onset of strong inversion and is a function of the channel voltage V_C. The classical expression [10] for $V_T(V_C)$ is

$$V_T(V_C) = V_{FB} + V_C + 2|\phi_p| + |Q_d^{\square}(V_C)|/C_{ox}$$
$$= V_{T0} + V_C + |\Delta Q_d^{\square}(V_C)|/C_{ox} \quad (1)$$

with

V_{FB} flat-band voltage,
ϕ_p internal substrate potential,
$Q_d^{\square}(V_C)$ depletion layer charge density,
C_{ox} gate oxide capacitance per unit area,

$$V_{T0} = V_T(0)$$

and

$$|\Delta Q_d^{\square}(V_C)| = |Q_d^{\square}(V_C) - Q_d^{\square}(0)|.$$

The first-order MOST model used in many classical MOST textbooks neglects the increase in depletion charge with increasing source–substrate voltage (i.e., assuming $\Delta Q_d^{\square} \approx 0$). Here we will assume a linear increase of the depletion charge with increasing channel–substrate voltage (i.e., assuming a constant depletion *capacitance*). Thus (1) can be written as

$$V_T(V_C) = V_{T0} + \alpha V_C \quad (2)$$

with

$$\alpha = \left(1 + C_d^{\square}/C_{ox}\right)$$

and

$$C_d^{\square} = \Delta Q_d^{\square}(V_C)/V_C \approx \text{constant}.$$

This yields a much better approximation without adding too much computational complexity. In modern processes α is between 1.05 and 1.35.

Equation (2) yields the gate voltage at the onset of inversion as a function of the channel voltage. The inverse relation, i.e., the channel voltage at the onset of inversion as a function of the gate voltage, generally referred to as the channel-saturation voltage or pinch-off voltage $V_{C,sat}(V_G)$, may now be written

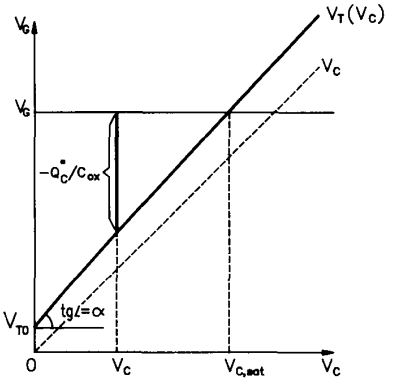

Fig. 2. The difference between the gate voltage V_G and the threshold voltage $V_T(V_C)$ (which is a function of the channel voltage V_C) represents the charge density in the channel divided by the oxide capacitance C_{ox}.

$$V_{C,sat}(V_G) = (V_G - V_{T0})/\alpha. \quad (3)$$

Conformably to the classical derivation of the MOST current–voltage relation [10], the inversion charge density is expressed as

$$Q_C^{\square}(V_G, V_C) = -(V_G - V_T(V_C))C_{ox}. \quad (4)$$

In Fig. 2 the above relations are represented in the following way. The horizontal axis shows channel voltages and the vertical axis gate voltages. In this graph the threshold voltage $V_T(V_C)$ is plotted as a function of the channel voltage V_C. The actual gate voltage is represented by a horizontal line, intersecting the y axis at V_G. The difference between the actual gate voltage V_G and the gate voltage at the onset of inversion $V_T(V_C)$ (threshold voltage) at some channel voltage V_C is indicated by a bracket. Apart from a factor $-C_{ox}$, this represents the inversion charge density $Q_C^{\square}$ at this point in the channel (see (4)). The channel saturates at the point where the inversion charge density just becomes zero. In the figure this is the crossing of the horizontal line and the $V_T(V_C)$ characteristic, indicated on the x axis by $V_{C,sat}$.

The current at an arbitrary location x in the channel is proportional to the local channel charge density $Q_C^{\square}$, the electron mobility μ, the local field along the channel dV_C/dx, and the channel width W:

$$I = -\mu W(V_G - V_T(V_C))C_{ox}dV_C/dx. \quad (5)$$

As the current is constant along the channel, integration from source to drain leads to the following equation:

$$IL = -\mu W C_{ox}\int_0^L (V_G - V_T(V_C))(dV_C/dx)\,dx. \quad (6)$$

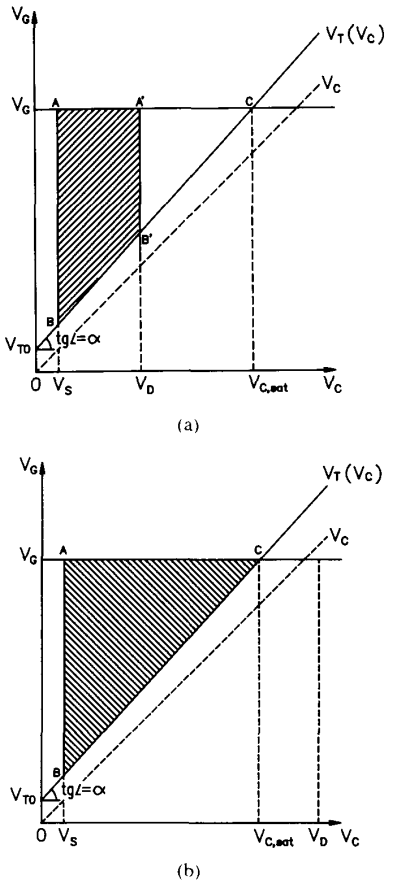

Fig. 3. The MOST current is proportional to the shaded area. For $V_D < V_{C,sat}$, the MOST operates in the linear region (a); for $V_D > V_{C,sat}$, the MOST is saturated (b). The proportionality constant $K = \mu C_{ox} W/L$. $I_D = K$. ▨

The expression for the drain current $I_D(=-I)$ now becomes

$$I_D = \mu C_{ox}(W/L)\int_{V_S}^{V_D}(V_G - V_T(V_C))\,dV_C. \tag{7}$$

Fig. 3 shows the graphical representation of this expression. Again the actual gate voltage V_G and the $V_T(V_C)$ characteristic are plotted. The values of the source and drain voltages V_S and V_D are indicated along the x axis. Hence, the shaded area equals the integral of $(V_G - V_T(V_C))$ from V_S to V_D. So, apart from the factor $\mu C_{ox} W/L$, the shaded area equals the total amount of drain current. In the linear region ($V_D < V_{C,sat}$), the shaded area is trapezoidal (Fig. 3(a)), whereas in the saturated region ($V_D > V_{C,sat}$), $V_{C,sat}$ should be taken as the upper bound and the shaded area becomes triangular (Fig. 3(b)).

By substituting (2) into (7) we can evaluate the drain current analytically as a function of the terminal voltages. In the linear region this leads to

$$I_D = K\{(V_G - V_{T0}) - (\alpha/2)(V_S + V_D)\}(V_D - V_S) \tag{8}$$

or

$$I_D = (K/2\alpha)\{(V_G - V_{T0} - \alpha V_S)^2 - (V_G - V_{T0} - \alpha V_D)^2\} \tag{9}$$

with

$$K = \mu C_{ox} W/L. \tag{10}$$

Expression (9) clearly shows the symmetry of the device between source and drain. The drain current is written as a difference of two quadratic expressions. Graphically, this is represented as a difference of the areas of two triangles, respectively ABC and $A'B'C$ in Fig. 3(a). For $V_D > V_{C,sat}(V_G)$ the channel pinches off at a channel voltage $V_{C,sat}(V_G)$ and with substitution of (3) into (9), the latter expression reduces to

$$I_{D,sat} = (K/2\alpha)(V_G - V_{T0} - \alpha V_S)^2. \tag{11}$$

Graphically the area of the triangle $A'B'C$ reduces to zero and only one triangle remains (ABC in Fig. 3(b)). If we substitute $\alpha = 1$ into (8) and (11), the expressions reduce to the classical first-order MOST model [10].

III. Merits and Shortcomings of the Model

The graphical representation comprises the dependence of the drain current on all terminal voltages. The effect of a change in one of the terminal voltages is clearly visualized.

The symmetry of the device between source and drain is also strikingly clear. It is easy to see that interchanging source and drain terminals has no effect on its behavior (but we have to keep in mind how we defined the drain current; if source and drain are interchanged, the trapezoidal surface represents the *negative* value of the drain current!).

As the body effect is included we can study its influence on the behavior of our circuits. Note that, without linearizing the $V_T(V_C)$ characteristic as is done in (2), the same graphical representation may be used. Analytically, this would lead to very complicated expressions. Using the graphical representation we are also able to gain insight into the effects of the *nonlinearity* of the $V_T(V_C)$ characteristic.

It is also easy to see when the transistor becomes saturated. However, the dependence of the drain current in saturation on the drain voltage cannot be modeled in this way. So no channel-shortening, static feedback, or other drain-dependent effects on the saturated drain current are included.

As the surface in the graphical representation has to be multiplied by the current factor K (equation (10)) to obtain the actual drain current, the voltage dependence of the K factor is also not included in the model. This means that the effects of mobility reduction cannot be studied in this way.

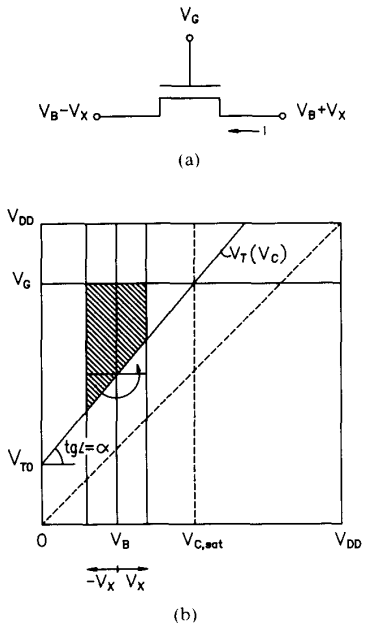

Fig. 4. (a) An MOS transistor used as a linear conductance [1]. Linearity is obtained by forcing the common voltage (V_B) of the source and drain terminals to be constant (signal independent). (b) Graphical representation of the voltage–current relationships in the circuit in (a). The signal current is represented by the shaded area.

IV. Examples of the Use of the Graphical Representation

In this section we will show how the graphical representation can be used to gain insight into the operation of MOS circuits. First several linearization techniques will be explained, both in the linear region (the MOSFET-C filters), and in the saturated region (the square-law circuits). From the latter class of circuits we will also deal with the functioning of a nonlinear circuit, a multiplier.

A. MOSFET-C Filters

Tsividis *et al.* [1], [3] have replaced the resistors in active *RC* filters by MOS transistors operating in the linear mode. Several linearization techniques are reported. In [1], eight different ways of linearization are shown. Six of them will be illustrated here. For a description of the basic circuits and their filter applications, we refer to the above-mentioned works.

Consider the MOST resistor in Fig. 4(a) (fig. 6(a) in [1]). The resistance value of such a transistor is controlled electronically via the gate voltage V_G. A signal V_x is applied to the drain terminal and $-V_x$ to the source terminal. The signal voltages are referred to a common bias voltage V_B. The graphical representation is shown in Fig. 4(b). Both the horizontal and the vertical axis show voltages within the circuit ranging from zero to V_{DD}. The line with slope 1 may be used to convert voltages of the source and drain terminals on the horizontal axis to gate voltages along the vertical axis and vice versa. The line with slope α and intersecting the vertical axis at V_{T0} is the $V_T(V_C)$ characteristic. The vertical line intersecting the horizontal axis at V_B represents the level at which the transistor is biased, whereas the horizontal line intersecting the vertical axis at V_G represents the gate voltage. The shaded area represents the current flowing in the device. As can easily be seen, this area equals $2V_x[V_G - V_T(V_B)]$ and the equivalent conductance becomes

$$G_C = K(V_G - V_T(V_B)) = K(V_G - V_{T0} - \alpha V_B). \quad (12)$$

Under the applied signal conditions, the device is clearly linear, as the conductance is signal independent. This can also be understood by realizing that the small triangle at the left of V_B just fits in the triangle at the right of V_B, yielding a rectangle with a height of $[V_G - V_T(V_B)]$ and a width of $2V_x$. The graphical representation of the voltages and currents in the way shown in Fig. 4(b) not only clarifies the linearization technique but also yields insight into the mutual relations of the voltages present in the circuit. It shows that, for a large voltage swing capability, V_G has to be chosen high, almost at V_{DD} (but a little headroom is needed for tuning). It also shows that the bias voltage V_B can best be chosen at $0.5*V_{C,sat}$ and that the maximum signal amplitude equals V_B. Note that for $V_x < 0$ the current changes sign and the shaded area represents the negative drain current. This does not change any of the above conclusions. It demonstrates the symmetry of the MOST for source and drain electrodes.

A more practical solution for a linear MOST conductance is the cancellation of nonlinearities by a fully balanced differential approach, as represented in Fig. 5(a) (fig. 6(b) in [1]). Two arbitrary signal voltages V_x and V_y are applied to the source and the drain terminals of an MOS transistor. An equally designed MOS transistor with an equal gate voltage is supplied with voltages $-V_x$ and $-V_y$. The difference in the currents $(I - I')$ is supposed to be linear with $(V_y - V_x)$ [1]. This is visualized in Fig. 5(b). Again a bias voltage V_B is chosen. The signal voltages V_x and V_y are referred to V_B. As in the above examples the drain currents are proportional to the shaded area in the figure. We have to realize, however, that the source and drain voltages of the lower transistor are interchanged, which means that the left shaded area is proportional to $-I'$. The current difference $(I - I')$ is thus represented by the *sum* of the shaded areas. The trapezoidal surface $A'B'C'D'$ just fits in the trapezoidal $ABCD$, if it is turned over 180° (as indicated by the arrow in Fig. 5(b)). The sum of the shaded areas now consists of two rectangles with height $(V_G - V_T(V_B))$ and width $(V_y - V_x)$ and equals $2(V_y - V_x)(V_G - V_T(V_B))$. As the height is constant, a linear (signal-independent) conductance according to (12) is obtained.

A third solution is shown in Fig. 6(a) (fig. 6(c) in [1], also used in [3]). In Fig. 6(b), the drain current I of the upper transistor is represented by the trapezoidal area $EFCD$, whereas the drain current I' of the lower transistor

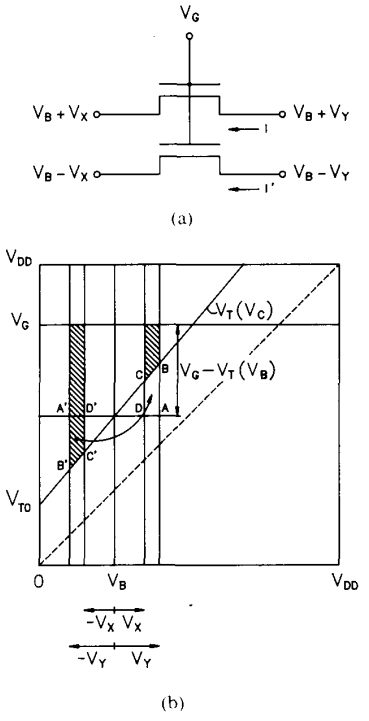

Fig. 5. (a) A balanced differential MOST conductance [1]. Linearity is obtained by forcing symmetrical (with respect to a bias voltage V_B) voltages to two equally designed MOS transistors. (b) Graphical representation of the currents in the circuit of (a). The sum of the shaded areas represents the signal current $(I - I')$.

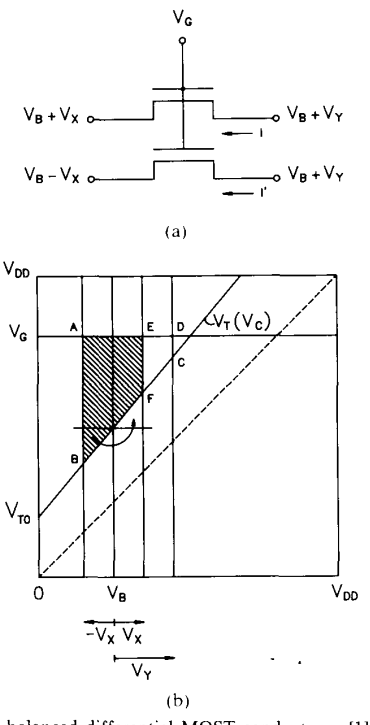

Fig. 6. (a) A balanced differential MOST conductance [1]. Linearity is obtained by forcing symmetrical (with respect to a certain bias voltage V_B) voltages to the sources of two equally designed MOS transistors. (b) Graphical representation of the currents in the circuit of (a). The shaded area represents the signal current $(I' - I)$.

is represented by the trapezoidal $ABCD$. The signal current is the difference $(I' - I)$ and is therefore represented by the shaded trapezoidal $ABFE$. Comparison with the results of Fig. 4 shows that (12) again holds and that we have obtained a linear conductance. We can also see that the current efficiency of the device (i.e., the ratio of the signal current to the total current flowing in the device) will be less than 1.0, except if V_y is chosen to be equal to zero.

The visualizations in Figs. 4(b), 5(b), and 6(b) show that all of the above-mentioned linearization techniques rely on the linearity of the $V_T(V_C)$ characteristic. Any nonlinearity in this curve will lead to distortion. The only way to circumvent this problem is to use two transistors with equal source and drain voltages, but with different gate voltages, as shown in Fig. 7(a). The graphical representation is shown in Fig. 7(b). The drain current I of the upper transistor is represented by trapezoidal $ABCD$, whereas drain current I' of the lower transistor is indicated by trapezoidal $EBCF$. Thus the signal current $(I - I')$ is represented by the (shaded) pure rectangle $AEFD$, with height $(V_{G1} - V_{G2})$ and width $(V_y - V_x)$. Hence the conductance may be written

$$G_C = K(V_{G1} - V_{G2}). \tag{13}$$

A balanced version of this linear conductor is also presented in [1] and [4].

In the examples shown so far our model predicts a linear conductance, as would also have been predicted by a simpler model, disregarding the body effect ($\alpha = 1$). The next two examples show nonlinearity, which would not have been discovered using the model with $\alpha = 1$.

In the circuit of Fig. 8(a) (fig. 6(d) in [1]) the signal dependence of the threshold voltage is (partly) compensated by a signal-dependent shift in the gate voltage. The shaded area represents the signal current in the circuit. The width of the trapezoidal area is the signal voltage $(V_y - V_x)$. In order to obtain a linear conductance, the average height of the trapezoidal ($|BA'|$ in Fig. 8(b)) should be signal independent. As is shown in Fig. 8(b), the voltage difference $|BA|$ equals V_{GC} and is signal independent. Due to the body effect, however, $|A'A|$ is not signal independent (but equals $(\alpha - 1)(V_x + V_y)/2)$) and hence $|BA'|$ is not signal independent, giving rise to distortion. If a model was used with $\alpha = 1$, this would not have been discovered.

Fig. 9(a) shows a circuit, which was presented in [9] (also fig. 6(f) in [1]), using depletion transistors. The signal current is the sum of the shaded areas $ABCD$ and $FBCE$ in Fig. 9(b). A rectangle can be obtained by turning trapezoid $ABCD$ over 180° in the plane of the paper along the middle of BC in such a way that it fits trapezoid $A'CBD'$. The width of the rectangle $FD'A'E$ thus obtained equals the signal voltage V_x, whereas the height of the rectangle is equal to the sum of $|FB|$ and $|DC|$. From Fig. 9(b) we can see that $|FB|$ is equal to $(V_C - V_{T0})$ and $|DC|$

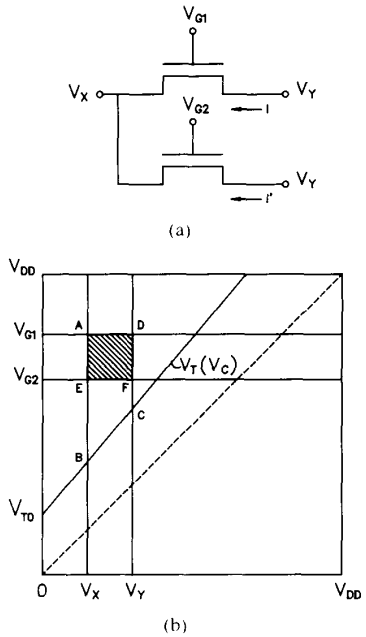

Fig. 7. (a) A linear MOST conductance [1]. Linearity is obtained by canceling the nonlinearity of one transistor with the nonlinearity of a second transistor with equal source and drain voltage but different gate voltage. (b) Graphical representation of the currents in the circuit of (a). The signal current ($I - I'$) is represented by the shaded area.

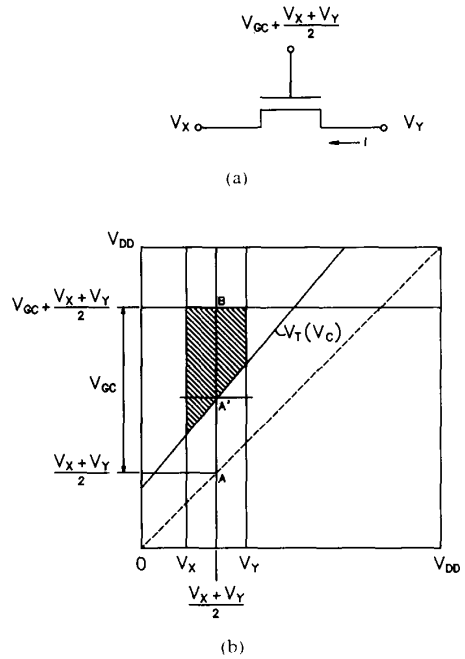

Fig. 8. (a) A MOST as linear conductance [1]. Nonlinearity is partly canceled by shifting the gate voltage with the mean of the terminal voltages at the source and drain. (b) The signal current I is represented by the shaded area.

equals ($V_x - V_{T0} - \alpha V_x$). Hence, if $\alpha \neq 1$ the height of the rectangle is not signal independent and thus distortion is introduced. Reference [9] shows that this cause of distortion can be canceled by choosing an appropriate ratio between the geometries of the transistors.

In the above examples only NMOS transistors were used. Fig. 10 shows that the graphical representation applies equally well to PMOS transistors or to a combination of P- and NMOS transistors. In the circuit of Fig. 10(a) (fig. 6(g) in [1]) the nonlinearity introduced by the NMOS transistors is (partly) canceled by the nonlinearity of the PMOST. Fig. 10(b) shows the graphical representation. For the PMOST another threshold voltage curve is plotted, $V_{Tp}(V_C)$, and the gate voltage of the PMOST is V_{Gp}. The lower trapezoidal represents the drain current of the PMOST whereas the upper trapezoidal represents the drain current of the NMOST. The sum of these (shaded) areas represents the signal current. If the slope of the $V_{Tp}(V_C)$ curve, α_p, is equal to the slope of the $V_{Tn}(V_C)$, α_n, and the K factors of both transistor are designed equal (by taking a different W/L ratio), then we can see that both trapezoidals can be shifted in the vertical direction to form a rectangle with constant (i.e., signal-independent) height. If, however, $\alpha_p \neq \alpha_n$ then different K values have to be chosen for the NMOST and the PMOST to cancel the remaining distortion. As in the previous example, nonlinearity effects arising from the body effect have to be canceled by choosing a difference in the geometries of the transistors. Because the geometry ratios of transistors are based on process parameters, the success of the linearize-

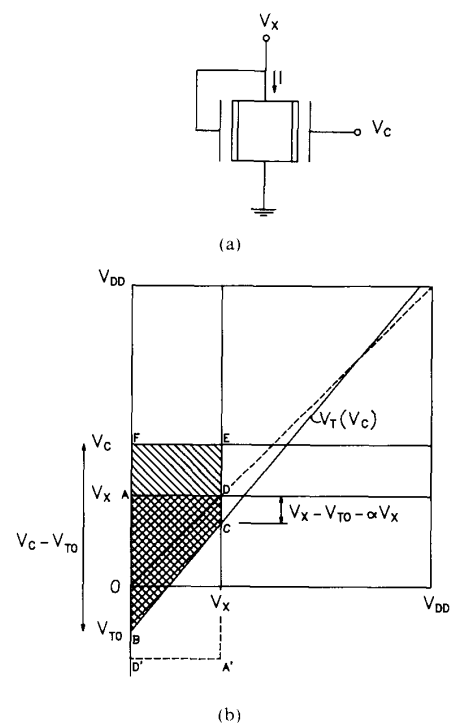

Fig. 9. (a) A linear MOST conductance with depletion transistors [15]. Nonlinearity is (partly) canceled by a signal-dependent gate voltage of one of the transistors. (b) Graphical representation of the currents in the circuit of (a). The signal current I is represented by the sum of the shaded areas $ABCD$ and $FBCE$.

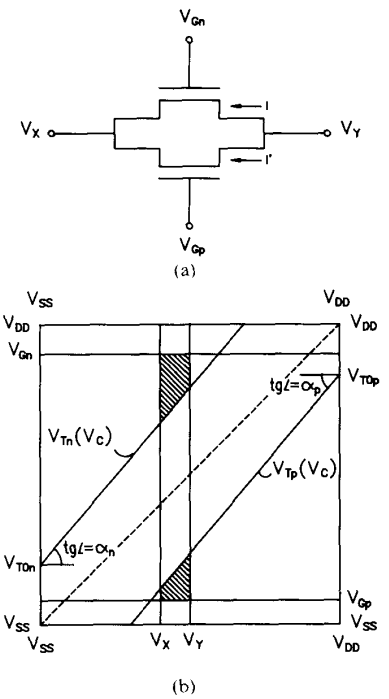

Fig. 10. (a) A linear conductance with an NMOST and a PMOST. The nonlinearity in the conductance of the NMOST is (partly) canceled by the nonlinearity of the PMOST. (b) Graphical representation of the currents in the circuit of (a). The signal current $(I + I')$ is represented by the sum of the shaded areas.

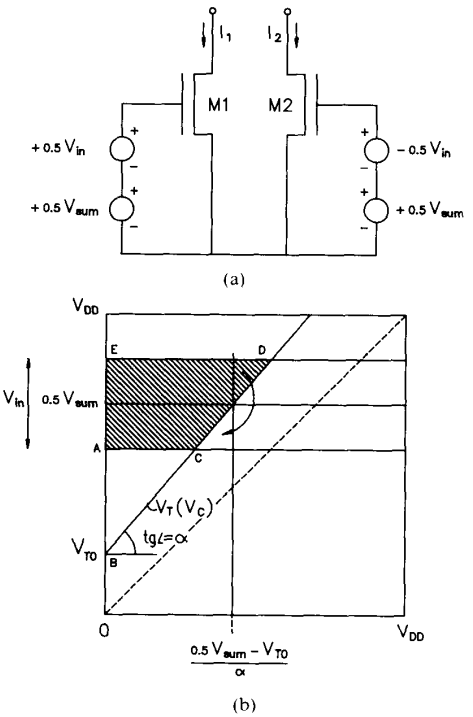

Fig. 11. (a) A linear transconductance with MOS transistors operating in the saturated region. Linearity is obtained by a purely differential operation. (b) Graphical representation of the currents of the circuit of (a). The signal current $(I_1 - I_2)$ is represented by the shaded area.

tion technique in the latter two examples suffers from dependence on process parameter variations.

B. MOST Square-Law Circuits

A different approach for analog signal processing is achieved by exploiting the square-law characteristic of a MOST in the saturated mode [2], [6]. For a MOST in saturation with source connected to substrate, the drain current of (11) reduces to

$$I_D = (K/2\alpha)(V_G - V_{T0})^2. \tag{14}$$

Two basic principles used in this class of circuits will be shown here. The first leads to linear voltage-to-current and current-to-voltage convertors and the second results in a four-quadrant multiplier.

Consider the circuit of Fig. 11(a), consisting of two identical MOS transistors $M1$ and $M2$. The gate voltages are, respectively, $(0.5 * V_{sum} + 0.5 * V_{in})$ and $(0.5 * V_{sum} - 0.5 * V_{in})$. Using (14), the following expression for the drain current difference can be derived [2], [6]:

$$I_1 - I_2 = (K/2\alpha)(V_{sum} - 2V_{T0})V_{in}. \tag{15}$$

Under the condition of a constant sum of gate voltages V_{sum}, the current difference is linearly proportional to the input voltage V_{in}. Based on this *two-transistor linear and squaring principle* [6] several linear $V-I$ and $I-V$ converters have been developed. A graphical representation of the currents in the $V-I$ converter of Fig. 11(a) is given in Fig. 11(b). As the transistors operate in the saturated mode we are now working with triangles. Triangle EBD represents the drain current I_1 of $M1$ and triangle ABC represents the drain current I_2 of $M2$. Thus the output current difference is proportional to the shaded area, the trapezoidal $ACDE$. It is easy to see that this is a linear function of V_{in}, as the shaded triangle (at point D) just fits in the triangle at point C, as indicated by the arrow, resulting in a rectangle with height V_{in} and a constant width of $(0.5 * V_{sum} - V_{T0})/\alpha$. Filter functions operating up to several 100 kHz and with a dynamic range in the order of 60 dB can be designed [5].

Besides linear $I-V$ and $V-I$ converters, nonlinear circuits such as analog multipliers, current squaring, and current divider circuits have also been developed in this class [2], [6]–[8]. The *four-transistor multiplying principle* [6] will be described using Fig. 12. Consider the circuit of Fig. 12(a). For practical implementations see [6] and [7]. The output current is defined as

$$I_{out} = I_1 - I_2 + I_3 - I_4. \tag{16}$$

By inspection of Fig. 12(a) and using (11), the drain

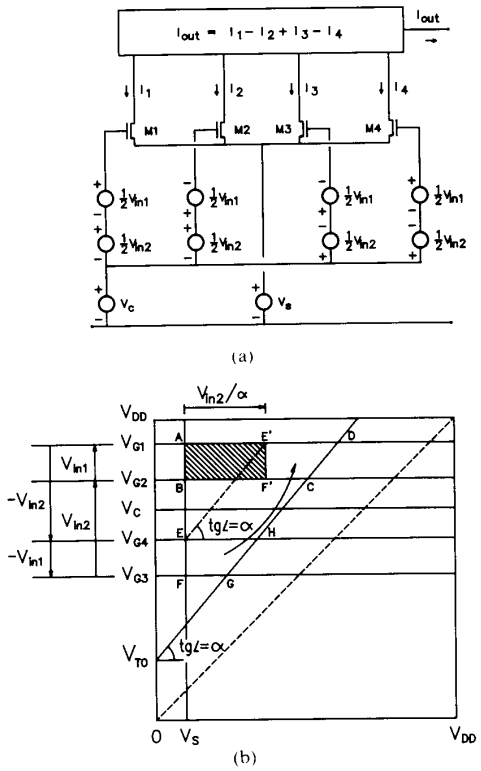

Fig. 12. (a) An NMOST four-quadrant multiplier, based on the quadratic dependence of the drain current on the gate voltage in the saturated region. (b) Graphical representation of the currents in the multiplier circuit of (a). The shaded area represents the signal current.

currents may be written:

$$I_1 = \frac{K}{2\alpha}\left(+\frac{1}{2}V_{in1} + \frac{1}{2}V_{in2} + V_C - \alpha V_S - V_{T0}\right)^2 \quad (17a)$$

$$I_2 = \frac{K}{2\alpha}\left(-\frac{1}{2}V_{in1} + \frac{1}{2}V_{in2} + V_C - \alpha V_S - V_{T0}\right)^2 \quad (17b)$$

$$I_3 = \frac{K}{2\alpha}\left(-\frac{1}{2}V_{in1} - \frac{1}{2}V_{in2} + V_C - \alpha V_S - V_{T0}\right)^2 \quad (17c)$$

$$I_4 = \frac{K}{2\alpha}\left(+\frac{1}{2}V_{in1} - \frac{1}{2}V_{in2} + V_C - \alpha V_S - V_{T0}\right)^2. \quad (17d)$$

Substitution of (17a)–(17d) into (16) yields

$$I_{out} = \frac{K}{\alpha}V_{in1}V_{in2}. \quad (18)$$

As both V_{in1} and V_{in2} may be positive as well as negative, we have obtained a four-quadrant voltage multiplier.

Though the above analysis is simple and straightforward, it does not provide much insight into the operation of the multiplier. Putting the voltage–current relations into graphics yields the result shown in Fig. 12(b). The current difference $(I_1 - I_2)$ is presented by the trapezoidal $ABCD$, whereas the current difference $(I_4 - I_3)$ is indicted by the trapezoidal $EFGH$. We can now find the output current according to (16) by shifting the trapezoidal $EFGH$ along the $V_T(V_C)$ curve as indicated by the arrow. The output current I_{out} is now proportional to the rectangle $ABF'E'$. This rectangle has a height equal to V_{in1} and a width equal to V_{in2}/α, thus yielding an output current according to (18).

V. Conclusions

A simple first-order MOST model has been described. In contrast to other models, this model includes the body effect. A graphical representation of the relations between the terminal voltages and the current flowing in the device is introduced. This representation is very attractive for gaining insight in the functioning of circuits depending on the characteristics of an MOS transistor. Several examples have been elaborated, including MOSFET-C filter circuits and CMOS square-law circuits.

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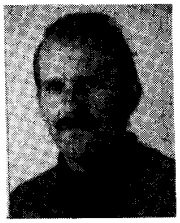

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