# A CMOS Analog Continuous-Time Delay Line with Adaptive Delay-Time Control

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*Abstract*—**A CMOS analog continuous-time delay line has been developed composed of cascaded first-order current-domain all-pass sections. Each all-pass section consists of CMOS transistors and a single capacitor. The operation is based on the square-law characteristic of an MOS transistor in saturation. The delay time per section can either be controlled by an external voltage or locked to an external reference frequency by means of a control system which features a large capture range. Experimental verification has been performed on two setups: an integrated cascade of 26 identical all-pass sections and a frequency locking system breadboard built around two identical on-chip all-pass sections.**

## I. Introduction

ANALOG delay lines are useful elements in signal processing circuits such as adaptive filters. Charge-coupled device and switched-capacitor solutions are well known [1]–[3]. A drawback of these discrete-time circuits is the necessity of clocking and the occurrence of aliasing effects. A continuous-time approach may be attractive, particularly if the delay per section can be controlled electronically.

However, due to the dependence of time constants of continuous-time circuits on temperature- and process-dependent values of monolithic components such as capacitors and transistors, some extra circuitry is required to control the delay time. In [4]–[7] several techniques have been described which lock the performance of a filter to an external reference frequency. A similar approach is used here.

A delay-line section has to fulfill two important properties. First, the modulus of the transfer function has to equal unity over a broad frequency range, and second, the phase shift has to depend linearly on frequency in order to provide a frequency-independent group delay. A first-order all-pass filter with a transfer function

$$H(j\omega) = \frac{1 - j\omega RC}{1 + j\omega RC} \tag{1}$$

satisfies the first condition, while the second condition is approximately true. The argument of $H(j\omega)$ is

$$\arg(H(j\omega)) = -2\arctan(\omega RC) \tag{2}$$

and the associated group delay is

$$D(\omega) = \frac{2RC}{1 + (\omega RC)^2}. \tag{3}$$

For

$$(\omega RC)^2 \ll 1 \tag{4}$$

the group delay is approximately constant. Hence, for band-limited signals a first-order all-pass filter may perform as a delay section. By cascading two or more first-order all-pass sections, with taps at the output of every stage, a tapped delay line is obtained.

The incorporation of frequency locking techniques requires that the $RC$ products of the filter sections have to be adjustable. Recently a class of analog CMOS circuits has been presented based on the square-law characteristic of an MOS transistor in saturation [8]. This class comprises, among others, voltage-controlled linear $V$–$I$ and linear $I$–$V$ convertors, which lend themselves very well to realizing the desired time constants. In Section II it is shown how a voltage-controlled all-pass filter may be constructed using these circuits. Section III describes the delay line, and Section IV explains the time-delay control system. In Section V an analysis is given of errors that can occur in the performance of the all-pass filter and the control system. Section VI presents experimental results and Section VII finishes the paper with some conclusions.

## II. A First-Order All-Pass Section

Writing the all-pass transfer function (1) as

$$H(j\omega) = 2\frac{1}{1 + j\omega RC} - 1 \tag{5}$$

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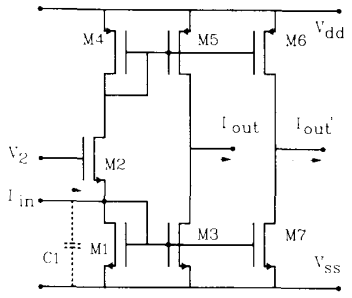

Fig. 1. The current invertor.

the all-pass function is split into two basic functions. The first term in (5) is a low-pass filter transfer function with a dc gain of two, and the second part represents a simple invertor. An analog CMOS current invertor circuit, which can provide both functions, has been described in [8] and is shown in Fig. 1. All transistors operate in the saturated region and the working of the circuit is based on the MOST square-law characteristic. The circuit features a linear input resistance

$$R = \frac{1}{2K(V_2 - 2V_t)} \tag{6}$$

and furnishes an output current

$$I_{\text{out}} = I'_{\text{out}} = -I_{\text{in}}. \tag{7}$$

Provided that

$$|I_{\text{in}}| = K(V_2 - 2V_t)^2 \tag{8}$$

the circuit can handle positive as well as negative input currents.

With a capacitor connected between input and ground, as indicated by the dotted lines in Fig. 1, the current invertor is modified into a current domain low-pass filter with transfer function

$$H(j\omega) = \frac{-1}{1 + j\omega RC} \tag{9}$$

where $R$ is given by (6). Note that $R$, and also by means of $R$, the group delay $D(\omega)$ in (3) may be electronically controlled via $V_2$. A low-frequency gain of two may be obtained by adding the currents of the two output stages of Fig. 1. The all-pass filter function (5) can now be obtained by combination of a current invertor and a low-pass filter section in the way as shown in Fig. 2.

The first current invertor has three outputs. The first output ($M3$ and $M5$) provides an auxiliary output current $I_{\text{out1}}$ (tap output). The second output ($M6$ and $M7$) contributes directly to the output current of the all-pass filter ($I_{\text{out3}}$) and realizes the second term in (5). The third output ($M8$ and $M9$) is connected to the input of the second current invertor. This second current invertor has a low-pass transfer function by action of the capacitor connected between input and ground. The double output branch of the second current invertor ($M15$–$M18$) is connected to the output of the all-pass filter and provides the invertor with a gain of two. This realizes the first term in (5). Transistors $M12$ and $M14$ serve as an auxiliary output ($I_{\text{out2}}$). All MOS transistors have identical geometry.

## III. The Delay Line

By cascading several all-pass sections, as given in Fig. 2, a delay line is obtained. The auxiliary output of the first current invertor ($I_{\text{out1},k}$) of each of the all-pass sections is used as a tap. The transfer function $H_k(j\omega)$ from the input current of the first stage to the output current $I_{\text{out1},k}$ of stage $k$ is given by

$$H_k(j\omega) = -\left(\frac{1 - j\omega RC}{1 + j\omega RC}\right)^{k-1}, \qquad k = 1,2,\cdots,n. \tag{10}$$

For band-limited signals, satisfying condition (4), the delay time $t_{d,k}$ from input to the $k$th tap may be approximated by

$$t_{d,k} = 2(k-1)RC. \tag{11}$$

The transfer function $H'_k(j\omega)$ from the input current to the auxiliary current output $I_{\text{out2},k}$ is

$$H'_k(j\omega) = \frac{1}{1 + j\omega RC}\left(\frac{1 - j\omega RC}{1 + j\omega RC}\right)^{k-1}, \qquad k = 1,2,\cdots,n. \tag{12}$$

The transfer functions described by (12) are Laplace transforms of Laguerre functions, which may be used advantageously in adaptive transversal filters [9]. As the relation between input current and input voltage of each stage is linear, both types of transfer functions are also available in the voltage domain at the gate of transistor $M1$ and the gate of transistor $M11$ of the $k$th stage.

## IV. The Delay-Time Control System

Adaptive tuning of the delay time is possible by using the $V_2$ terminal. We will use an indirect tuning scheme [7] with one all-pass section as a reference filter as shown in Fig. 3. The functioning of this scheme is as follows. A reference signal with amplitude $A$ and an accurately determined frequency $\omega_{\text{ref}}$ is fed into the input of the all-pass section and the input of a multiplier. The all-pass section will produce an output signal $V_{\text{out}}$ of the same amplitude but with a phase shift given by (2):

$$V_{\text{out}} = A\sin(\omega_{\text{ref}}t + p) \tag{13}$$

with

$$p = -2\arctan\left(\frac{\omega_{\text{ref}}C}{2K(V_2 - 2V_t)}\right). \tag{14}$$

The output signal of the all-pass section is fed to the same multiplier as the input reference signal. The multiplier

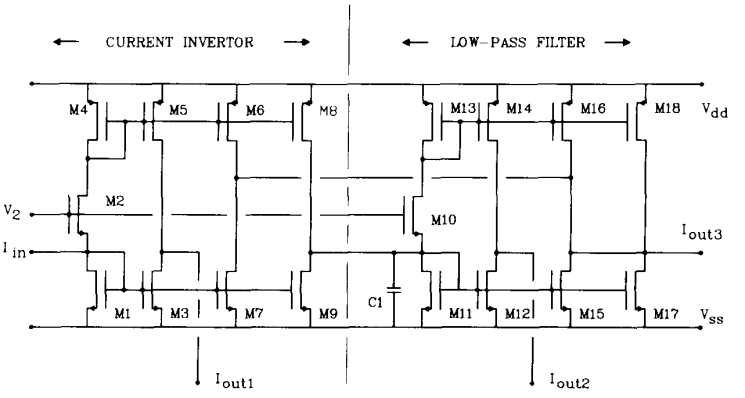


Fig. 2. The first-order all-pass circuit.

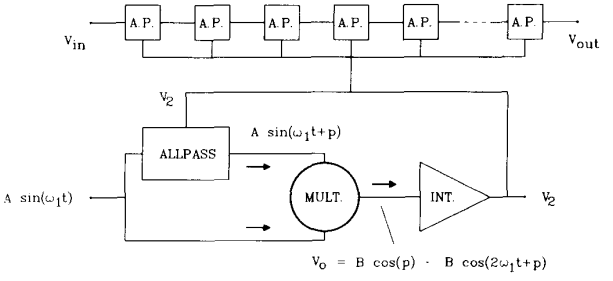


Fig. 3. Time-delay control system.

produces an output signal $V_o$ containing two components:

$$V_o = B\cos(p) - B\cos(2\omega_{\text{ref}}t + p) \tag{15}$$

in which $B$ is determined by the amplitude of the input signal $A$ and the multiplying constant of the multiplier. The multiplier is then followed by an integrator with a large time constant with respect to the reciprocal of the reference frequency. The second term in (15) is filtered out and will be neglected in this discussion. What remains is the first term in (15), a dc component. If the multiplier is connected correctly with respect to the sign of the inputs, the integrator will change its output signal $V_2$ in such a way that the dc component of (15) vanishes. In this situation the phase shift $p$ of the all-pass filter is exactly 90° and the pole-zero frequency of the all-pass section is tuned to the reference input frequency.

The behavior of the system may be studied by finding an expression for the voltage $V_o$ at the output of the multiplier as a function of the control voltage $V_2$. Substituting (14) into (15) and neglecting the second term in (15) we obtain

$$V_o = B\cos\left(2\arctan\left(\frac{V_2^* - 2V_t}{V_2 - 2V_t}\right)\right) \tag{16}$$

with

$$V_2^* = 2V_t + \frac{\omega_{\text{ref}}C}{2K} \tag{17}$$

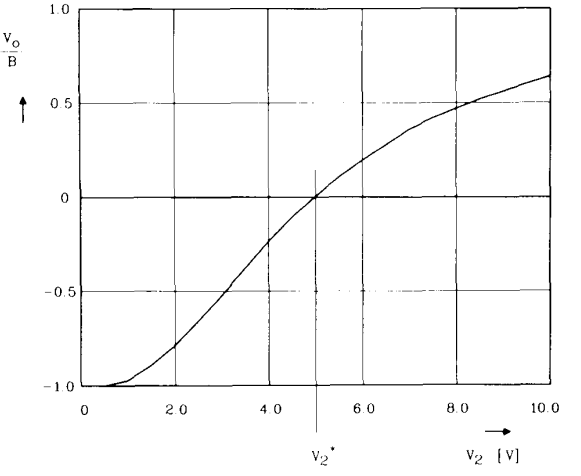


Fig. 4. The error voltage at the output of the multiplier as a function of $V_2$.

the voltage $V_2$ for which the all-pass filter generates a phase shift of 90° for a given reference frequency. The voltage $V_0$ is plotted in Fig. 4 as a function of $V_2$ according to (16) for $V_2^* = 5.0$ V. This curve shows that in principle the system will always lock to the reference frequency irrespective of the initial value of $V_2$ and the value of the reference frequency. In practice, however, $\omega_{\text{ref}}$ has to be within a range, determined at the lower side by the deterioration of the circuit behavior due to weak inversion [8] and at the upper side by the supply voltage. Nevertheless the capture range of the system should be very large.

## V. Error Analysis

### A. The All-Pass Section

The all-pass transfer function (1) is realized by adding the output signal of a low-pass filter with a low-frequency gain of two and the output signal of a current invertor, as described by (5). Transistor mismatch and channel-length shortening may lead to deviations of the low-frequency

TABLE I
MEASURED RESULTS FOR 26TH-ORDER ALL-PASS FILTER

| | | | | | | |
|---|---|---|---|---|---|---|
| Supply Voltage | V | 8.0 | 8.0 | 8.0 | 8.0 | 8.0 |
| Bias Current Ib | μA | 80 | 40 | 20 | 10 | 5 |
| Bias Voltage V2 | V | 7.18 | 5.31 | 4.08 | 3.26 | 2.69 |
| Total Supply Current | mA | 13.3 | 6.66 | 3.32 | 1.67 | 0.85 |
| Group Delay | μS | 8.1 | 10.6 | 14.3 | 19.6 | 27.9 |
| DC-gain | dB | -2.9 | -2.4 | -3.0 | -1.5 | +0.8 |
| Ripple | dB | 3.7 | 4.7 | 5.0 | 4.5 | 3.0 |
| RMS Noise volt. (100Hz...300KHz) | mV | 0.115 | 0.099 | 0.082 | 0.079 | - |
| RMS Max. inp. volt. (THD=1%) | mV | 360 | 300 | 170 | 97 | 79 |

gains of these circuits and hence of the desired transfer function. We can analyze the effect of mismatch on the transfer function by assuming the low-frequency gain of the low-pass filter to be $2+\Delta_{Ip}$ and the low-frequency gain of the current invertor $-(1+\Delta_{ci})$, with $\Delta_{Ip}$ and $\Delta_{ci}$ being the deviations of the low-frequency gains. The transfer-function (1) is now written as

$$H(j\omega)=\frac{(1+\Delta_{Ip}-\Delta_{ci})-j\omega(1+\Delta_{ci})RC}{(1+j\omega RC)}. \quad (18)$$

As we can see, the pole frequency is not influenced. The zero frequency, however, is shifted, which means that the amplitude of the transfer function is not equal for all frequencies anymore. The low-frequency gain becomes

$$|H(0)|=(1+\Delta_{Ip}-\Delta_{ci}) \quad (19)$$

whereas the high-frequency gain is

$$|H(\infty)|=(1+\Delta_{ci}). \quad (20)$$

For use in a delay line we can tolerate only a small deviation from unity. If we allow the modulus of the transfer function of the delay line to be in the range

$$0.5<|H_k(j\omega)|<2.0, \quad (21)$$

and $k=26$, we obtain the following restrictions for $\Delta_{Ip}$ and $\Delta_{ci}$:

$$\max(|\Delta_{Ip}-\Delta_{ci}|,|\Delta_{ci}|)<0.027. \quad (22)$$

This means that, in our situation, a deviation of the low-frequency gains of the current invertor and the low-pass filter of 2.7 percent may be tolerated.

### B. The Delay-Time Control System

Mismatch, offsets, and other nonidealities in the subcircuits of the control system (Fig. 3) may lead to a deviation of the effective pole-zero frequency $\omega_{\text{eff}}$, from the desired frequency set by the reference frequency $\omega_{\text{ref}}$. It can be shown that

$$\left|\frac{\omega_{\text{eff}}-\omega_{\text{ref}}}{\omega_{\text{ref}}}\right|=\left|\frac{V_{zo}+CV_{xo}V_{yo}+V_{io}+V_2/A_0}{V_{\text{in}\,int}}\right| \quad (23)$$

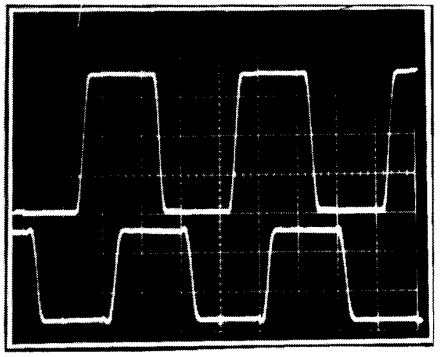

Fig. 5. Step response (lower trace) of the 26-stage delay line. The circuit is biased at $V_2=7.18$ V. The input signal (upper trace) has a magnitude of 0.4 V with a leading and a trailing edge time of 2.0 μs. The horizontal scale is 10 μs per division. The output load resistance was 360 Ω.

where

$V_{zo}$ multiplier output offset voltage,
$V_{xo}$ multiplier $x$-input offset voltage,
$V_{yo}$ multiplier $y$-input offset voltage,
$C$ multiplier constant,
$V_{io}$ integrator input offset voltage,
$A_0$ integrator low-frequency gain, and
$V_{\text{in}\,int}$ signal amplitude at the input of the integrator.

As usually both input offset voltages are small, the product of both voltages is small with respect to the output offset voltage and may be neglected. Important is a low multiplier output offset voltage, a low integrator input offset voltage, a high integrator low-frequency gain, and a high signal level at the input of the integrator. For this reason an XOR circuit with two comparators is sometimes used instead of a multiplier (see also Fig. 12). In this situation (23) still holds with

$$V_{zo}=(V_{dd}-V_{ss})/2-V_{GND} \quad (24)$$

and

$$V_{\text{in}\,int}=(V_{dd}-V_{ss}).$$

In this case special arrangements can be made to minimize $V_{zo}$, as will be explained in Section VI.

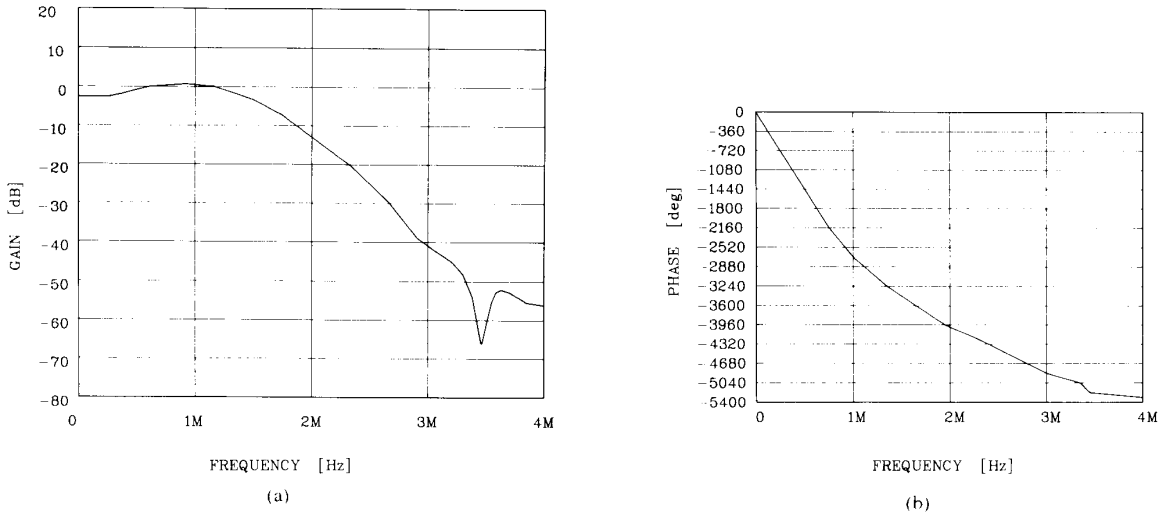


Fig. 6. (a), (b) Transfer function of the total filter biased with $V_2 = 7.18$ V; the dc current is 80 $\mu$A in each branch, 480 $\mu$A in each section, and 13.3 mA in the total filter.

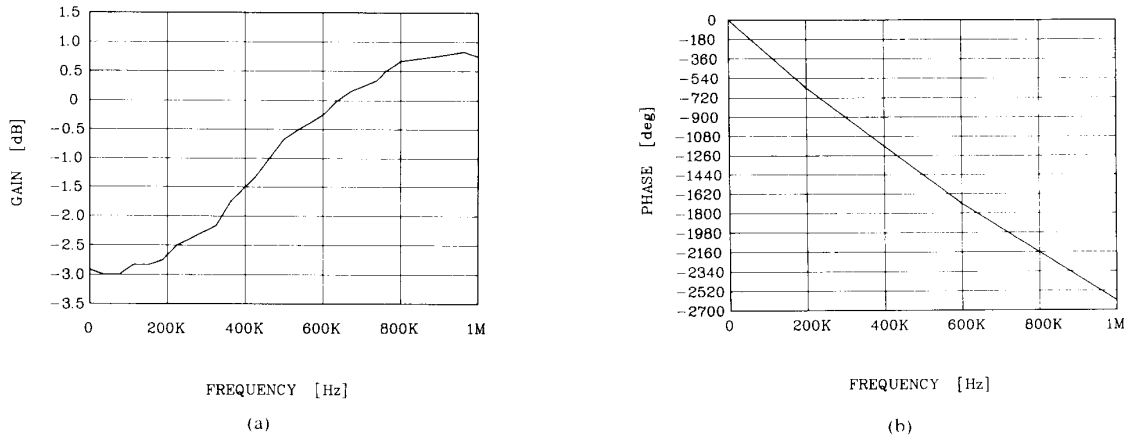


Fig. 7. (a), (b) Transfer function of the total filter biased at $V_2 = 7.18$ V.

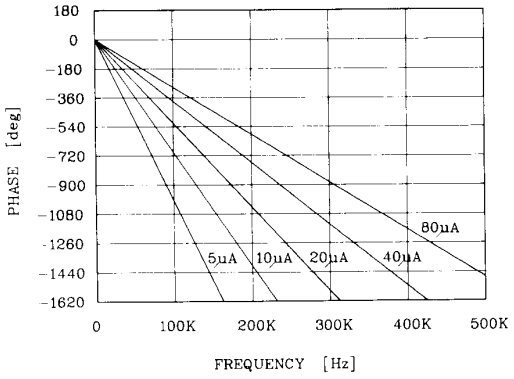


Fig. 8. Phase shift of the total filter as a function of frequency at several bias currents.

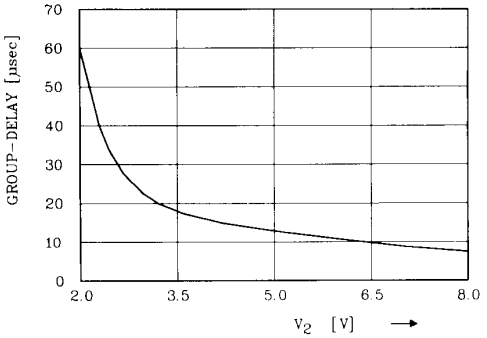


Fig. 9. Group delay as a function of the bias voltage $V_2$.

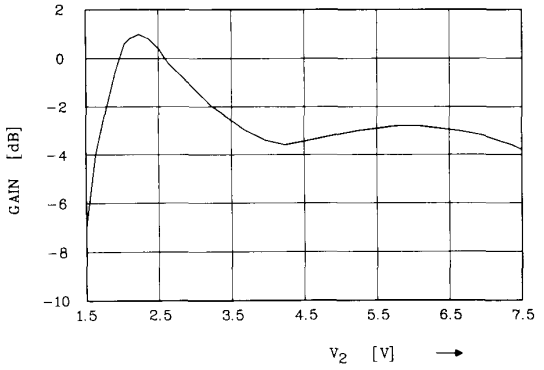


Fig. 10. Low-frequency gain (1 kHz) as a function of the bias voltage $V_2$.

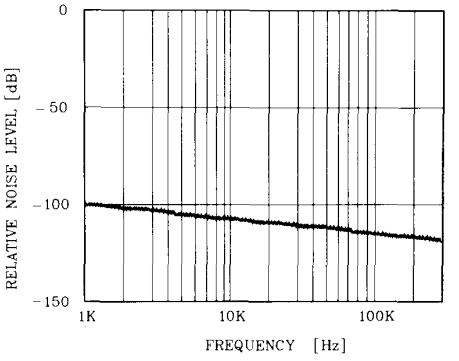


Fig. 11. The relative output noise level at $V_2 = 7.18$ V. The reference level in this measurement is the signal level at which a THD of 1 percent is measured.

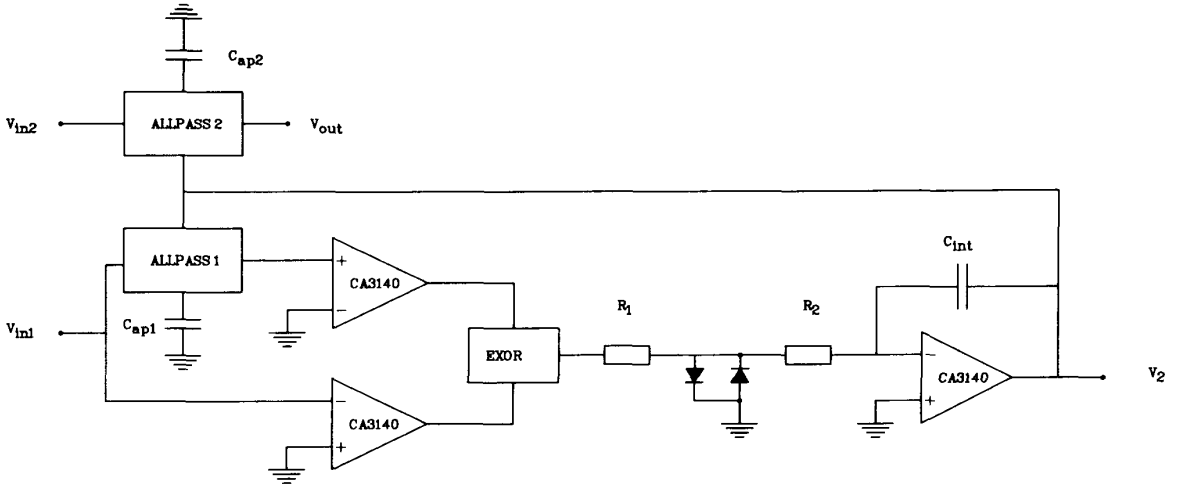


Fig. 12. Breadboard realization of the control system. Both all-pass sections are on the same chip.

## VI. Results of Measurements

Experimental verification has been performed on two setups: an integrated cascade of 26 identical all-pass sections, acting as a continuous-time delay line, and a frequency locking system breadboard built on breadboard around two identical on-chip all-pass sections. Both the delay-line and the two separate all-pass sections have been realized in the retrograde twin-well CMOS process of the University of Twente. Although all circuit schemes show NMOS transistors in the core of the circuits (transistors $M1-M3$ and $M7$ in Fig. 1), PMOS transistors were used to be able to reduce the body effect by connecting the source of each transistor to its own substrate well. The PMOST threshold voltage is $-0.6$ V. All transistors (in all circuits) have the same geometry: $W = 40$ $\mu$m and $L = 20$ $\mu$m.

Table I shows the measurement conditions for the 26th-order all-pass filter for five different bias currents. Fig. 5 shows the step response of the filter biased at $V_2 = 7.18$ V. At this bias voltage the bias current in each branch is 80 $\mu$A, in each section 480 $\mu$A, and in the complete filter 13.3 mA. The delay time is 8.1 $\mu$s.

For the same bias condition ($V_2 = 7.18$ V) the transfer function of the complete filter is measured. The results are shown in Fig. 6. Fig. 7 shows the same results for a smaller frequency span.

Fig. 8 shows the phase shift of the complete filter as a function of frequency at several bias currents, whereas Fig. 9 shows the group delay as a function of the bias voltage.

Fig. 10 shows the low-frequency gain at 1 kHz of the total filter as a function of the bias voltage $V_2$.

The noise spectrum has been measured between 1 and 300 kHz; Fig. 11 shows the results. The reference level (0 dB) in this measurement is defined as the input level at which the total harmonic distortion (THD) of the total circuit (26 stages) equals 1 percent.

The measurements on the delay-time control system have been performed on a breadboard setup with the electrical scheme of Fig. 12. This is basically the setup of Fig. 3. The multiplier has been realized with CA3140 op amps, used as comparators and an XOR circuit. The output

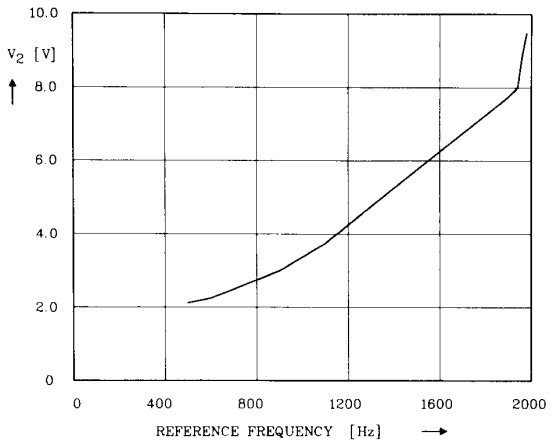


Fig. 13. Control voltage $V_2$ in the control loop as a function of the reference frequency with $C_{ap1} = 10$ nF.

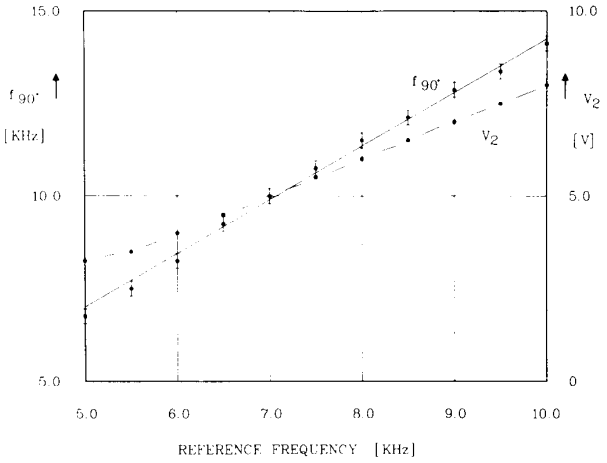


Fig. 14. The frequency at which the second all-pass filter has a phase shift of 90° as a function of the reference frequency. The control-loop voltage $V_2$ is also shown. In this measurement $C_{ap1} = 2.2$ nF and $C_{ap2} = 1.5$ nF.

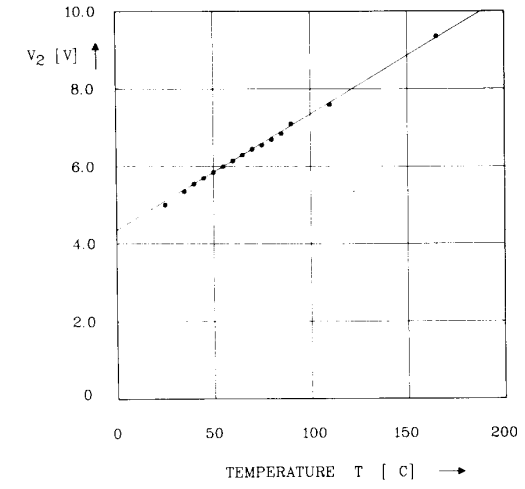


Fig. 15. The control-loop voltage $V_2$ as a function of temperature.

of the XOR circuit is connected via $R_1$ to two diodes to limit the voltage swing at the input of the integrator and to make the setup less susceptible to supply voltage variations. The integrator consists of $R_2$, $C_{int}$, and a CA3140 op amp. Both all-pass sections are on the same chip. ALLPASS1 is used in the loop as a reference filter whereas ALLPASS2 may be used for signal processing. The capacitors $C_{ap1}$ and $C_{ap2}$ are external capacitors. The supply voltage in this setup is 10 V whereas the ground level is 5.0 V. This setup functions very well. The system always locks to the reference frequency as long as $V_2^*$ (see (17)) is within certain limits: $2.1\ \text{V} < V_2^* < 8.0\ \text{V}$. The lower limit is in this case determined by the operation region of the integrator. The upper limit is set by the supply voltage.

The following measurements have been performed on the circuit of Fig. 12. The loop voltage $V_2$ has been measured as a function of the reference frequency. Fig. 13 shows the results measured with $C_{ap1} = 10$ nF. The scheme works properly for reference frequencies in the range 500–1950 Hz.

The performance of the ALLPASS2 filter (Fig. 12) has been determined in the following way. The frequency $f_{90}$ at which the ALLPASS2 filter exhibits a phase shift of 90° has been measured as a function of the reference frequency $f_{\text{ref}}$. The result is shown in Fig. 14. This measurement has been performed with $C_{ap1} = 2.2$ nF and $C_{ap2} = 1.5$ nF. The theoretical results are plotted as a solid line. The figure shows a close agreement between theory and measurements. In this figure the loop voltage $V_2$ is also plotted.

Finally the loop voltage $V_2$ has been measured as a function of temperature; the result is shown in Fig. 15. During this measurement no change could be observed in the transfer function of the ALLPASS2 filter.

## VII. Discussion

Fig. 6(a) shows an approximately flat (3.8-dB ripple) amplitude response of the 26 sections for frequencies up to 1.5 MHz. This amounts to 0.14-dB ripple per section in this frequency range. With respect to the phase linearity, however, the input signal frequency has to be limited to a smaller range. Equation (3) predicts a nonlinearity of 2 percent for signals with $\omega < 0.2/RC$ which amounts to 176 kHz for $V_2 = 7.18$ V. Fig. 7(a) shows in this range a ripple in the amplitude response of about 0.2 dB for 26 sections, or about 0.077-dB per section.

The feasibility of the all-pass section of Fig. 1 is shown by Figs. 5–14. However, a first-order all-pass filter may not be the best solution. Higher order all-pass filters, as for instance, second-order filters with maximally flat phase response, have to be considered. This may lead to a larger usable bandwidth. Also, a larger delay time may be obtained with a smaller number of transistors.

It has yet to be investigated whether it is necessary to connect the source of each transistor to its own substrate. Connecting the substrate of each device to the power supply would largely reduce the parasitic capacitance on these nodes and the usable bandwidth would be much

larger. Furthermore, NMOS transistors could be used in the core which also enhances the speed of the circuits.

The monotonously rising curve of the error voltage at the output of the multiplier as a function of $V_2$ (Fig. 4) gives the delay-time control system a very large capture range of about two octaves in frequency. This is due to the use of an all-pass filter as a reference filter. Other types of reference filters such as low pass, high pass, or bandpass will always show a decline of the error voltage as a result of the decreasing amplitude of the filter response towards the lower and/or higher frequencies. Consequently the application of such types of reference filters leads to capture ranges of 10–20 percent of the center frequency.

The deviation of $V_2$ from the straight line in Fig. 13, as predicted by the simple relation of (17), is probably due to carrier mobility reduction, which necessitates a higher gate voltage to obtain a certain value of the transconductance than the simple square-law would predict.

The temperature measurements shown in Fig. 15 have to be considered with ample wariness as the determination of the temperature could not be performed with great accuracy. However, it shows the range in which the system performs well and moreover, as no noticable difference could be observed in the behavior of the second all-pass filter (ALLPASS2), it shows the feasibility of the system.

## VIII. Conclusion

A CMOS analog continuous-time delay line has been developed composed of cascaded current domain all-pass sections. The operation is based on the square-law behavior of an MOS transistor in the saturated region. An adaptive delay-time control system makes the delay time independent of processing and temperature variations. Measurements have been performed on an on-chip realization of the delay line of 26 stages and on a breadboard of the control system built around two all-pass sections on the same chip. The measurements show good results: a large capture range and good tracking of the reference frequency make the delay time very well controllable. We have demonstrated that it is possible to build an analog continuous-time delay line on the basis of analog CMOS circuits, using the square-law characteristic of an MOS transistor in saturation.

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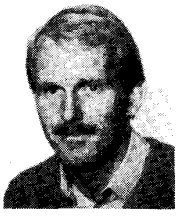

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