ANALOG CMOS COMPUTATIONAL CIRCUITS.

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ABSTRACT

A new CMOS three transistor current squaring circuit is proposed. The versatility of the circuit is shown in three applications: an eight transistor four-quadrant current multiplier/divider circuit with a THD of less than 0.8% at an output current of 80% of the bias current, a floating input linear V-I convertor with variable transconductance and a THD of less than 0.28% at an output current of 120% of the bias current and a bandwidth of above 5 Mhz, and a four-quadrant voltage multiplier.

INTRODUCTION

A squaring circuit is a fundamental computational circuit with many applications such as multipliers, RMS-DC convertors, modulators, frequency doublers and adaptive filters [1]. Until now little has been published on CMOS squaring circuits.
Especially in systems where large numbers of computational circuits are needed, as for instance adaptive filters, the simplicity of the circuits is very important. The circuits to be shown here excel in simplicity: a three transistor squaring circuit, an eight transistor current multiplier, a ten transistor multiplier/divider circuit, and a thirteen transistor floating input linear V-I convertor with variable transconductance.
The three transistor current squaring circuit is the basic building block with which the above mentioned circuits are built. The current relation of two MOST's with a constant sum of gate-source voltages, as explained in [2], is exploited. First the current squaring circuit is shown. Using two of these devices and a current mirror results in the current multiplier. The linear V-I convertor is realised with a quadratic current feedback to linearise the voltage-to-current conversion of a differential pair. Two of these circuits form the four-quadrant voltage multiplier.

THE THREE TRANSISTOR CURRENT SQUARING CIRCUIT.

Consider the circuit of fig.1. The actual circuits have been

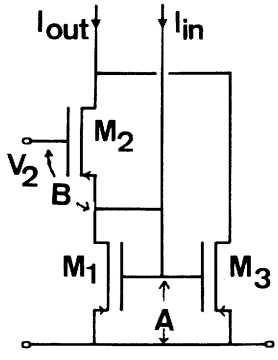

Fig.1. The Basic Current Squaring Circuit.

realised in PMOS as shown in the circuit schemes, however, for reasons of simplicity, the derivation below uses the NMOS equations. All devices have the same geometry and operate in the saturation region. The gate-source voltage of M1 (and M3) is called A and the gate-source voltage of M2 is called B. As shown in the figure:

$$V_2 = A + B \ . \qquad (1)$$

This voltage, representing the sum of gate-source voltages of M1 and M2, is kept constant. Using the simple square-law characteristic

$$I_d = K (V_{gs} - V_t)^2, \qquad (2)$$

the input current I_{in} may be written as

$$I_{in} = I_1 - I_2 = K (A - B)(V_2 - 2V_t) \ . \qquad (3)$$

The output current I_{out} may be written as

$$I_{out} = I_1 + I_3 =$$

$$= K [(V_2 - 2V_t)^2/2 + (I_{in}/(K(V_2 - 2V_t))^2/2] \ . \qquad (4)$$

Equation (4) shows a DC term in the output current dependent only on V_2 and a term dependent on the square of the input current. Note that the input current may be positive as well as negative. This circuit is the basic current squaring circuit. Deriving V_2 from the bias circuit shown in fig.2, the

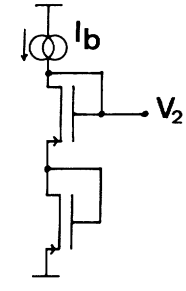

Fig.2. The Biasing Circuit.

following simple expression for the output current evolves:

$$I_{out} = 2 I_b + I_{in}^2/(8 I_b) \ . \qquad (5)$$

Biased in this way the circuit becomes independent on geometries and process parameters. In order to maintain the validity of (2) the input current must be kept within the range:

$$|I_{in}| <= 4 I_b \qquad (6)$$

The utility of this current squaring circuit is demonstrated at the hand of the following three functional circuits.

THE FOUR QUADRANT CURRENT MULTIPLIER.

Fig.3 shows a circuit which performs a multiplication of two

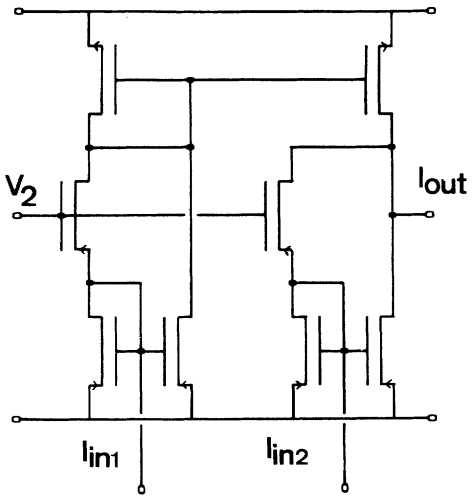

Fig.3. The Four Quadrant Current Multiplier.

currents I_A and I_B. The circuit consists of two current squaring circuits and a current mirror. The input currents of the squaring circuit are chosen:

$$I_{in1} = I_A + I_B \quad , \tag{7}$$

$$I_{in2} = I_A - I_B \quad . \tag{8}$$

The output current is the difference of the output currents of the two squaring circuits. With (5), (7) and (8) I_{out} may be written as:

$$I_{out} = I_A I_B/(2I_b) \quad . \tag{9}$$

So the simple circuit of fig.3 is the core of a four quadrant current multiplier. In order to fullfil restriction (6) the input currents have to be kept within the range:

$$|I_A| + |I_B| <= 4\ I_0. \tag{10}$$

Equation (9) shows that the circuit may also be used as a current divider circuit.

THE LINEAR V-I CONVERTOR.

In this section another usefull application of the current squaring circuit is shown. The circuit performs a linear V-I conversion with variable transconductance.
The voltage to current conversion of a simple differential pair

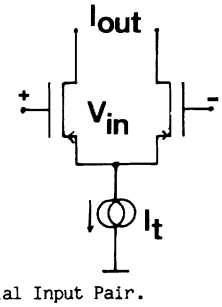

Fig.4. A Differential Input Pair.

as shown in fig.4 is

$$I_{out} = K\ V_{in} \sqrt{2I_t/K - V_{in}^2} \quad . \tag{11}$$

A well-known technique to achieve a linear V-I convertor is described in [3]. In this technique the tail current I_t is replaced by a controlled current:

$$I_t = I_b + K\ V_{in}^2 \quad . \tag{12}$$

Substitution of (12) in (11) yields the following equation for the output current:

$$I_{out} = K\ V_{in} \sqrt{2I_b/K} \quad . \tag{13}$$

Implementation of this technique requires a voltage squaring circuit for the realisation of the square law term in equation (12). The current squaring circuit as described above could be applied preceded by a linear V-I convertor (which is the circuit to be aimed) In fig.5 this solution is shown, where the linear V-I convertor itself is used to supply the current for the current squaring circuit in the tail. It is just like the

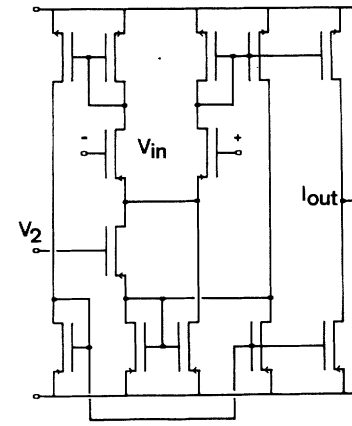

Fig.5. The Linear V-I Convertor.

snake that bites in its own tail. The output current of the circuit in fig.5 may be written as:

$$I_{out} = K\ V_{in}\ (V_2 - 2V_t) \quad . \tag{14}$$

This circuit looks very much like a simple one stage opamp, only four transistors have been added and a linear V-I convertor is obtained. Another advantage of this circuit is that the circuit is adaptively biased: larger output currents are possible because the tail current becomes larger when an input voltage is applied. For proper operation restriction (6) has to be respected and the largest possible output current becomes:

$$I_{outmax} = 4\ I_b \quad , \tag{15}$$

which is achieved at an input voltage of:

$$V_{inmax} = (V_2 - 2V_t) \quad . \tag{16}$$

THE FOUR-QUADRANT VOLTAGE MULTIPLIER.

Using two linear V-I convertors as described above with equal input voltages V_{in} and bias voltages V_2 and V_2' respectively, leads to the following expression for the output current difference:

$$I_{outdif} = K\ (V_2 - V_2')\ V_{in}. \tag{17}$$

This represents a four quadrant voltage multiplication. For proper operation the input voltage should be smaller than indicated in (16):

$$|V_{in}| <= \min[(V_2 - 2V_t),\ (V_2' - 2V_t)] \quad . \tag{18}$$

EXPERIMENTAL RESULTS.

Fig.6 shows the die photograph of the four quadrant current

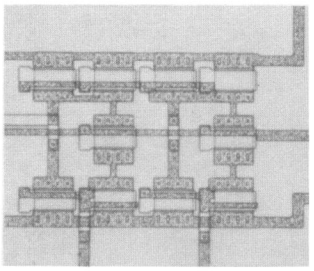

Fig.6. Die photograph of the four quadrant current multiplier.

multiplier. This IC was fabricated in the IC processing facility of Twente University of Technology, using a retrograde twin well CMOS process [4]. As this process has isolated n-wells, the circuits have been realised in PMOS because now the body-effect could be reduced by connecting the well-substrate to the source. The threshold voltage is ¬0.6 V. All devices have the same geometry: W=40 μm, L=20 μm.
Fig. 7 shows the performance of the squaring circuit as a

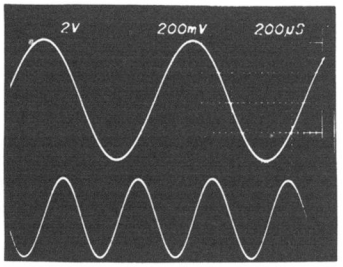

Fig.7. The current squaring circuit as a frequency doubler.

frequency doubler. The input signal was a 1 Khz sine wave of 160 μA_{tt}. The output is a sine wave of twice the input signal frequency and has a magnitude of 60

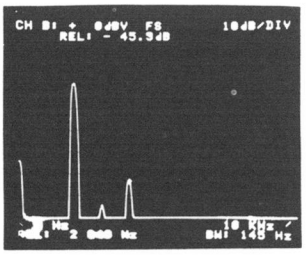

Fig.8. The spectrum of the output signal.

μA_{tt}. Fig.8 shows the spectrum of this output signal; the fourth harmonic of the input signal is the largest distortion component and is more than 45 dB below the desired second harmonic.
Fig.9 and fig.10 show the performance of the four quadrant

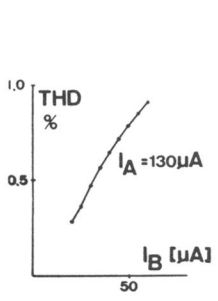

Fig.9. The THD of the current multiplier as a function of I_B.

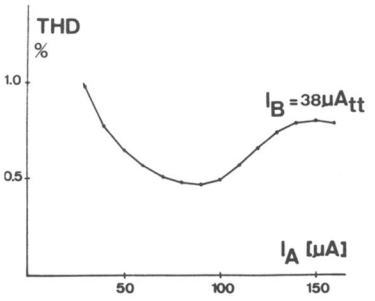

Fig.10. The THD of the current multiplier as a function of I_A.

current multiplier; I_A is a dc current whereas I_B is a 1 KHz sine wave. In fig.9 the THD of the output signal is plotted against the magnitude of the sine wave with I_A= 130 μA and in fig.10 the THD is shown versus the magnitude of the dc current with I_B being a 1 KHz sine wave of 38 μA_{tt}.
Fig.11 and fig.12 show the performance of the linear V-I

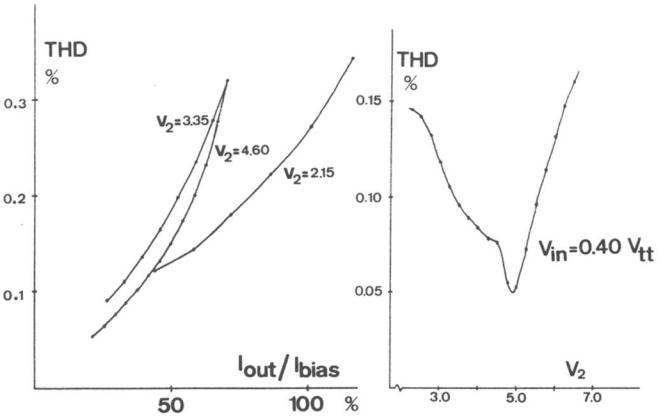

Fig.11. The THD of the LVIC as a function of I_{out}/I_{bias}.

Fig.12. The THD of the LVIC as a function of V_2.

convertor. In fig.11 the THD is plotted against the magnitude of the input sine wave with various values of V_2, and in fig.12 the THD is shown as a function of V_2 with V_{in} being a sine wave of 0.4 V_{tt}.
The bandwidth of the circuits have not yet been investigated thoroughly. Preliminary measurements have already shown a bandwidth of at least 5 MHz for the squaring circuit and 5 MHz for the linear V-I convertor, both measured with a 200 Ohm load resistor and a load capacitor of 30 pF. These are not the largests possible bandwidth values for these circuits. Further investigations have to be performed on this topic.

CONCLUSIONS.

An extremely simple and versatile design for a current squaring circuit is presented. Some important applications have been realized: a four quadrant current multiplier with a measured THD of 0.8% at an output current of 80% of the bias current, a linear V-I convertor with a measured THD of less than 0.28% at an output current of 120% of the bias current.
The bandwidth of these circuits is at least 5 MHz.

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